NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD) 97-06-19

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)*	5. CAGE CODE	6. NOR NO.
	Defense Supply Center, Columbus 3990 East Broad Street Columbus, OH 43216-5000	67268	5962-R364-97
a. TYPED NAME *(First, Middle Initial, Last)*		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-96571**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, OCTAL BUFFER/LINE DRIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON	a. CURRENT A	b. NEW B	No users listed.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "B".
Revisions description column; add "Changes in accordance with NOR 5962-R364-97".
Revisions date column; add "97-06-19".
Revision level block; change “A” to “B”.
Rev status of sheets; for sheet 1 change “A” to “B”; for sheets 4, and 15 through 21, add "B".
Sheet block; change “14” to “21”.

Sheet 4: Add new paragraph which states; "3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document."
Revision level block; add "B".

Sheets 15 through 21: Add attached appendix A.

CONTINUED ON NEXT SHEET

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DSCC-VAC	MONICA L. POELKING

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
CHIEF, CUSTOM MICROELECTRONICS TEAM	MONICA L. POELKING	97-06-19

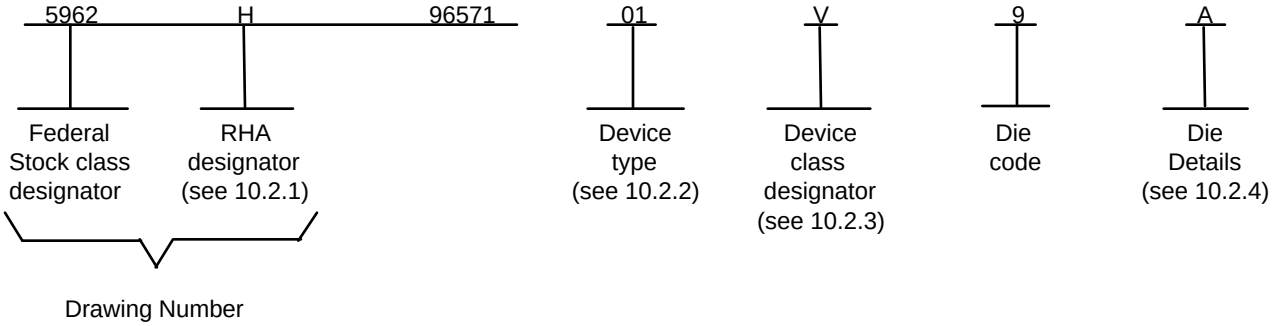
15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED (YYMMDD)
DSCC-VAC	CHARLES F. SAFFLE, JR.	97-06-19

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96571

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN shall be as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACTS244	Radiation Hardened, octal buffer/line driver with three-state outputs, TTL compatible inputs

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96571

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

10.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die Physical dimensions.

Die Type	Figure number
01	A-1

10.2.4.2 Die Bonding pad locations and Electrical functions.

Die Type	Figure number
01	A-1

10.2.4.3 Interface Materials.

Die Type	Figure number
01	A-1

10.2.4.4 Assembly related information.

01	A-1

10.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96571

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item Requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die Physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.6 of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QM" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer Lot acceptance for Class V product using the criteria defined within MIL-STD-883 TM 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 TM2010 or the alternate procedures allowed within MIL-STD-883 TM5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3 and 4.4.4.4.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96571

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined with MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of Supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

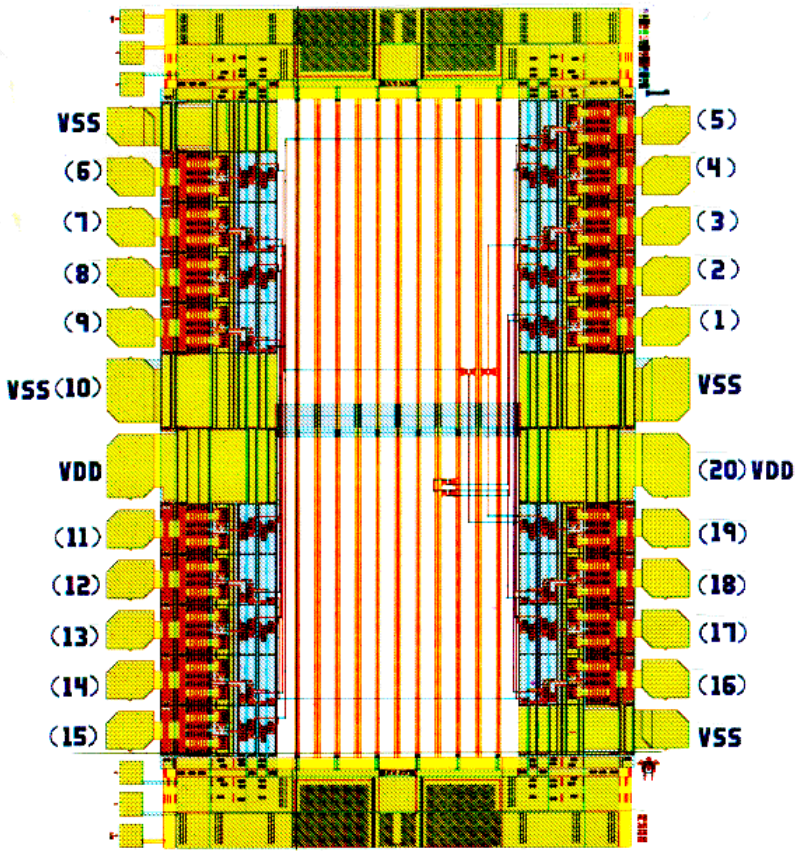
APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96571

FIGURE A-1

o DIE PHYSICAL DIMENSIONS

Die Size:	111 x 81 mils.
Die Thickness:	17 +/- 1 mils.

o DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS



NOTE: Pad numbers reflect terminal numbers when placed in Case Outlines R, X (see Figure 1).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96571

o INTERFACE MATERIALS

Top Metallization:	Si Al Cu	9.0kA - 12.5kA
Backside Metallization:	None: Backgrind.	
Glassivation		
Type:	Phosphorous Doped SiO2	
Thickness:	9.0kA - 11.0kA	
Substrate:	Epitaxial Layer on Single crystal silicon.	

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Tied to VDD.
Special assembly instructions:	Bond pad #20 (VDD) first. Do not wire bond the six probe ID pads.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-06-19

Approved sources of supply for SMD 5962-96571 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962H9657101V9A	65342	UT54ACTS244-VDIE
5962H9657101Q9A	65342	UT54ACTS244-QDIE

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronic Systems 4350 Centennial Boulevard Colorado Springs, CO 80907-3486

NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE *(YYMMDD)* 96-11-19

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME *(First, Middle Initial, Last)*

b. ADDRESS *(Street, City, State, Zip Code)*
Defense Supply Center Columbus
3990 East Broad Street
Columbus, OH 43216-5000

5. CAGE CODE 67268

7. CAGE CODE 67268

6. NOR NO. 5962-R086-97

8. DOCUMENT NO. **5962-96571**

9. TITLE OF DOCUMENT
MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, OCTAL BUFFER/LINE DRIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

10. REVISION LETTER

a. CURRENT -

b. NEW A

11. ECP NO. N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "A".
Revisions description column; add "Changes in accordance with NOR 5962-R086-97".
Revisions date column; add "96-11-19".
Revision level block; add "A".
Rev status of sheets; for sheet 1, 3, 7, and 8, add "A".

Sheet 3: Footnote 4/; following "Derate", add "system".
Revision level block; add "A".

Output current (sink)	I_{OL} 10/	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4$ V	All	4.5 V and 5.5 V	1, 2, 3	12		mA
Output current (source)	I_{OH} 10/	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD} - 0.4$ V	All	4.5 V and 5.5 V	1, 2, 3	-12		mA

Revision level block; add "A".

Sheet 8: Table IA; add the following: "10/ This test is guaranteed based on characterization data but not tested."
Table IB; in last column, change "LET = 3/" to "LET = 3/ 4/" in heading and change "≥ 80" to "≥ 120".
Table IB, add the following after footnote 3/: "4/ Tested to an LET of ≥120 MeV/(mg/cm^2), with no latch-up (SEL)."
Revision level block; add "A".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT
DSCC-VAC

c. TYPED NAME *(First, Middle Initial, Last)*
Monica L. Poelking

d. TITLE
Chief, Custom Microelectronics

e. SIGNATURE
Monica L. Poelking

f. DATE SIGNED *(YYMMDD)* 96-11-19

15a. ACTIVITY ACCOMPLISHING REVISION
DSCC-VAC

b. REVISION COMPLETED *(Signature)*
Jeff Bowling

c. DATE SIGNED *(YYMMDD)* 96-11-19

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thanh V. Nguyen

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
96-03-11

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, OCTAL BUFFER/LINE DRIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

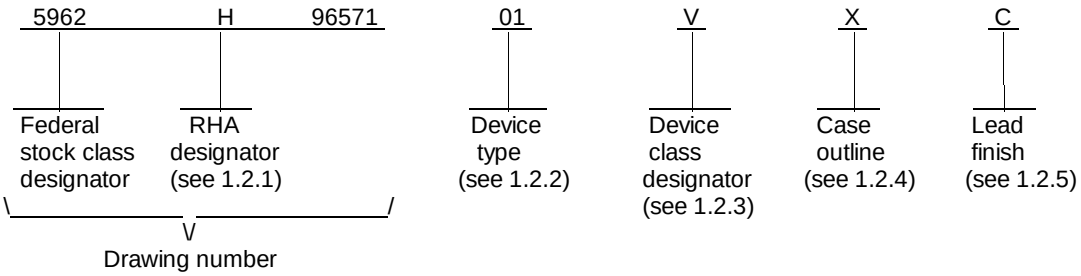
SIZE	CAGE CODE	
A	**67268**	**5962-96571**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACTS244	Radiation hardened, octal buffer/line driver with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
X	CDFP4-F20	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to V_{DD} + 0.3 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current, any one input (I_{IN})	±10 mA
Latch-up immunity current (I_{LU})	±150 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum package power dissipation (P_D)	1.0 W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{DD}
Output voltage range (V_{OUT})	+0.0 V dc to V_{DD}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise and fall time at V_{DD} = 4.5 V (t_r, t_f)	1 ns/V 4/

1.5 Radiation features. 5/

Total dose	> 1 x 10^6 Rads (Si)
Single event phenomenon (SEP) effective linear energy threshold (LET) No upsets (see 4.4.4.4)	> 80 MeV/(mg/cm^2)
Dose rate upset (20 ns pulse)	> 1 x 10^9 Rads (Si)/s
Latch-up	None
Dose rate survivability	> 1 x 10^{12} Rads (Si)/s

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to V_{SS}.

3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise noted.

4/ Derate propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.

5/ Radiation testing is performed on the standard evaluation circuit.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 4.

3.2.6 Irradiation test connections. The irradiation test connections shall be as specified in table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity (ESDS) qualification inspection. ESDS testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 or as specified in QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/ Min	Limits 2/ Max	Unit
High level output voltage	V_{OH}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} $I_{OH} = -12.0$ mA	All	4.5 V	1, 2, 3	3.15		V
		M, D, L, R, F, G, H 3/	All		1	3.15		
Low level output voltage	V_{OL}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} $I_{OL} = 12.0$ mA	All	4.5 V	1, 2, 3		0.4	V
		M, D, L, R, F, G, H 3/	All		1		0.4	
High level input voltage	V_{IH}		All	4.5 V	1, 2, 3	2.25		V
		M, D, L, R, F, G, H 3/	All		1	2.25		
			All	5.5 V	1, 2, 3	2.75		
		M, D, L, R, G, G, H 3/	All		1	2.75		
Low level input voltage	V_{IL}		All	4.5 V	1, 2, 3		0.8	V
		M, D, L, R, F, G, H 3/	All		1		0.8	
			All	5.5 V	1, 2, 3		0.8	
		M, D, L, R, F, G, H 3/	All		1		0.8	
Input current high	I_{IH}	For input under test, $V_{IN} = 5.5$ V For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		+1.0	µA
		M, D, L, R, F, G, H 3/	All		1		+1.0	
Input current low	I_{IL}	For input under test, $V_{IN} = V_{SS}$ For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		-1.0	µA
		M, D, L, R, F, G, H 3/	All		1		-1.0	
Quiescent supply current delta, TTL input levels	ΔI_{DD} 4/	For input under test $V_{IN} = V_{DD}$ -2.1 V For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		1.6	mA
		M, D, L, R, F, G, H 3/	All		1		1.6	
Quiescent supply current	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		10.0	µA
		M, D, L, R, F, G, H 3/	All		1		10.0	
Short circuit output current	I_{OS} 5/ 6/	$V_{OUT} = V_{DD}$ and V_{SS}	All	5.5 V	1, 2, 3		±300	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/ Min	Limits 2/ Max	Unit
Three-state output leakage current high	I_{OZH}	$\overline{mG}$ = 5.5 V For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $V_{OUT} = V_{DD}$	All	5.5 V	1, 2, 3		+30.0	µA
		M, D, L, R, F, G, H 3/	All		1		+30.0	
Three-state output leakage current low	I_{OZL}	$\overline{mG}$ = 5.5 V For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $V_{OUT} = V_{SS}$	All	5.5 V	1, 2, 3		-30.0	µA
		M, D, L, R, F, G, H 3/	All		1		-30.0	
Input capacitance	C_{IN}	f = 1MHz, see 4.4.1c	All	0.0 V	4		15	pF
Output capacitance	C_{OUT}	f = 1MHz, see 4.4.1c	All	0.0 V	4		15	pF
Power dissipation	P_{SW} 7/	C_L = 50 pF, per switching output	All	4.5 V and 5.5 V	4, 5, 6		2.0	mW/ MHz
Functional test	8/	$V_{IH} = 0.5\ V_{DD}$, V_{IL} = 0.8 V See 4.4.1 b	All	4.5 V and 5.5 V	7, 8	L	H	
		M, D, L, R, F, G, H 3/	All		7	L	H	
Propagation delay time, mAn to mYn	t_{PLH} 9/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	1.0	11.0	ns
		M, D, L, R, F, G, H 3/	All		9	1.0	11.0	
	t_{PHL} 9/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	1.0	11.0	
		M, D, L, R, F, G, H 3/	All		9	1.0	11.0	
Propagation delay time, output enable, $\overline{mG}$ to mYn	t_{PZH} 9/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	ns
		M, D, L, R, F, G, H 3/	All		9	2.0	12.0	
	t_{PZL} 9/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	
		M, D, L, R, F, G, H 3/	All		9	2.0	12.0	
Propagation delay time, output disable, $\overline{mG}$ to mYn	t_{PHZ} 9/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	ns
		M, D, L, R, F, G, H 3/	All		9	2.0	12.0	
	t_{PLZ} 9/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	
		M, D, L, R, F, G, H 3/	All		9	2.0	12.0	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{DDQ} and ΔI_{DD} tests, the output terminals shall be open. When performing the I_{DDQ} and ΔI_{DD} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

TABLE IA. Electrical performance characteristics - Continued.

3/ Devices supplied to this drawing meet all levels M, D, L, R, F, G, and H of irradiation. However, these devices are only tested at the "H" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{DD} - 2.1$ V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed. For the preferred method, a minimum of one input shall be tested. All other inputs shall be guaranteed, if not tested, to the limits specified in table IA, herein.

5/ This parameter is supplied as design limit but not guaranteed or tested.

6/ No more than one output should be shorted at a time for a maximum duration of one second.

7/ This value is calculated during the design/qualification process and is supplied as a design limit but is not tested. Total power consumption is determined by both idle/standby power consumption (Ps) and "at frequency" power consumption (Pf). To determine standby power consumption use the formula:

$P_T = (n \times P_{SW} \times f) + (Loads \times Prdy \times I_{OL} \times V_{OL})$

where n is the number of switching outputs; f is the frequency of the device; loads is the resistive power component, typically a TTL load; and Prdy is the percent duty cycle that the output is sinking current.

8/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, L ≤ 0.5 V and H ≥ 4.0 V and are tested at V_{SS} = 4.5 V and V_{SS} = 5.5 V.

9/ For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C 3/	V_{DD} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 3/
		Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section	
01	+25°C	LET ≥ 80	6 x 10^{-9} cm^2/bit	≥ 80

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and quaifying activity.
3/ Worst case temeprature is T_A ≥ +125°C.

Device type	All		
Case outlines	R and X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{1G}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	$\overline{2G}$
10	V_{SS}	20	V_{DD}

FIGURE 1. Terminal connections.

Inputs		Outputs
$\overline{m}\overline{G}$	mAn	mYn
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

FIGURE 2. Truth table.

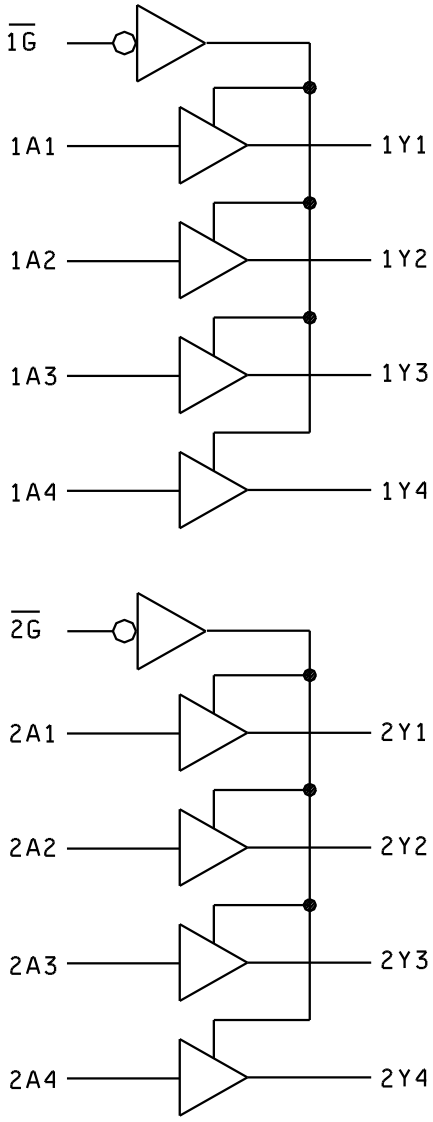
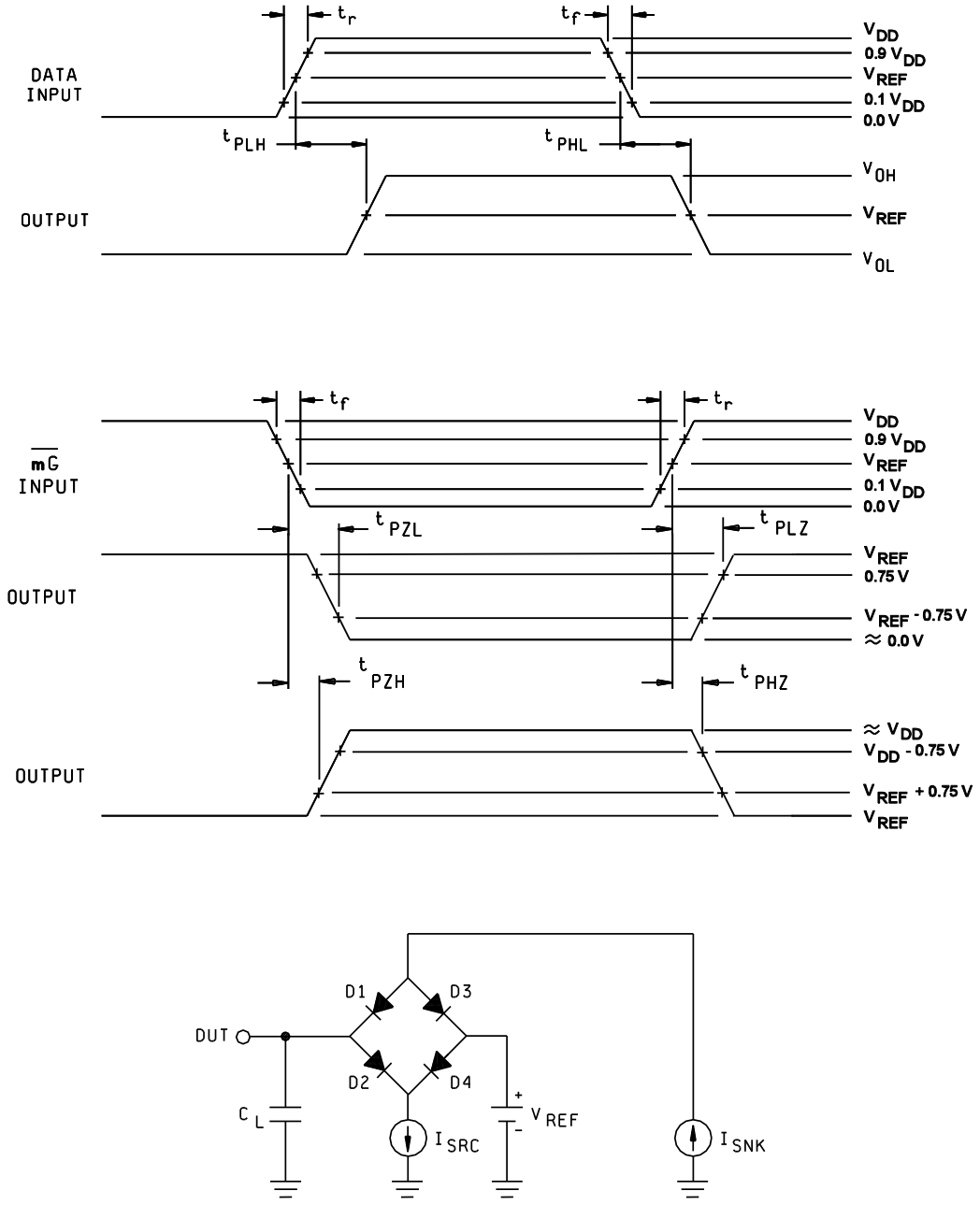


FIGURE 3. Logic diagram.



NOTES:
1/ V_{REF} = 1.4 V.
2/ C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3/ I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL}, t_{PLH}, t_{PZL}, and t_{PZH} measurements. I_{SRC} is set to -12.0 mA and I_{SNK} is set to 12.0 mA for t_{PLZ} and t_{PHZ} measurements.
4/ Input signal from pulse generator: V_{IN} = 0.0 V to V_{DD}; f ≤ 10 MHz; t_r = 1.0 V/ns ±0.3 V/ns; t_f = 1.0 V/ns ±0.3 V/ns; t_r and t_f shall be measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.

FIGURE 4. Switching waveforms and test circuit.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q, and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, test method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging testing. Accelerated aging testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1010 of MIL-STD-883 and as specified herein (see 1.4 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1011 of MIL-STD-883 and herein (see 1.4 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7, and delta's.
3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, Delta parameters (+25°C).

Parameters	Symbol	Delta limits
Output voltage low	V_{OL}	±100 mV
Output voltage high	V_{OH}	±100 mV

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latchup measurements.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

TABLE III. Irradiation test connections.

Device type	Open	Ground	V_{DD} = 5.0 V ±0.5 V
01	3, 5, 7, 9, 12, 14, 16, 18	1, 10, 11, 13, 15 17, 19	2, 4, 6, 8, 20

NOTE: Each pin except 10 and 20 will have a resistor of 2.49 kΩ ±5% for irradiation testing.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-03-11

Approved sources of supply for SMD 5962-96571 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9657101VRA	65342	UT54ACTS244PVAH
5962H9657101VXA	65342	UT54ACTS244UVAH
5962H9657101VRC	65342	UT54ACTS244PVCH
5962H9657101VXC	65342	UT54ACTS244UVCH
5962H9657101QRA	65342	UT54ACTS244PQAH
5962H9657101QXA	65342	UT54ACTS244UQAH
5962H9657101QRC	65342	UT54ACTS244PQCH
5962H9657101QXC	65342	UT54ACTS244UQCH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	United Technologies Microelectronics Center 1575 Garden of Gods Road Colorado Springs, CO 80907-3486