REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																					
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SHEET	15	16	17	18																	
REV STATUS OF SHEETS			REV																		
			SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Larry T. Gauder

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
93-02-08

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY TTL, TRIPLE BIDIRECTIONAL LATCHED BUS TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-91597

SHEET 1 OF 18

DESC FORM 193
JUL 91

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

5962-E430

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

```
  5962         -         91597       01          M          R           X
  |            |                     |           |          |           |
  |            |                     |           |          |           |
  |            |                     |           |          |           |
Federal      RHA                   Device      Device     Case        Lead
stock class  designator            type        class      outline     finish
designator   (see 1.2.1)           (see 1.2.2) designator (see 1.2.4) (see 1.2.5)
\__________________   ___________________/     (see 1.2.3)
                   \/
            Drawing number
```

1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F777	Triple bidirectional latched bus transceiver

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line-package
S	GDFP2-F20 or CDFP3-F20	20	flat package
2	CQCC1-N20	20	square chip carrier package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) - - - - - - - - - - - - - - -0.5 V dc to +7.0 V dc
Threshold control (V_X) - - - - - - - - - - - - - - -0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})
OEB_n, OEA_n, LE_n - - - - - - - - - - - - - - - - -0.5 V dc to +7.0 V dc
A_0 - A_2, B_0 - B_2 - - - - - - - - - - - - - - - - -0.5 V dc to +5.5 V dc
Input current range (I_{IN}) - - - - - - - - - - - - -30 mA to + 5.0 mA
Voltage applied to output in
high output state range (V_{OUT}) - - - - - - - - - - -0.5 V dc to +V_{CC}
Current applied to output in low output state (I_{OUT})
A_0 - A_2 - 40 mA
B_0 - B_2 - 200 mA
Storage temperature range (T_{STG}) - - - - - - - - - - -65°C to +150°C
Maximum power dissipation (P_D) 2/- - - - - - - - - - 440 mW
Lead temperature (soldering, 10 seconds) - - - - - +300°C
Junction temperature (T_J) - - - - - - - - - - - - - +175°C
Thermal resistance, junction-to-case (Θ_{JC}) - - - - See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - - - - - - - - - - - - - - - - +4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})
Except B_0 - B_2 - - - - - - - - - - - - - - - - +2.0 V dc
B_0 - B_2 - +1.6 V dc
Maximum low level input voltage (V_{IL})
Except B_0 - B_2 - - - - - - - - - - - - - - - - +0.8 V dc
B_0 - B_2 - +1.43 V dc
Maximum input clamp current (I_{IK})
Except A_0 - A_2 - - - - - - - - - - - - - - - - -18 mA
A_0 - A_2 -40 mA
Maximum high level output current (I_{OH})
A_0 - A_2 -3 mA
Maximum low level output current (I_{OL})
A_0 - A_2 - +20 mA
B_0 - B_2 - +90 mA
Case operating temperature range (T_C)- - - - - - -55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) - - - - - - - - XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Maximum power dissipation is defined as V_{CC} x I_{CC} and must withstand the added P_D due to the short-circuit output test (e.g., I_{OS}).

3/ Values will be added when they become available.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuits and switching waveforms. The test circuits and switching waveforms shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 9 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

  (1) Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

  (2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified			Group A Subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	A_0 - A_2 2/	V_{CC} = 4.5 V V_{IL} = 1.43 V for B_n. V_{IL} = 0.8 V for other inputs. V_{IH} = 1.6 V for B_n. V_{IH} = 2.0 V for other inputs.	I_{OH} = -3 mA V_X = 4.5 V	1, 2, 3	2.4	4.5	V
				I_{OH} = 0.4 mA V_X = 3.13 V	1, 2, 3	2.5	3.13	
				I_{OH} = 0.4 mA V_X = 3.47 V	1, 2, 3	2.5	3.47	
Low level output voltage	V_{OL}			I_{OL} = 20 mA V_X = 4.5 V	1, 2, 3		0.50	
		B_0 - B_2	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OL} = 90 mA	1, 2, 3		1.15	
				I_{OL} = 4 mA	1, 2, 3	0.40		
Input clamp voltage	V_{IK}	A_0 - A_2	V_{CC} = 4.5 V, I_{IN} = -40 mA		1, 2, 3		-0.5	V
		Except A_0 - A_2	V_{CC} = 4.5 V I_{IN} = -18 mA		1, 2, 3		-1.2	
High level output current	I_{OH}	B_0 - B_2	V_{CC} = 5.5 V, V_{IL} = 0.8 V V_{OH} = 2.1 V V_{IH} = 2.0 V		1, 2, 3		100	µA
Power-off output current	I_{OFF}	B_0 - B_2	V_{CC} = 0.0 V, V_{IL} = 0.8 V V_{OH} = 2.1 V V_{IH} = 2.0 V		1, 2, 3		100	
High level input current	I_{IH1}	$\overline{OEB}_n$, OEA_n, LE_n		V_{CC} = 5.5 V V_{IN} = 2.7 V $B_n - A_n$ = 0 V	1, 2, 3		20	µA
		B_0 - B_2		V_{CC} = 5.5 V V_{IN} = 2.1 V	1, 2, 3		100	
	I_{IH2}	$\overline{OEB}_n$, OEA_n, LE_n		V_{CC} = 5.5 V V_{IN} = 7.0 V	1, 2, 3		100	
		A_0 - A_2, B_0 - B_2		V_{CC} = 5.5 V V_{IN} = 5.5 V	1, 2, 3		1.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified		Group A Subgroups	Limits		Unit
					Min	Max	
Low level input current	I_{IL}	$\overline{OEB}_n$, OEA_n, LE_n	V_{CC} = 5.5 V V_{IN} = 0.5 V	1, 2, 3		-20	µA
		B_0 - B_2	V_{CC} = 5.5 V V_{IN} = 0.3 V	1, 2, 3		-100	
Off-state output current, high level voltage applied	I_{OZH}	A_0 - A_2	V_{CC} = 5.5 V V_{OUT} = 2.7 V	1, 2, 3		70	
Off-state output current, low level voltage applied	I_{OZL}	A_0 - A_2	V_{CC} = 5.5 V V_{OUT} = 0.5 V	1, 2, 3		-70	
High level control current	I_X	V_{CC} = 5.5 V, V_X = 5.5 V, $\overline{LE}_n$ = OEA_n = $\overline{OEB}_n$ = 2.7 V, A_0 - A_2 = 2.7 V, B_0 - B_2 = 2.0 V		1, 2, 3	-100	100	
		V_{CC} = 5.5 V, V_X = 3.13 V and 3.47 V $\overline{LE}_n$ = OEA_n = $\overline{OEB}_n$ = 2.7 V, A_0 - A_2 = 2.7 V, B_0 - B_2 = 2.0 V		1, 2, 3	-10	10	mA
Short circuit output current	I_{OS} 3/	A_0 - A_2 only	V_{CC} = 5.5 V, B_n = 1.8 V OEA_n = 2.0 V $\overline{OEB}_n$ = 2.7 V	1, 2, 3	-60	-150	
Supply current, total	I_{CCH}	V_{CC} = 5.5 V		1, 2, 3		60	
	I_{CCL}		V_{IL} = 0.5V			80	
	I_{CCZ}					67	
Functional tests		See 4.4.1b, V_{CC} = 4.5 V, 5.5 V		7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +125^{\circ}C$ 1/ unless otherwise specified			Group A Subgroups	Limits		Unit
						Min	Max	
Propagation delay time, B_n to A_n	t_{PLH1}	A PORT	R_L = 500Ω C_L = 50 pF See figure 4	V_{CC} = 5.0 V	9	8.5	13.0	ns
				V_{CC} = 4.5 V, 5.5 V	10, 11	5.0	15.0	
	t_{PHL1}			V_{CC} = 5.0 V	9	7.5	12.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	7.5	14.0	
Output enable time to high or low, OEA_n to A_n	t_{PZH}			V_{CC} = 5.0 V	9	8.0	13.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	7.0	16.0	
	t_{PZL}			V_{CC} = 5.0 V	9	9.0	14.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	8.0	18.5	
Output disable time from high or low, OEA_n to A_n	t_{PHZ}			V_{CC} = 5.0 V	9	1.5	6.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	1.0	6.5	
	t_{PLZ}			V_{CC} = 5.0 V	9	1.5	6.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	1.0	6.5	
Propagation delay time, A_n to B_n	t_{PLH2}	B PORT	R_U = 9Ω C_L = 30 pF See figure 4	V_{CC} = 5.0 V	9	3.0	7.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	1.5	10.0	
	t_{PHL2}			V_{CC} = 5.0 V	9	4.0	9.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	3.5	11.5	
Propagation delay time, LE_n to B_n	t_{PLH3}			V_{CC} = 5.0 V	9	3.5	8.0	
				V_{CC} = 4.5 V, 5.5 V	10, 11	2.0	11.5	
	t_{PHL3}			V_{CC} = 5.0 V	9	5.5	10.5	
				V_{CC} = 4.5 V, 5.5 V	10, 11	5.0	12.0	
Enable/disable time, OEB_n to B_n	t_{PLH4}			V_{CC} = 5.0 V	9	3.0	7.5	
				V_{CC} = 4.5 V, 5.5 V	10, 11	2.0	10.0	
	t_{PHL4}			V_{CC} = 5.0 V	9	4.5	10.5	
				V_{CC} = 4.5 V, 5.5 V	10, 11	4.0	12.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ 1/ unless otherwise specified			Group A Subgroups	Limits		Unit
						Min	Max	
Transition time, B Port 1.3 V to 1.7 V, 1.7 V to 1.3 V 4/	t_{PLH5}	B PORT	R_U = 9Ω C_L = 30 pF See figure 4	V_{CC} = 5.0 V V_{CC} = 4.5 V, 5.5 V	9 10, 11	0.5 0.5	4.5 7.0	ns
	t_{PHL5}			V_{CC} = 5.0 V V_{CC} = 4.5 V, 5.5 V	9 10, 11	0.5 0.5	4.5 4.5	
Setup time, A_n to LE_n	t_s (H)	R_L = 500Ω C_L = 50 pF See figure 4		V_{CC} = 5.0 V V_{CC} = 4.5 V, 5.5 V	9 10, 11	4.0 4.5		
	t_s (L)			V_{CC} = 5.0 V V_{CC} = 4.5 V, 5.5 V	9 10, 11	4.5 4.5		
Hold time, A_n to LE_n	t_h (H)			V_{CC} = 5.0 V V_{CC} = 4.5 V, 5.5 V	9 10, 11	0.0 0.0		
	t_h (L)			V_{CC} = 5.0 V V_{CC} = 4.5 V, 5.5 V	9 10, 11	0.0 0.0		
$\overline{LE}_n$ Pulse width, low	t_w (L)			V_{CC} = 5.0 V V_{CC} = 4.5 V, 5.5 V	9 5/ 10, 11	5.5 7.0		

1/ Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
2/ Due to test equipment limitations actual test conditions are for V_{IH} = 1.8 V and V_{IL} = 1.3 V.
3/ Not more than one output should be shorted at a time. I_{OS} testing should be performed last.
4/ This parameter may be guaranteed by the manufacturer in place of testing.
5/ For subgroup 9, due to test equipment limitations, the actual test limit is 7.0 ns, but the specified limit is guaranteed.

Device type	01
Case outlines	R, S and 2
Terminal number	Terminal symbol
1	$\overline{LE}_0$
2	$\overline{LE}_1$
3	$\overline{LE}_2$
4	OEA_0
5	A_0
6	OEA_1
7	A_1
8	OEA_2
9	A_2
10	GND
11	$\overline{OEB}_2$
12	$\overline{OEB}_1$
13	$\overline{OEB}_0$
14	GND
15	B_2
16	B_1
17	B_0
18	GND
19	V_X
20	V_{CC}

FIGURE 1. Terminal connections.

INPUTS					LATCH STATE	OUTPUTS		MODE
A_n	B_n 4/	$\overline{LE}_n$	OEA_n	$\overline{OEB}_n$		A_n	B_n	
H	X	L	L	L	H	Z	H 3/	A three-state, data from A to B
L	X	L	L	L	L	Z	L	
X	X	H	L	L	Q_n	Z	Q_n	A three-state, latched data to B
-	-	L	H	L	1/	1/	1/	Feedback: A to B, B to A
-	H	H	H	L	H 2/	H	Z 2/	Preconditioned latch enabling data transfer from B to A
-	L	H	H	L	H 2/	L	Z 2/	
-	-	H	H	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	H	Z	Z	B and A three-state
L	X	L	L	H	L	Z	Z	
X	X	H	L	H	Q_n	Z	Z	
-	H	L	H	H	H	H	Z	B three-state, data from B to A
-	L	L	H	H	L	L	Z	
-	H	H	H	H	Q_n	H	Z	
-	L	H	H	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Irrelevant
- = Input not externally driven
Z = High impedance state
Q_n = High or low voltage level one setup time prior to the low-to-high $\overline{LE}$ transition
1/ = Condition will cause a feedback loop path; A to B and B to A.
2/ = The latch must be preconditioned such that B inputs may assume a high or low level while OEB_0 and OEB_1 are low and LE is high.
3/ = H; Goes to level of pullup voltage.
4/ = B; Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

FIGURE 2. Truth table.

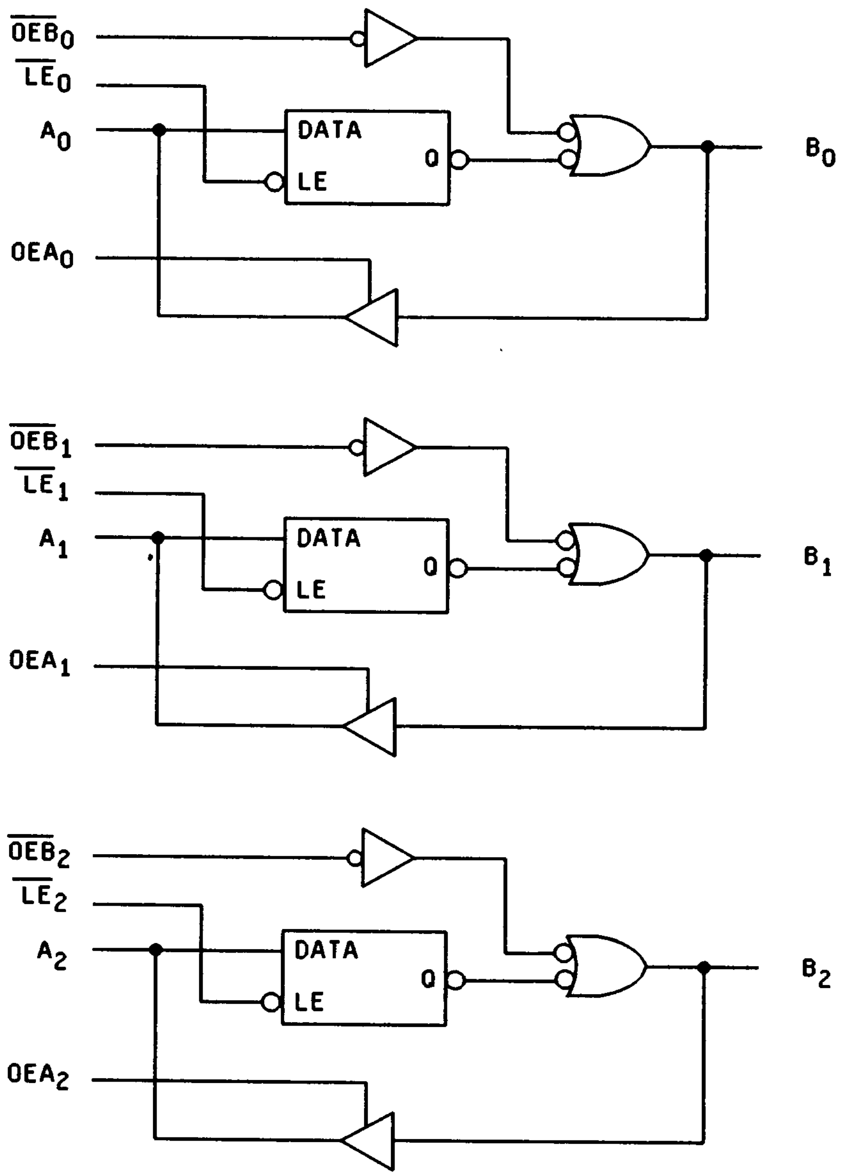
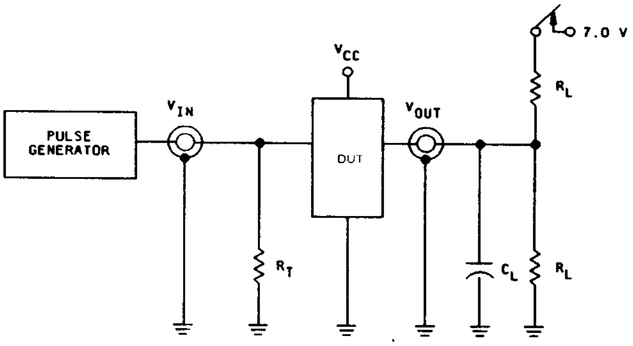


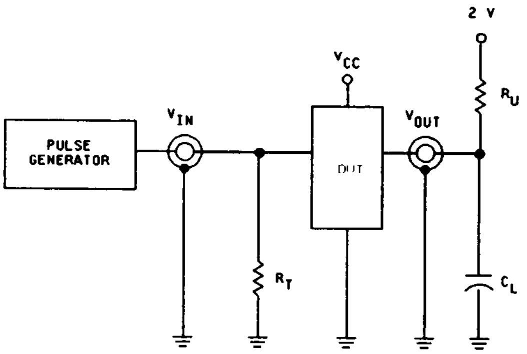
FIGURE 3. Logic diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91597
		REVISION LEVEL	SHEET 12



Test circuit for three-state outputs on A port

Test	Switch
t_{PLZ}	Closed
t_{PLZ}	Closed
All other	Open

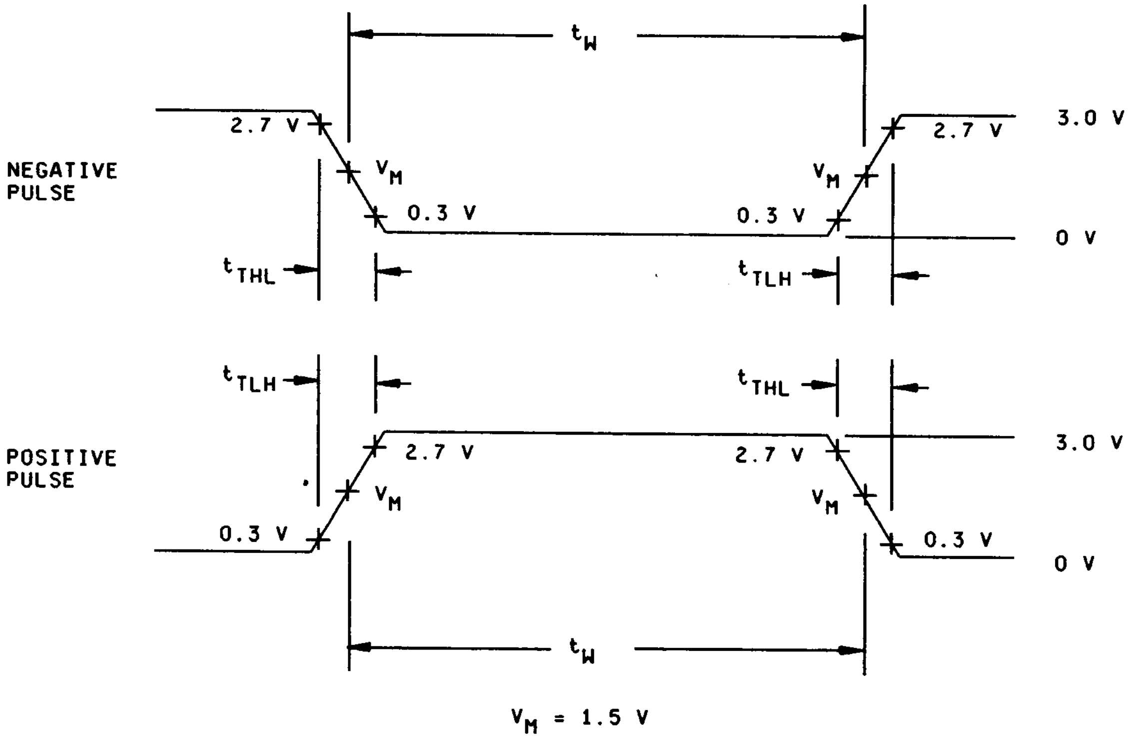


Test circuit for three-state outputs on B port

NOTES:

R_L = Load resistor; see table I for value.
C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination resistance should be equal to Z_{OUT} for pulse generators.
R_U = Pull up resistor.

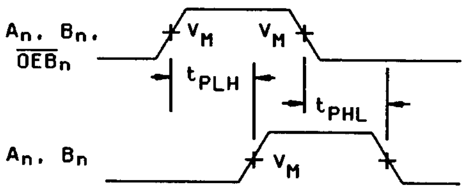
FIGURE 4. Test circuits and switching waveforms.



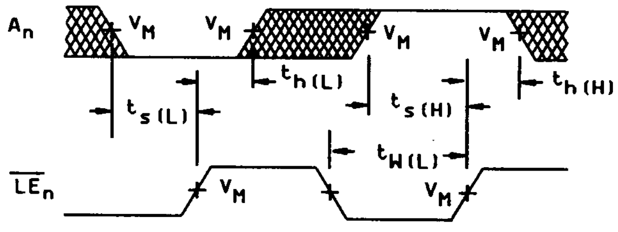
Input pulse definition

	Input pulse characteristics					
	Amplitude	Low V	Rep. rate	t_W	t_{TLH}	t_{THL}
A Side	3.0 V	0.0 V	1 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns
B Side	2.0 V	1.0 V	1 MHz	500 ns	≤ 4.0 ns	≤ 4.0 ns

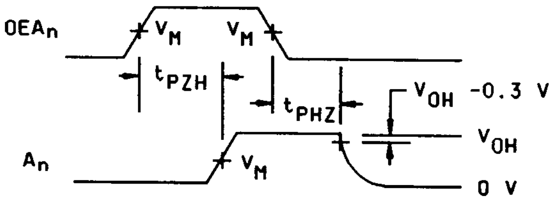
FIGURE 4. Test circuits and switching waveforms - Continued



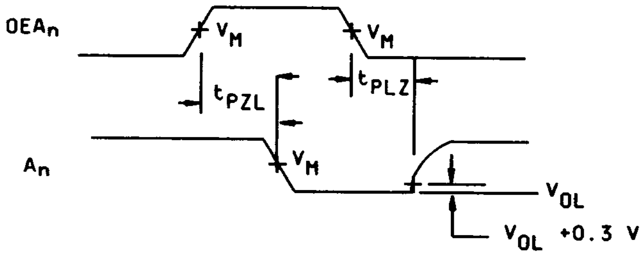
Propagation delay for data to output and enable/disable time $\overline{OEB}_n$ to B_n



Data setup and hold times and $\overline{LE}$ pulse width



Three-state output enable time to high level and output disable time from high level



Three-state output enable time to low level and output disable time from low level

NOTE: For all waveforms, V_M = 1.5 V.

FIGURE 4. Test circuits and switching waveforms - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table II herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1,7		1,7
Final electrical parameters (see 4.2)	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 2/	1,2,3,7, 8,9,10,11 2/	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 1/
Group A test requirements (see 4.4)	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,2,3,7, 8,9,10,11		
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3,7, 8,9,10,11		1,2,3,7, 8,9,10,11	1,2,3,7 8,9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in ccordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.5 Symbols, definitions, and functional descriptions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.