

4V+2.5V Drive Nch+Nch MOSFET

US6M1

●Structure

Silicon N-channel / P-channel MOSFET

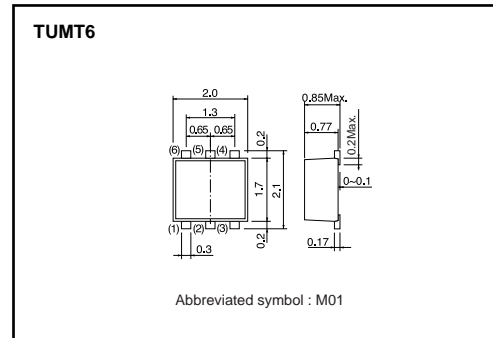
●Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (TUMT6).

●Application

Power switching, DC / DC converter.

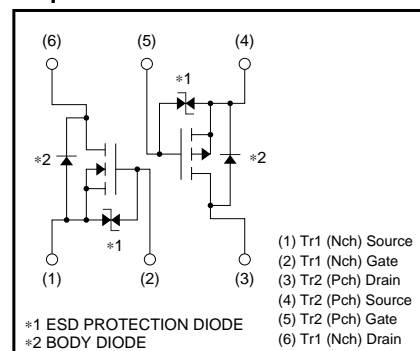
●Dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6M1		○

●Equivalent circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit	
		Tr1 : Nchannel	Tr2 : Pchannel		
Drain-source voltage	V _{BSS}	30	-20	V	
Gate-source voltage	V _{GSS}	20	-12	V	
Drain current	Continuous	I _D	±1.4	±1	A
	Pulsed	I _{DP} *1	±5.6	±4	A
Source current (Body diode)	Continuous	I _S	0.6	-0.4	A
	Pulsed	I _{SP} *1	5.6	-4	A
Total power dissipation	P _D *2	1		W / TOTAL	
		0.7		W / ELEMENT	
Channel temperature	T _{ch}	150		°C	
Storage temperature	T _{stg}	-55 to +150		°C	

*1 Pw≤10μs, Duty cycles≤1%
 *2 Mounted on a ceramic board.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	R _{th} (ch-a)*	125	°C / W / TOTAL
		179	°C / W / ELEMENT

*2 Mounted on a ceramic board.

Transistors

N-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{gss}	–	–	10	μA	V _{GS} =20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	30	–	–	V	I _D =1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	1	μA	V _{DS} =30V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	1.0	–	2.5	V	V _{DS} =10V, I _D =1mA
Static drain-source on-state resistance	R _{DS(on)} [*]	–	170	240	mΩ	I _D =1.4A, V _{GS} =10V
		–	250	350		I _D =1.4A, V _{GS} =4.5V
		–	270	380		I _D =1.4A, V _{GS} =4V
Forward transfer admittance	Y _{fs} [*]	1.0	–	–	S	I _D =1.4A, V _{DS} =10V
Input capacitance	C _{iss}	–	70	–	pF	V _{DS} =10V
Output capacitance	C _{oss}	–	15	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	12	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} [*]	–	6	–	ns	I _D =0.7A, V _{DD} ≐15V
Rise time	t _r [*]	–	6	–	ns	V _{GS} =10V
Turn-off delay time	t _{d(off)} [*]	–	13	–	ns	R _L =21Ω
Fall time	t _f [*]	–	8	–	ns	R _G =10Ω
Total gate charge	Q _g [*]	–	1.4	2.0	nC	V _{DD} ≐15V R _L =11Ω
Gate-source charge	Q _{gs} [*]	–	0.6	–	nC	V _{GS} =5V R _G =10Ω
Gate-drain charge	Q _{gd} [*]	–	0.3	–	nC	I _D =1.4A

*Pulsed

●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward voltage	V _{SD}	–	–	1.2	V	I _S =0.6A, V _{GS} =0V

Transistors

P-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	–10	μA	$V_{GS}=12V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–20	–	–	V	$I_D = -1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS} = -20V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	–0.7	–	–2.0	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	280	390	m Ω	$I_D = -1A, V_{GS} = -4.5V$
		–	310	430		$I_D = -1A, V_{GS} = -4V$
		–	570	800		$I_D = -0.5A, V_{GS} = -2.5V$
Forward transfer admittance	$ Y_{fs} $ *	0.7	–	–	S	$I_D = -0.5A, V_{DS} = -10V$
Input capacitance	C_{iss}	–	150	–	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	–	20	–	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	–	20	–	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	9	–	ns	$I_D = -0.5A, V_{DD} = -15V$
Rise time	t_r *	–	8	–	ns	$V_{GS} = -4.5V$
Turn-off delay time	$t_{d(off)}$ *	–	25	–	ns	$R_L = 30\Omega$
Fall time	t_f *	–	10	–	ns	$R_G = 10\Omega$
Total gate charge	Q_g *	–	2.1	–	nC	$V_{DD} = -15V, R_L = 15\Omega$
Gate-source charge	Q_{gs} *	–	0.5	–	nC	$V_{GS} = -4.5V, R_G = 10\Omega$
Gate-drain charge	Q_{gd} *	–	0.5	–	nC	$I_D = -1A$

*Pulsed

●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward voltage	V_{SD}	–	–	–1.2	V	$I_S = -0.4A, V_{GS} = 0V$

Transistors

N-ch

●Electrical characteristic curves

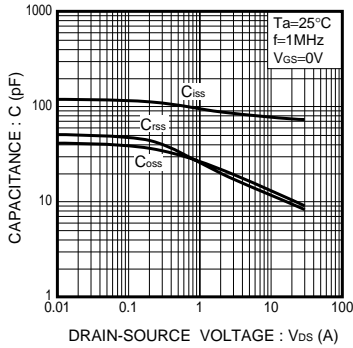


Fig.1 Typical Capacitance vs. Drain-Source Voltage

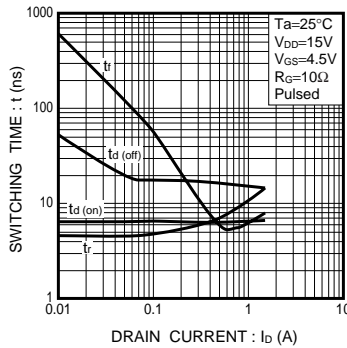


Fig.2 Switching Characteristics

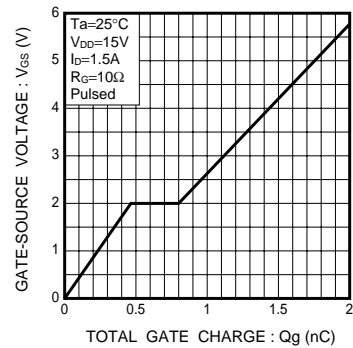


Fig.3 Dynamic Input Characteristics

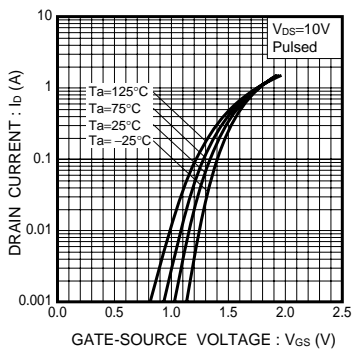


Fig.4 Typical Transfer Characteristics

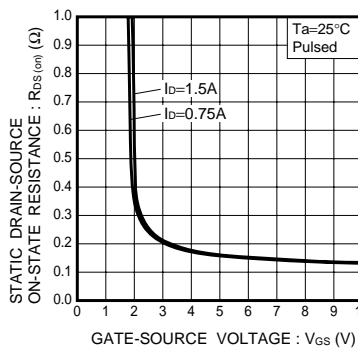


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

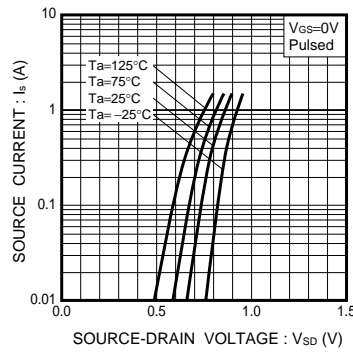


Fig.6 Source Current vs. Source-Drain Voltage

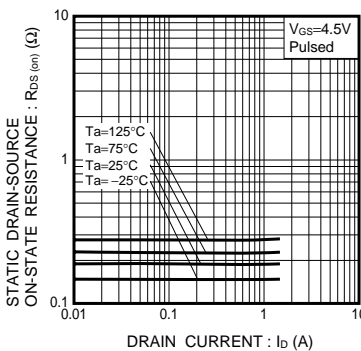


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

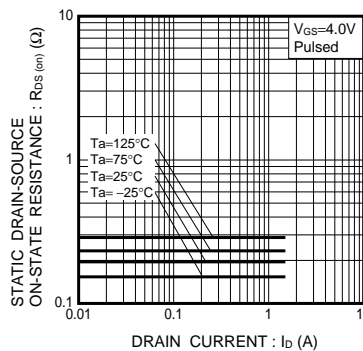


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

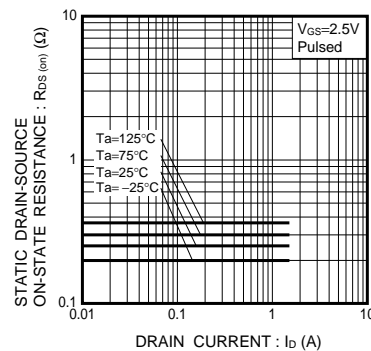


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

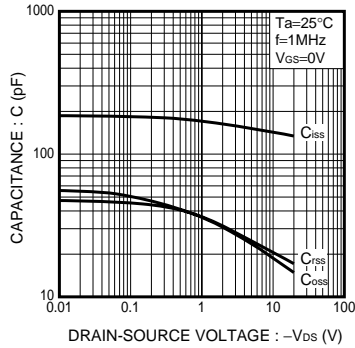


Fig.1 Typical Capacitance vs. Drain-Source Voltage

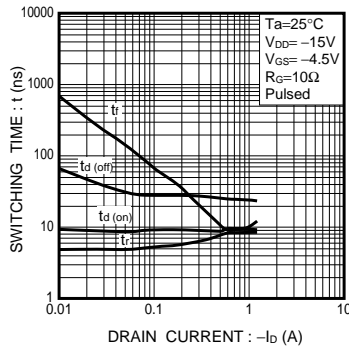


Fig.2 Switching Characteristics

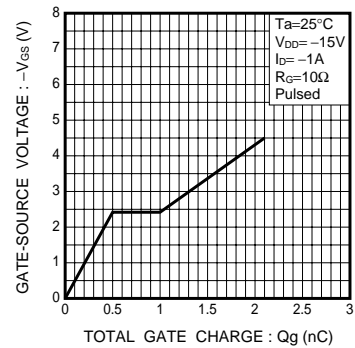


Fig.3 Dynamic Input Characteristics

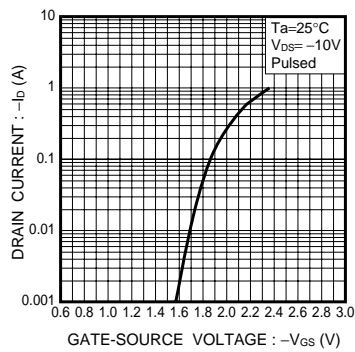


Fig.4 Typical Transfer Characteristics

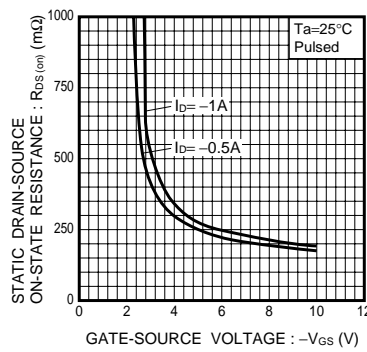


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

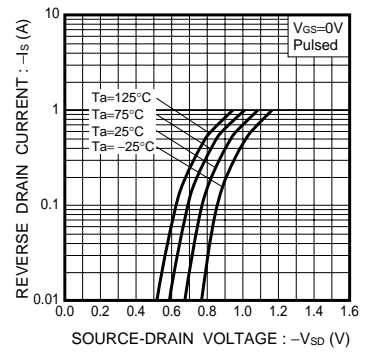


Fig.6 Source Current vs. Source-Drain Voltage

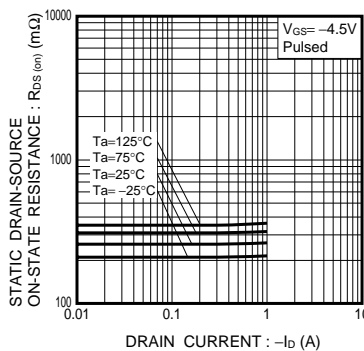


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

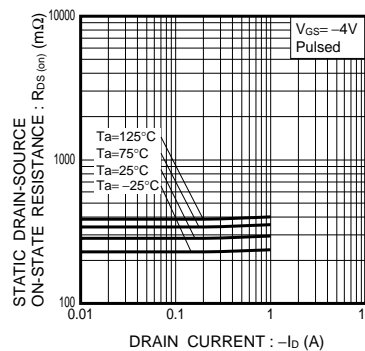


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

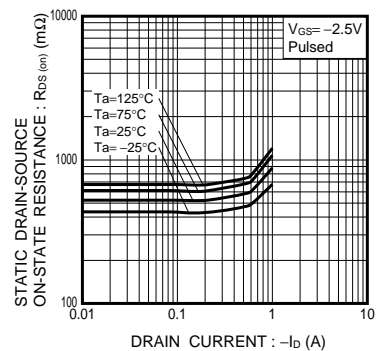


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

N-ch

● Measurement circuit

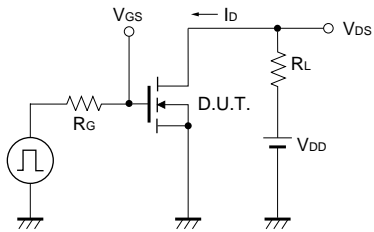


Fig.1-1 Switching Time Measurement Circuit

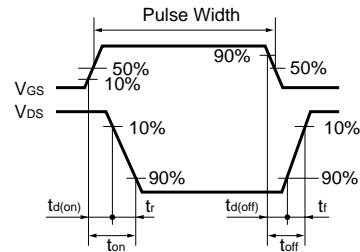


Fig.1-2 Switching Waveforms

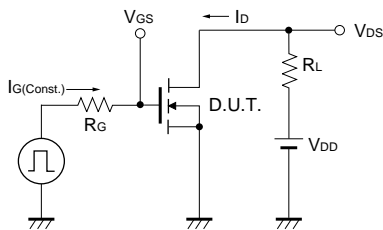


Fig.2-1 Gate Charge Measurement Circuit

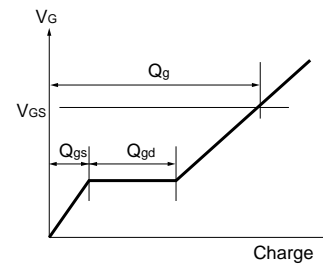


Fig.2-2 Gate Charge Waveform

Transistors

P-ch

●Measurement circuit

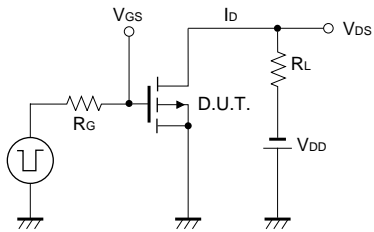


Fig.3-1 Switching Time Measurement Circuit

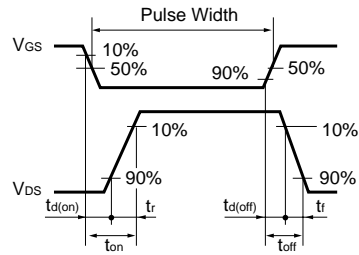


Fig.3-2 Switching Waveforms

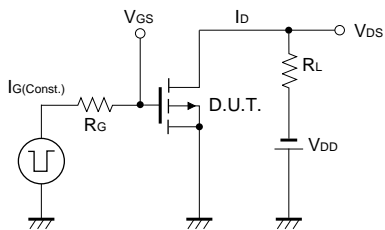


Fig.4-1 Gate Charge Measurement Circuit

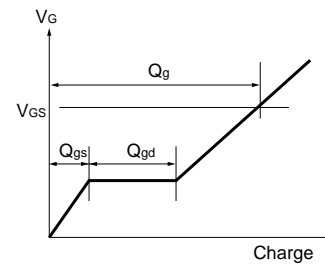


Fig.4-2 Gate Charge Waveform

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