

NEC

MOS INTEGRATED CIRCUIT

μ PD78052, 78053, 78054, 78055, 78056, 78058

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μ PD78052, 78053, 78054, 78055, 78056 and 78058 are the μ PD78054 subseries products of the 78K/0 series. 8-bit resolution D/A converter, timer, serial interface, real-time output port and interrupt functions.

The μ PD78P054, a one-time PROM or EPROM product which can be operated in the same supply voltage range as for the mask ROM product, and various development tools are also available.

Details of the function description, etc, are described in the following User's Manual. Be sure to read it when designing.

μ PD78054 Subseries User's Manual: IEU-1356
78K/0 Series User's Manual Instruction: IEU-1372

FEATURES

- Large on-chip ROM & RAM

Products Name	Items	Program Memory (ROM)	Data Memory		
			Internal High-Speed RAM	Buffer RAM	Internal Expanded RAM
μ PD78052		16K bytes	512 bytes	32 bytes	No
μ PD78053		24K bytes	1024 bytes		
μ PD78054		32K bytes			
μ PD78055		40K bytes			
μ PD78056		48K bytes			
μ PD78058		60K bytes			1024 byte

- External memory expansion space: 64K bytes
- Instruction execution time can be varied from high-speed (0.4 μ s) to ultra-low-speed (122 μ s)
- I/O ports: 69 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- 8-bit resolution D/A converter : 2 channels
- Serial interface : 3 channels
- Timer: 5 channels
- Operating voltage range: 2.0 to 6.0 V

APPLICATION

Pocket telephone, pager, printer, AV equipment, airconditioners, cameras, PPC, fuzzy home appliances, vending machine, etc.

The information in this document is subject to change without notice.

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The mark * shows major revised points.

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ORDERING INFORMATION

Part Number	Package
μPD78052GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)
μPD78052GK-xxx-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78053GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)
μPD78053GK-xxx-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78054GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)
μPD78054GK-xxx-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78055GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)
μPD78056GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)
★ μPD78058GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)

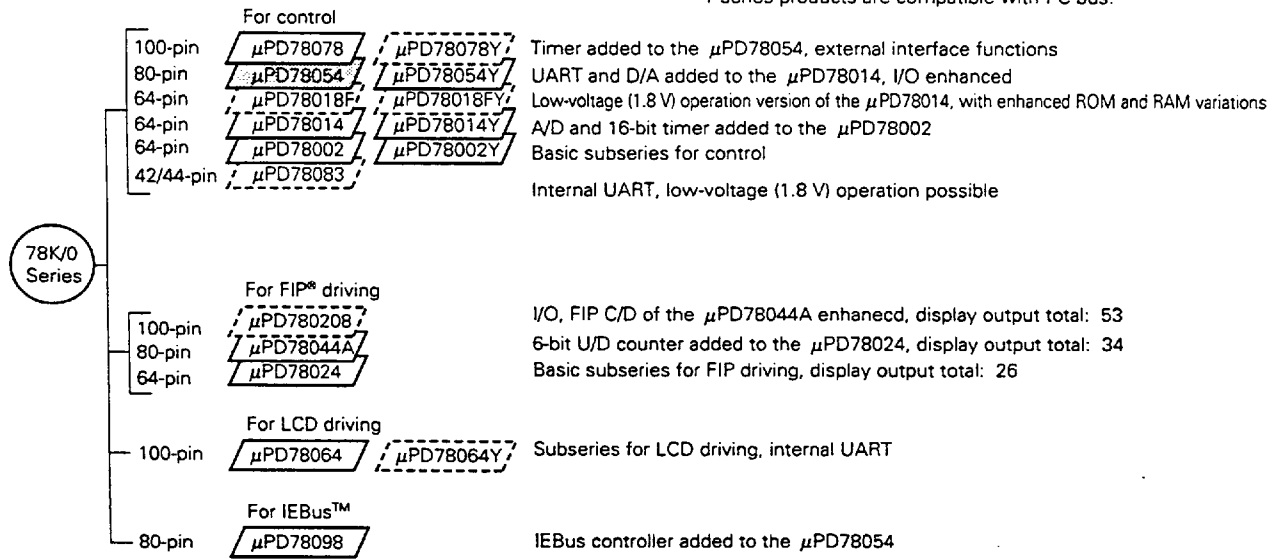
Remark xxx denotes the ROM code number.

78K/0 SERIES PRODUCT DEVELOPMENT



These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.

Products in Volume Production
 Products under Development
 Y series products are compatible with I²C bus.



The major functional differences among the subseries are shown below.

Name	Function	Timer				A/D	D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion						
		8-bit	16-bit	Watch	Watchdog												
For Control	μPD78078	4ch	1ch	1ch	1ch	8-bit × 8ch	8-bit × 2ch	3ch (UART: 1ch)	88	1.8 V	C						
	μPD78054	2ch	1ch	1ch	1ch				—	2ch		69	2.0 V				
	μPD78018F							—				—	—	—	1ch	53	1.8 V
	μPD78014															2.7 V	
	μPD78002							—				—	—	—	—	1ch	—
	μPD78083	—	—	—	—	8-bit × 8ch	1ch (UART: 1ch)	33	1.8 V	—							
For FIP® driving	μPD780208	2ch	1ch	1ch	1ch	8-bit × 8ch	—	2ch	74	2.7 V	—						
	μPD78044A								68	—							
	μPD78024								54	—							
For LCD driving	μPD78064	2ch	1ch	1ch	1ch	8-bit × 8ch	—	2ch (UART: 1ch)	57	2.0 V	—						
For IEBus™	μPD78098	2ch	1ch	1ch	1ch	8-bit × 8ch	8-bit × 2ch	3ch (UART: 1ch)	69	2.7 V	C						

OVERVIEW OF FUNCTION

Item		Product Name					
		μPD78052	μPD78053	μPD78054	μPD78055	μPD78056	μPD78058
Internal memory	ROM	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes	60K bytes
	Internal high-speed RAM	512 bytes	1024 bytes				
	Buffer RAM	32 bytes					
	Internal expanded RAM	None					1024K bytes
Memory space		64 K bytes					
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)					
Instruction cycle		On-chip instruction execution time cycle modification function					
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0 MHz operation)					
	When subsystem clock selected	122 μs (at 32.768 kHz operation)					
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits + 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc. 					
I/O ports		Total : 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O : 4					
A/D converter		• 8-bit resolution × 8 channels					
D/A converter		• 8-bit resolution × 2 channels					
Serial interface		<ul style="list-style-type: none"> • 3-wire/SBI/2-wire mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel • 3-wire/UART mode selectable: 1 channel 					
Timer		<ul style="list-style-type: none"> • 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel 					
Timer output		3 (14-bit PWM output × 1)					
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock 5.0 MHz operation) 32.768 kHz (at subsystem clock 32.768 kHz operation)					
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 5.0 MHz operation)					
Vectored interrupts	Maskable interrupts	Internal interrupt : 13, external interrupt : 7					
	Non-maskable interrupts	Internal interrupt : 1					
	Software interrupts	Internal interrupt : 1					
Test input		Internal : 1, external : 1					
Operating voltage range		VDD = 2.0 to 6.0 V					
Operating temperature range		- 40 to + 85°C					
Package		<ul style="list-style-type: none"> • 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)^{Note} 					

★ Note μPD78052, 78053, 78054



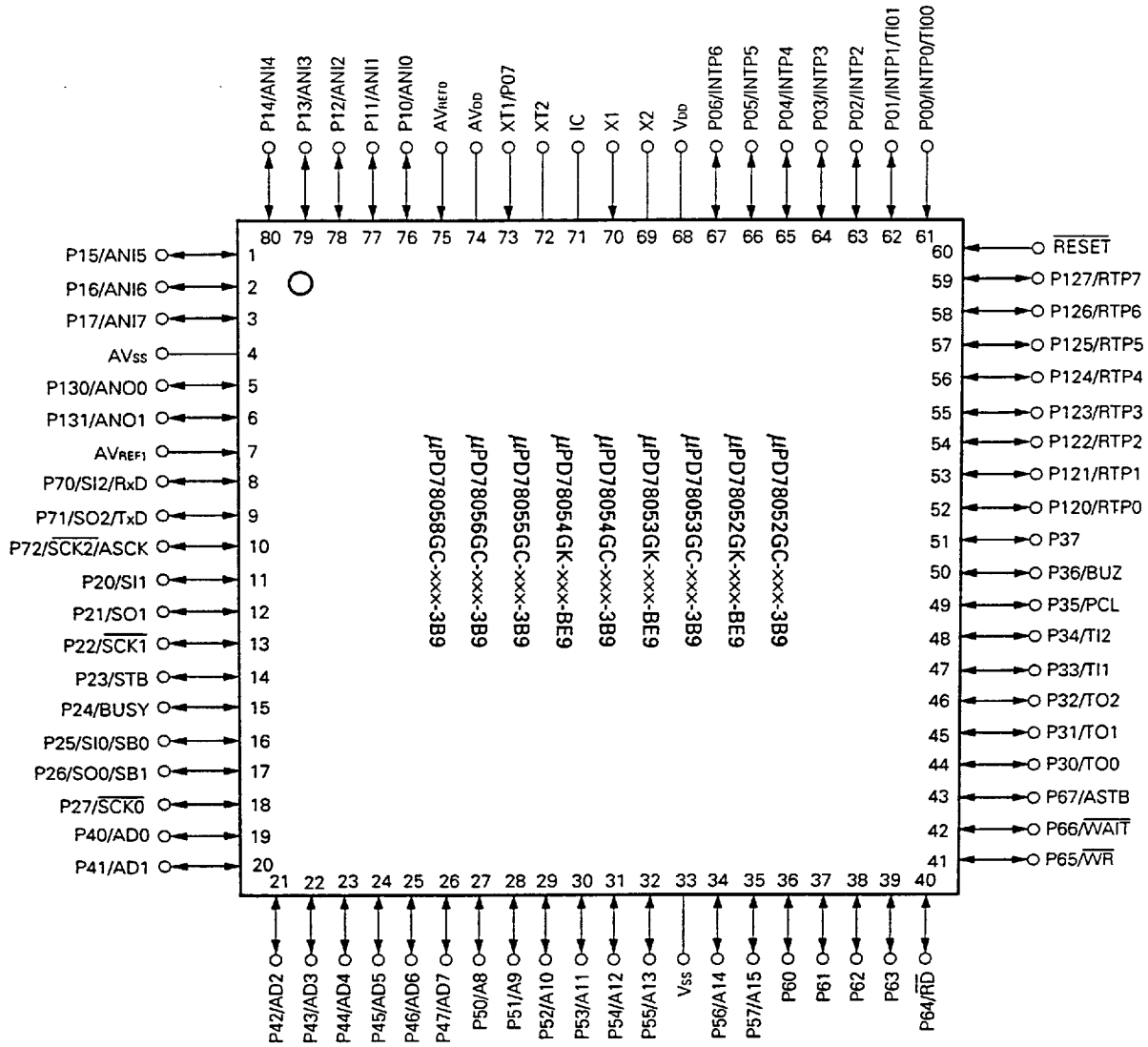
CONTENTS

- 1. PIN CONFIGURATION (TOP VIEW) 5
- 2. BLOCK DIAGRAM 7
- 3. PIN FUNCTIONS 9
 - 3.1 PORT PINS 9
 - 3.2 OTHER PINS 11
 - 3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS 13
- 4. MEMORY SPACE 17
- 5. PERIPHERAL HARDWARE FUNCTION FEATURES 19
 - 5.1 PORTS 19
 - 5.2 CLOCK GENERATOR 20
 - 5.3 TIMER/EVENT COUNTER 20
 - 5.4 CLOCK OUTPUT CONTROL CIRCUIT 23
 - 5.5 BUZZER OUTPUT CONTROL CIRCUIT 23
 - 5.6 A/D CONVERTER 24
 - 5.7 D/A CONVERTER 25
 - 5.8 SERIAL INTERFACES 25
 - 5.9 REAL-TIME OUTPUT PORT FUNCTIONS 27
- 6. INTERRUPT FUNCTIONS 28
 - 6.1 INTERRUPT FUNCTIONS 28
 - 6.2 TEST FUNCTIONS 32
- 7. EXTERNAL DEVICE EXPANSION FUNCTIONS 33
- 8. STANDBY FUNCTION 33
- 9. RESET FUNCTION 33
- 10. INSTRUCTION SET 34
- 11. ELECTRICAL SPECIFICATIONS 37
- 12. CHARACTERISTIC CURVS (REFERENCE VALUE) 64 *
- 13. PACKAGE DRAWINGS 66
- 14. RECOMMENDED SOLDERING CONDITIONS 68
- APPENDIX A. DEVELOPMENT TOOLS 70
- APPENDIX B. RELATED DOCUMENTATIONS 72

1. PIN CONFIGURATION (TOP VIEW)

80-pin plastic QFP (14 × 14 mm)

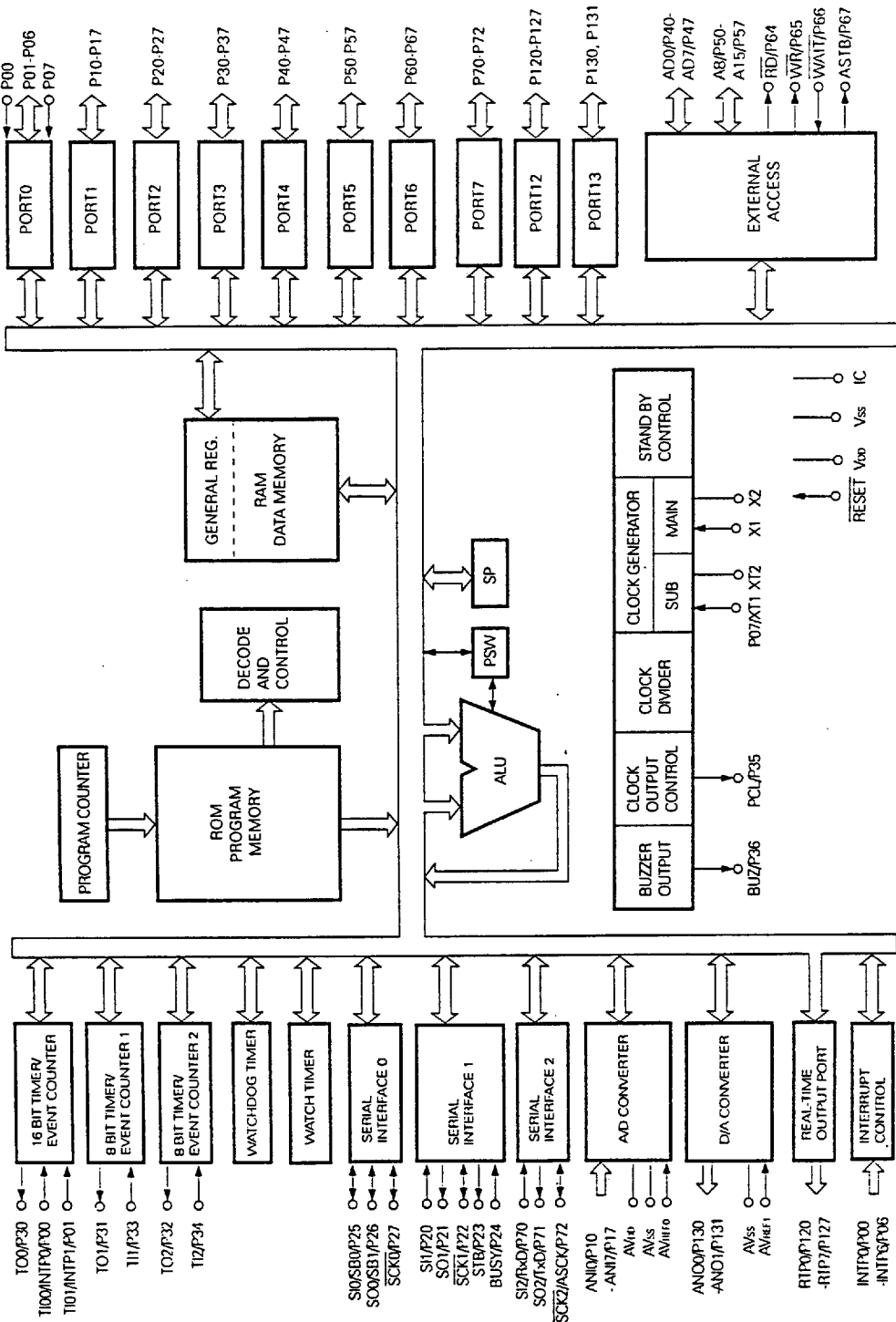
80-pin plastic TQFP (fine pitch) (12 × 12 mm)



- Cautions**
1. IC (Internally Connected) should be connected directly to Vss.
 2. AV_{DD} pin should be connected to V_{DD} pin.
 3. AV_{SS} pin should be connected to V_{SS} pin.

P00 to P07	: Port0	PCL	: Programmable Clock
P10 to P17	: Port1	BUZ	: Buzzer Clock
P20 to P27	: Port2	STB	: Strobe
P30 to P37	: Port3	BUSY	: Busy
P40 to P47	: Port4	AD0 to AD7	: Address/Data Bus
P50 to P57	: Port5	A8 to A15	: Address Bus
P60 to P67	: Port6	\overline{RD}	: Read Strobe
P70 to P72	: Port7	\overline{WR}	: Write Strobe
P120 to P127	: Port12	\overline{WAIT}	: Wait
P130, P131	: Port13	ASTB	: Address Strobe
RTP0 to RTP7	: Real-Time Output Port	X1, X2	: Crystal (Main System Clock)
INTP0 to INTP6	: Interrupt From Peripherals	$\overline{XT1}, \overline{XT2}$: Crystal (Subsystem Clock)
TI00, TI01	: Timer Input	RESET	: Reset
TI1, TI2	: Timer Input	ANI0 to ANI7	: Analog Input
TO0 to TO2	: Timer Output	ANO0, ANO1	: Analog Output
SB0, SB1	: Serial Bus	AV _{DD}	: Analog Power Supply
SI0 to SI2	: Serial Input	AV _{SS}	: Analog Ground
SO0 to SO2	: Serial Output	AV _{REF0,1}	: Analog Reference Voltage
$\overline{SCK0}$ to $\overline{SCK2}$: Serial Clock	V _{DD}	: Power Supply
RxD	: Receive Data	V _{SS}	: Ground
TxD	: Transmit Data	IC	: Internally Connected
ASCK	: Asynchronous Serial Clock		

2. BLOCK DIAGRAM



Remark The internal ROM & RAM capacity depends on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 8-bit I/O port	Input only	Input	INTP0/TI00
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 ^{Note 1}	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software. ^{Note 2}		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	SI1	
P21				SO1	
P22				SCK1	
P23				STB	
P24				BUSY	
P25				SI0/SB0	
P26				SO0/SB1	
P27				SCK0	
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	TO0	
P31				TO1	
P32				TO2	
P33				TI1	
P34				TI2	
P35				PCL	
P36				BUZ	
P37				—	
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

- Notes 1.** When using the P07/XT1 pins as an input port, set 1 in the bit 6 (FRC) of the processor clock control register. On-chip feedback resistor of the subsystem clock oscillator should not be used.
- 2.** When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, use of the pull-up resistor is cancelled automatically.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be connected by software.	Input	\overline{RD}
P65					\overline{WR}
P66					\overline{WAIT}
P67					ASTB
P70	Input/output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	$\overline{SI2/RxD}$	
P71				$\overline{SO2/TxD}$	
P72				$\overline{SCK2/ASCK}$	
P120 to P127	Input/output	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	

3.2 OTHER PINS (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
SCK0	Input /output	Serial interface serial clock input/ output	Input	P27
SCK1				P22
SCK2				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/SCK2
TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1)		P33
TI2		External count clock input to the 8-bit timer (TM2)		P34
TO0	Output	16-bit timer output (dual-function as 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120 to P127
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
RD	Output	External memory read operation strobe signal output.	Input	P64
WR		External memory write operation strobe signal output.		P65

3.2 OTHER PINS (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
WAIT	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AVREF0	Input	A/D converter reference voltage input.	—	—
AVREF1	Input	D/A converter reference voltage input.	—	—
AVDD	—	A/D converter analog power supply. Connected to VDD	—	—
AVSS	—	A/D converter ground potential. Connected to VSS	—	—
RESET	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
VDD	—	Positive power supply.	—	—
VSS	—	Ground potential.	—	—
IC	—	Internal connection. Connect to VSS directly.	—	—

3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used	
P00/INTP0/TI00	2	Input	Connected to Vss.	
P01/INTP1/TI01	8-A	Input/output	Independently connected to Vss through resistor.	
P02/INTP2				
P03/INTP3				
P04/INTP4				
P05/INTP5				
P06/INTP6				
P07/XT1	16	Input	Connected to V _{DD} or Vss.	
P10/ANI0 to P17/ANI7	11	Input/output	Independently connected to V _{DD} or Vss through resistor.	
P20/SI1	8-A			
P21/SO1	5-A			
P22/SCK1	8-A			
P23/STB	5-A			
P24/BUSY	8-A			
P25/SI0/SB0	10-A			
P26/SO0/SB1				
P27/SCK0				
P30/TO0	5-A			
P31/TO1				
P32/TO2				
P33/TI1	8-A			
P34/TI2				
P35/PCL	5-A			
P36/BUZ				
P37				
P40/AD0 to P47/AD7				5-E
P50/A8 to P57/A15	5-A			Independently connected to V _{DD} or Vss through resistor.
P60 to P63	13-B			Independently connected to V _{DD} through resistor.
P64/RD	5-A	Independently connected to V _{DD} or Vss through resistor.		
P65/WR				
P66/WAIT				
P67/ASTB				

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Table 3-1. Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P70/SI2/RxD	8-A	Input/ output	Independently connected to V _{DD} or V _{SS} through resistor.
P71/SO2/TxD	5-A		
P72/ $\overline{\text{SCK2}}$ /ASCK	8-A		
P120/RTP0 to P127/RTP7	5-A	Input/ output	
P130/ANO0 , P131/ANO1	12-A	Input/ output	Independently connected to V _{SS} through resistor.
RESET	2	Input	—
XT2	16	—	Leave open.
AVREF0	—		Connected to V _{SS} .
AVREF1			Connected to V _{DD} .
AV _{DD}			
AV _{SS}			Connected to V _{SS} .
IC			Connected to V _{SS} directly.

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Figure 3-1. Pin Input/Output Circuits (1/2)

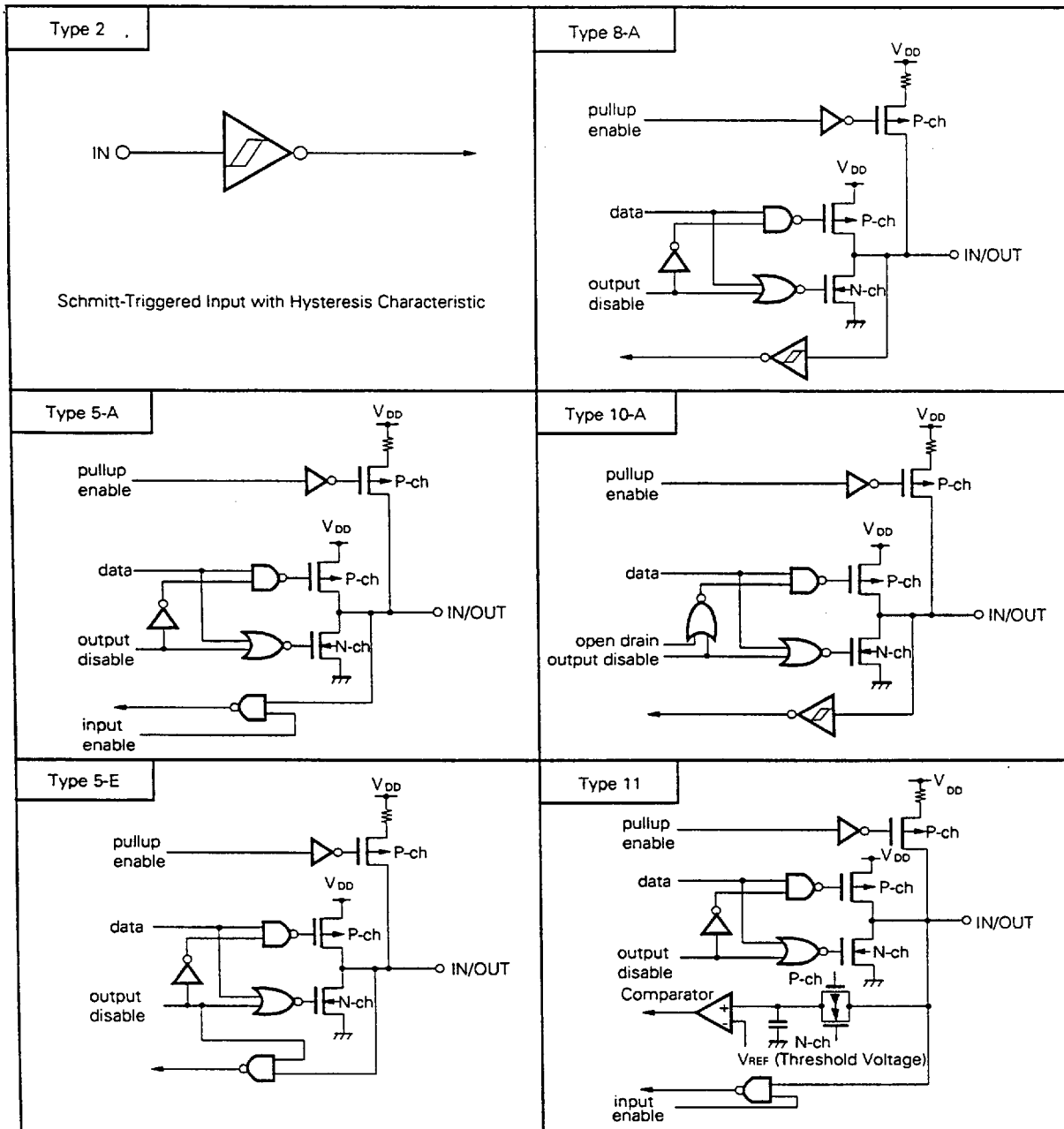
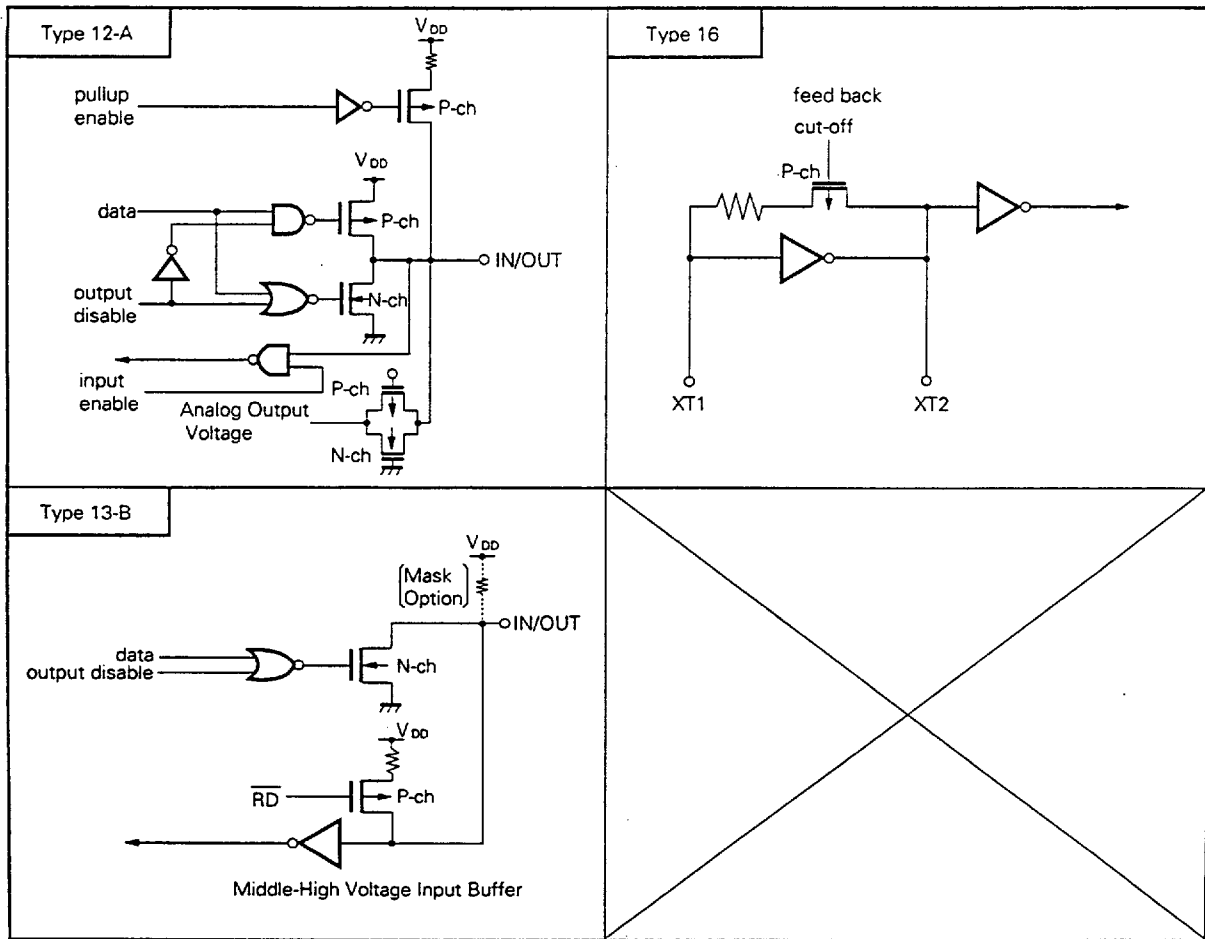


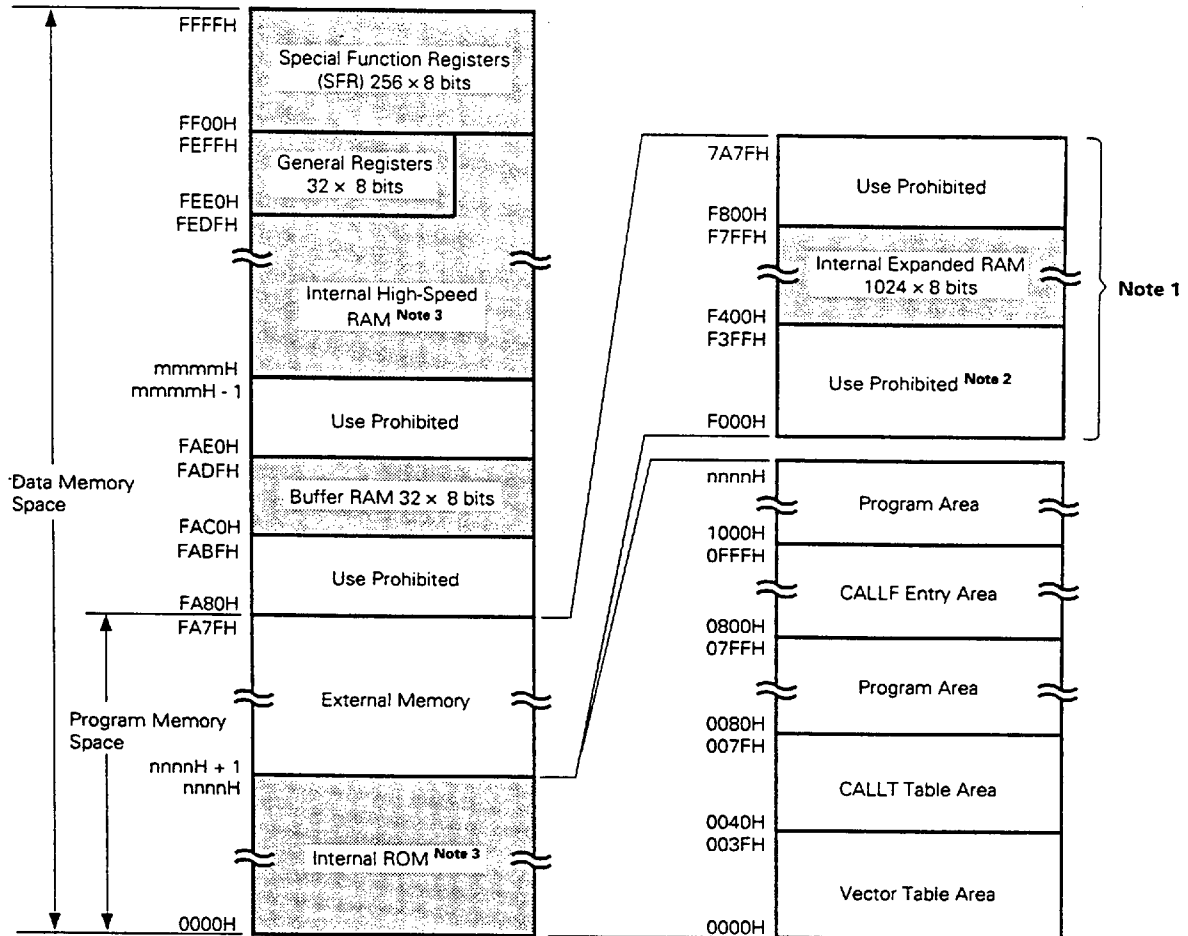
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the μPD78052/78053/78054/78055/78056/78058 memory map.

Figure 4-1. Memory Map



Remark Shaded area indicates internal memory.

Notes 1. μPD78058 only

- When the external device expansion function is used with the μPD78058, set the internal ROM capacity to 56K bytes using the memory size switching register.
- The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the next table).

Relevant Product Name	Internal ROM Last Address nnnnH	Internal RAM First Address mmmmH
μ PD78052	3FFFH	FD00H
μ PD78053	5FFFH	FB00H
μ PD78054	7FFFH	
μ PD78055	9FFFH	
μ PD78056	BFFFH	
μ PD78058	EFFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The following 3 types of I/O ports are available.

- CMOS input (P00, P07) : 2
 - CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 7, port 12, port 13) : 63
 - N-channel open-drain input/output (P60 to P63) : 4
-
- Total : 69

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port pins
	P01 to P06	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable in 8-bit units. When used as input port pins, on-chip pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. LED direct drive capability.
Port 6	P60 to P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be used by mask option. LED direct drive capability.
	P64 to P67	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 7	P70 to P72	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 12	P120 to P127	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 13	P130, P131	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.

5.2 CLOCK GENERATOR

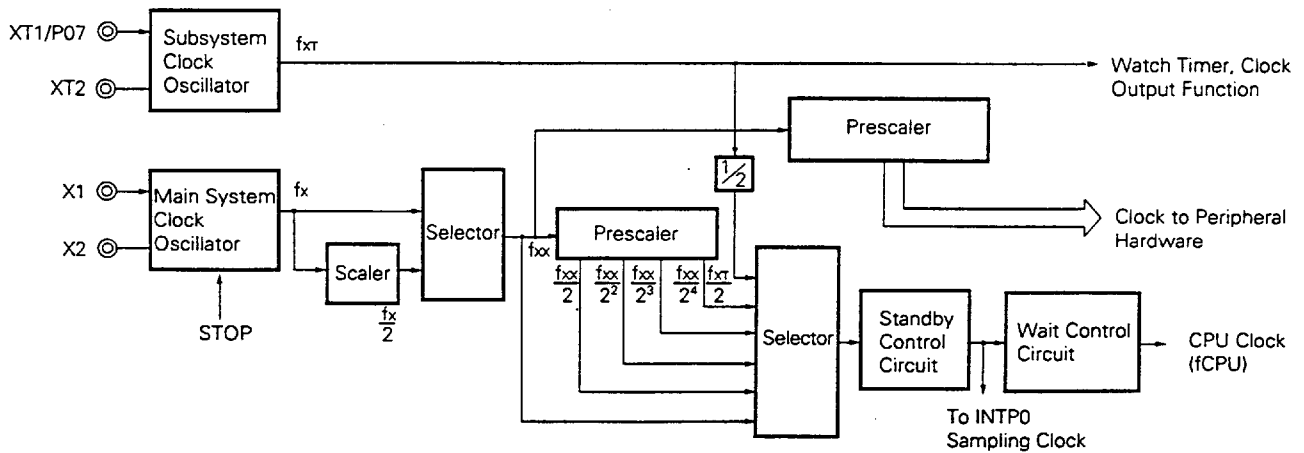
Two types of generators, a main system clock generator and a subsystem clock generator, are available.

The instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: at 5.0 MHz operation)
- 122 μs (subsystem clock: at 32.768 kHz operation)

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Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

The μPD78052/78053/78054/78055/78056/78058 incorporate 5 channels of the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channel
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counter

	16-Bit Timer/Event Counter	8-Bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type				
Interval timer	1 channel	2 channels	1 channel	1 channel
External event counter	1 channel	2 channels	—	—
Function				
Timer output	1 output	2 outputs	—	—
PWM output	1 output	—	—	—
Pulse amplitude measurement	1 input	—	—	—
Square wave output	1 output	2 outputs	—	—
Ono-shot pulse output	1 output	—	—	—
Interrupt request	2	2	2	1

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

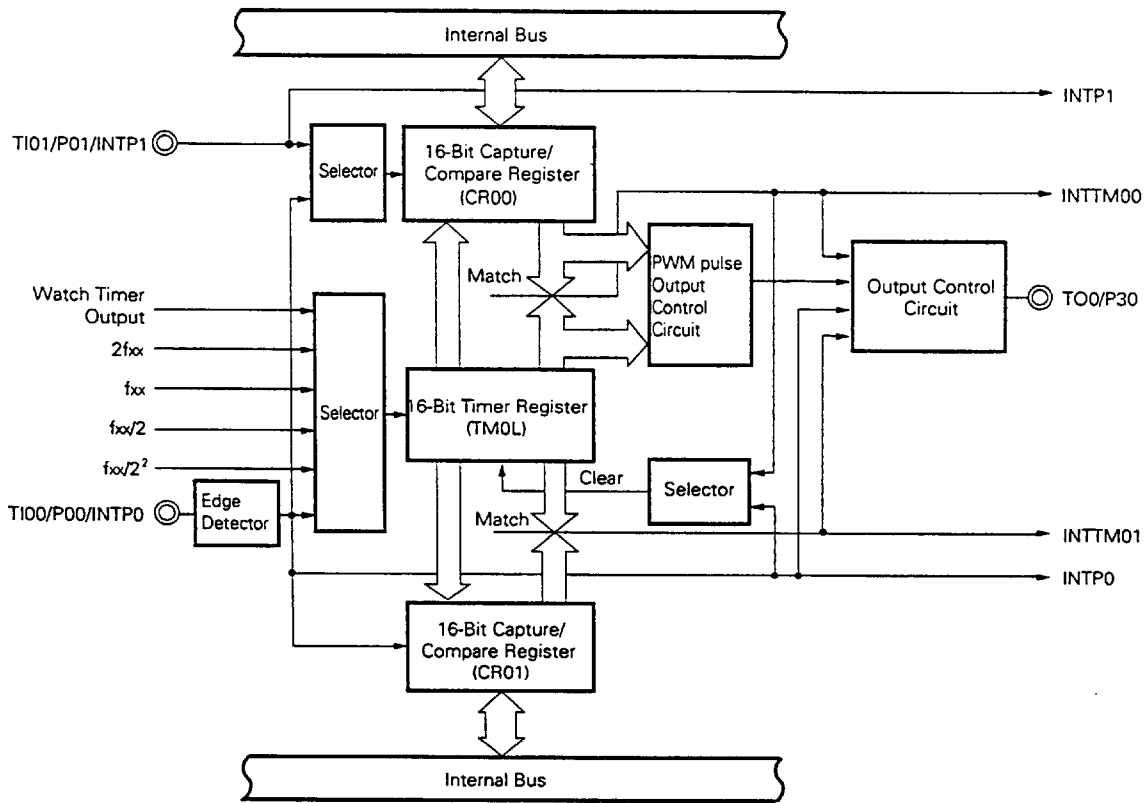


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

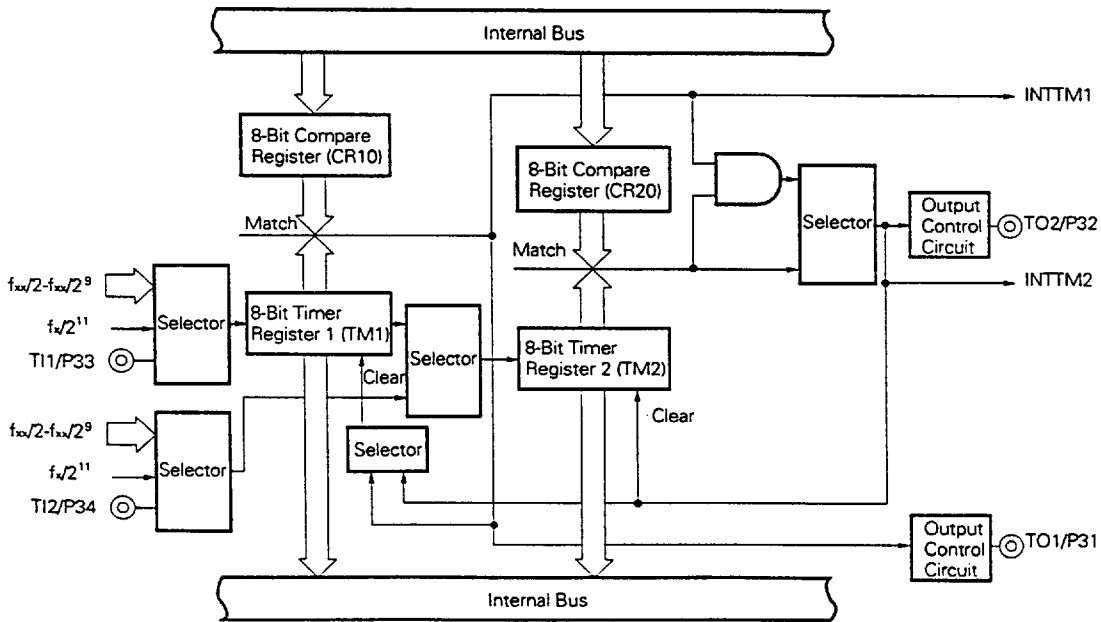


Figure 5-4. Watch Timer Block Diagram

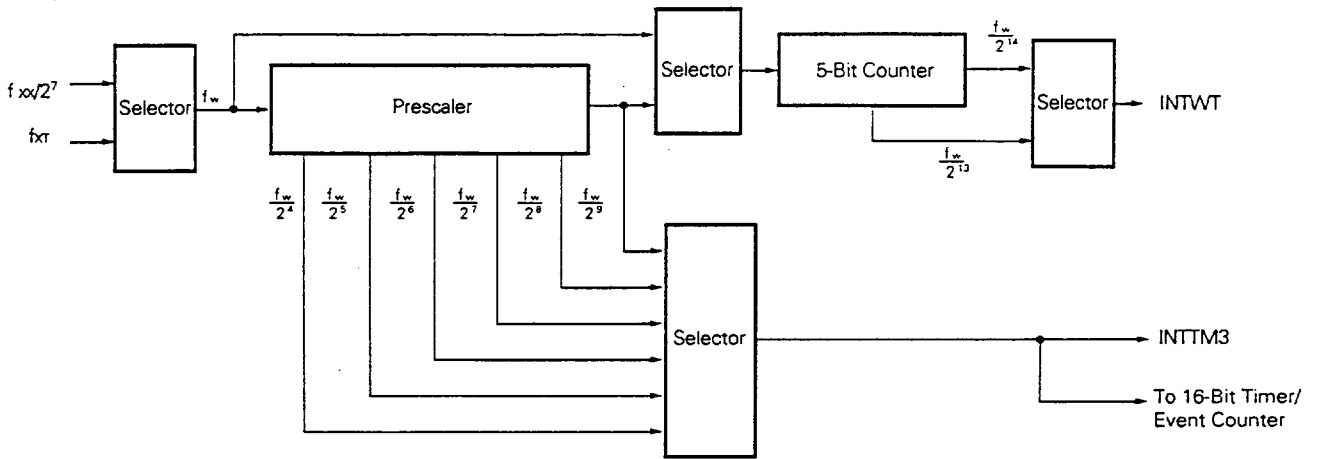
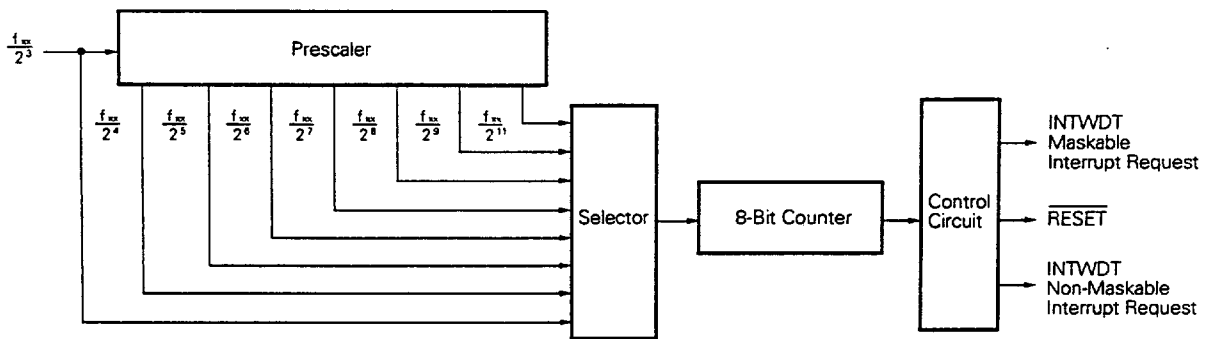


Figure 5-5. Watchdog Timer Block Diagram

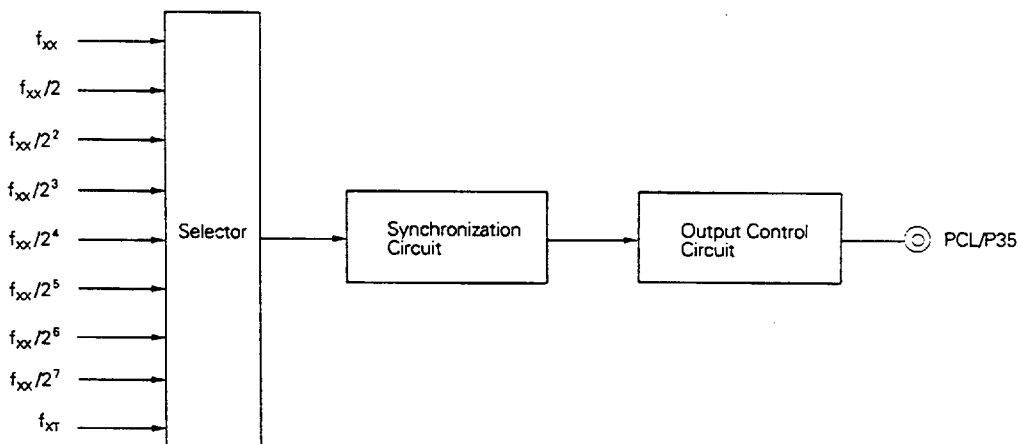


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: at 5.0 MHz operation)
- 32.768 kHz (subsystem clock: at 32.768 kHz operation)

Figure 5-6. Clock Output Control Circuit Configuration

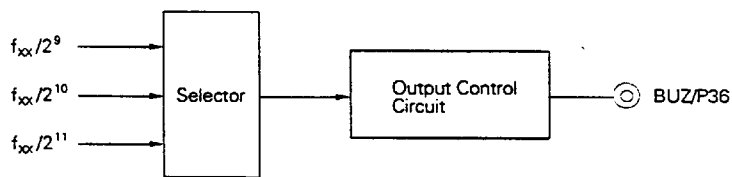


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock: at 5.0 MHz operation)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



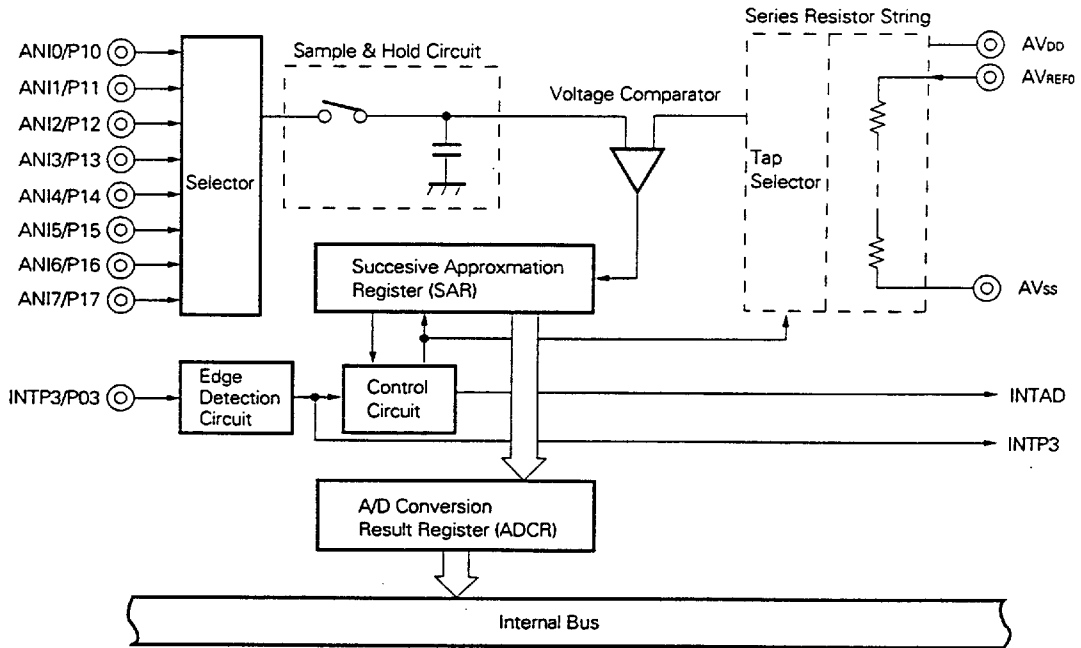
5.6 A/D CONVERTER

An A/D converter of 8-bit resolution × 8 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

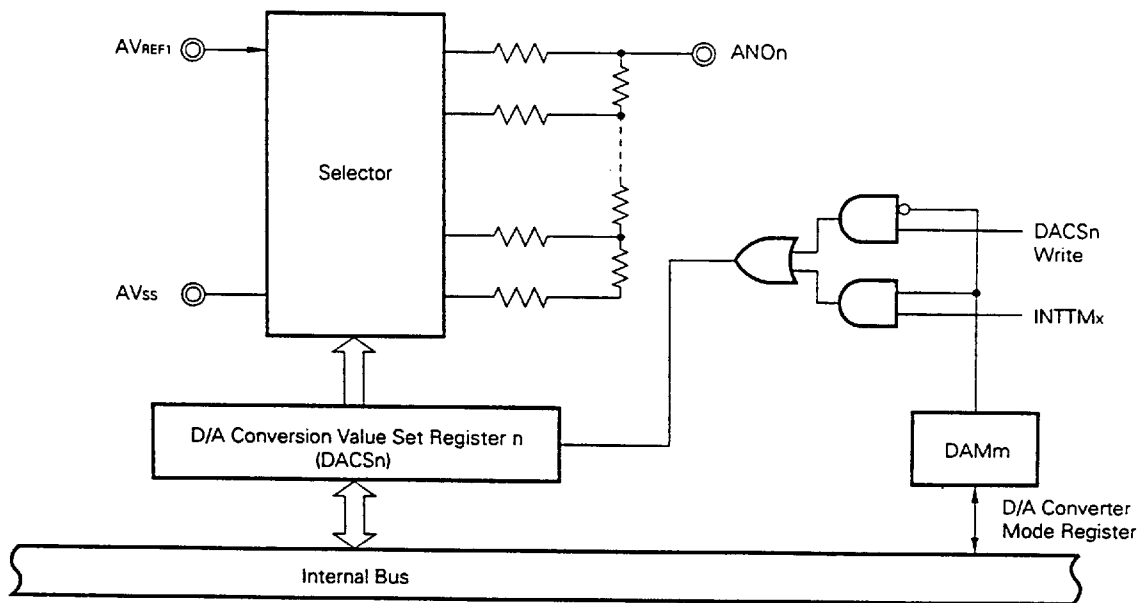
Figure 5-8. A/D Converter Block Diagram



5.7 D/A CONVERTER

A D/A converter of 8-bit resolution × 2 channels is available.
Conversion method is R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1
m = 4, 5
x = 1, 2

5.8 SERIAL INTERFACES

3 channels of the clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-Wired serial I/O mode	○ (MSB/LSB first switchable)	○ (MSB/LSB first switchable)	○ (MSB/LSB first switchable)
3-Wired serial I/O mode with automatic transmission/reception function	—	○ (MSB/LSB first switchable)	—
SBI (serial bus interface) mode	○ (MSB first)	—	—
2-wired serial I/O mode	○ (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	○ (Dedicated baud rate generator incorporated)

Figure 5-10. Serial Interface Channel 0 Block Diagram

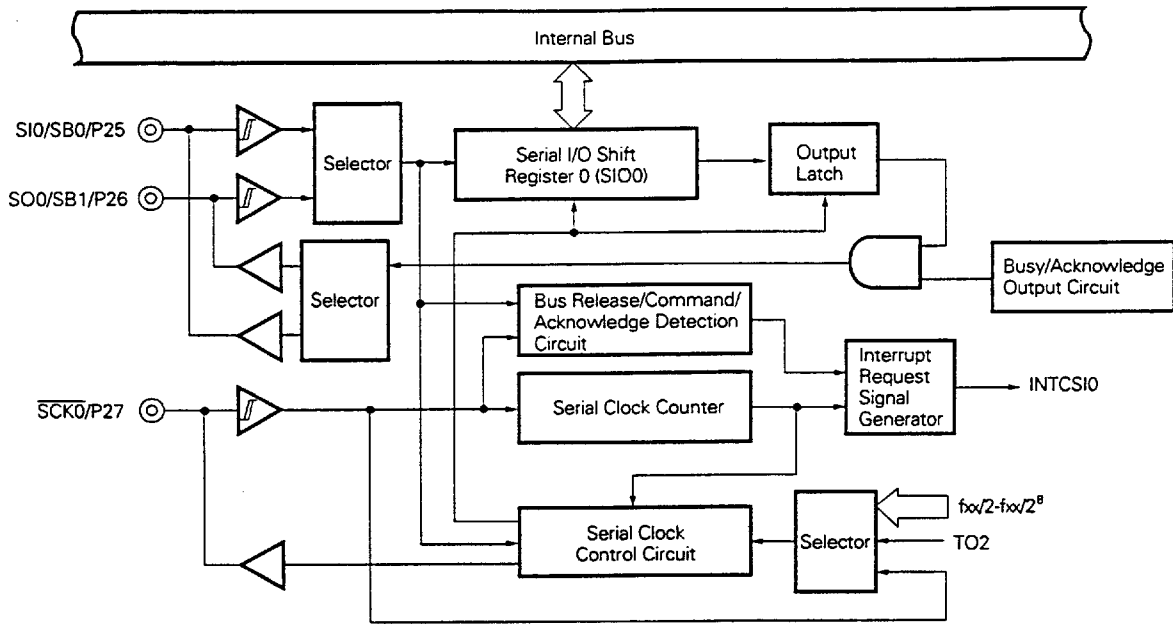


Figure 5-11. Serial Interface Channel 1 Block Diagram

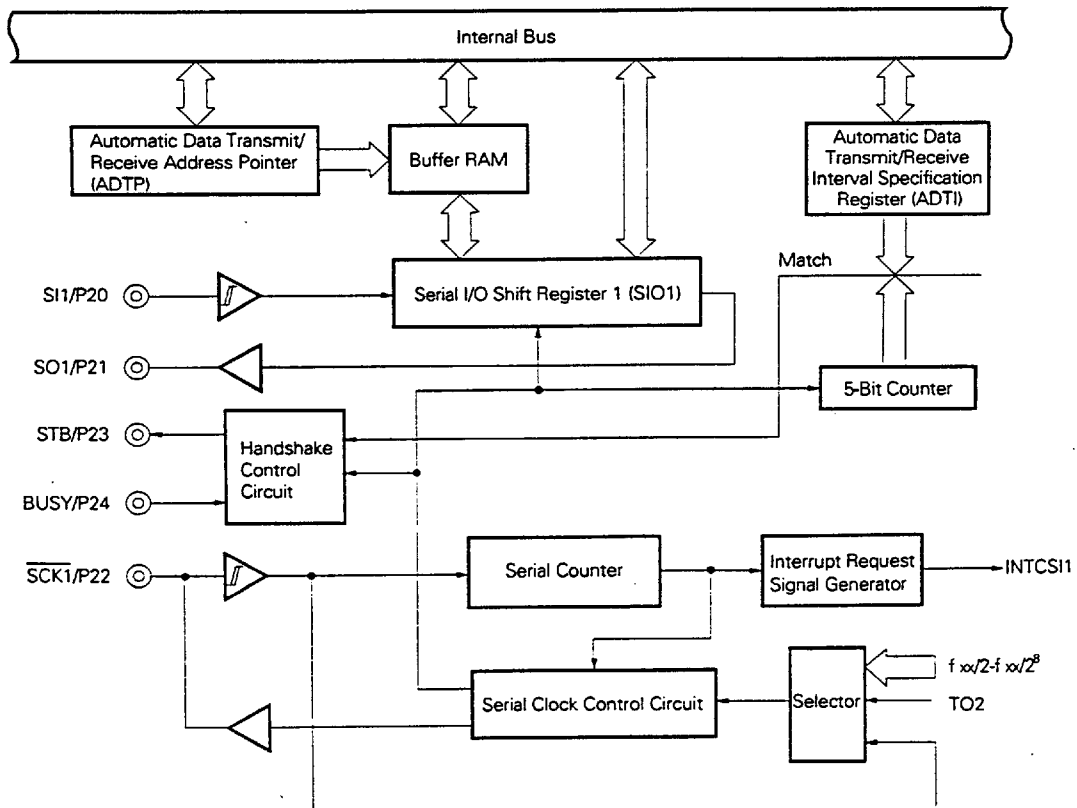
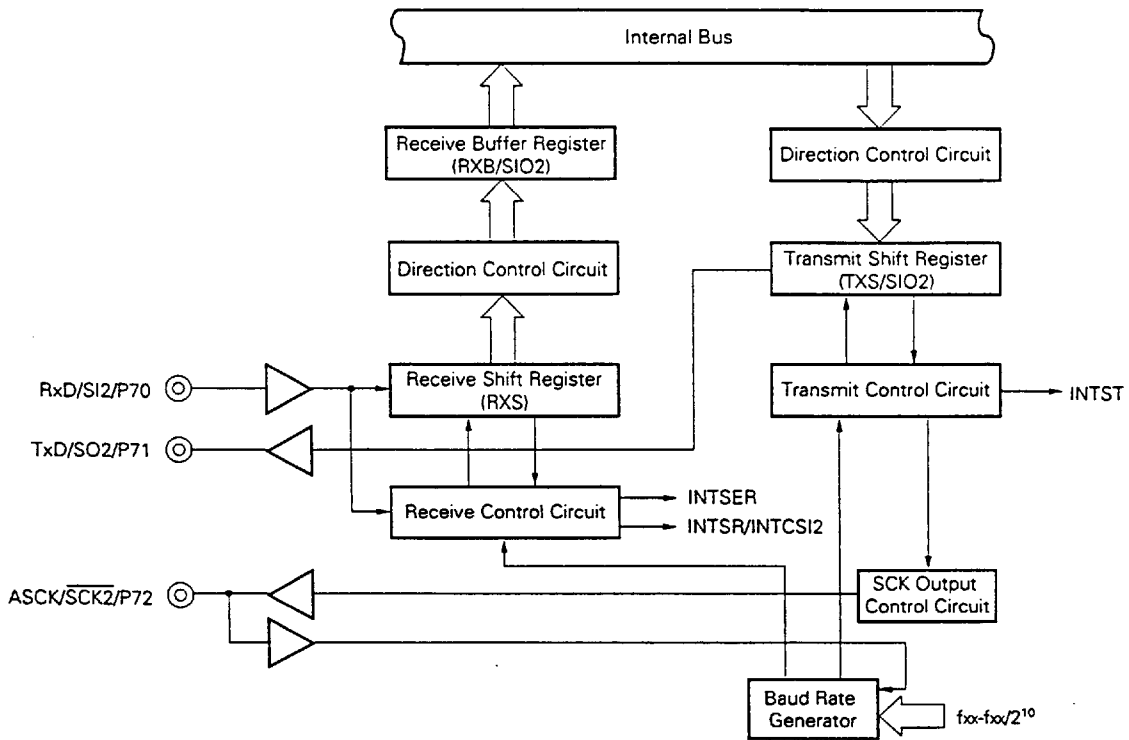


Figure 5-12. Serial Interface Channel 2 Block Diagram

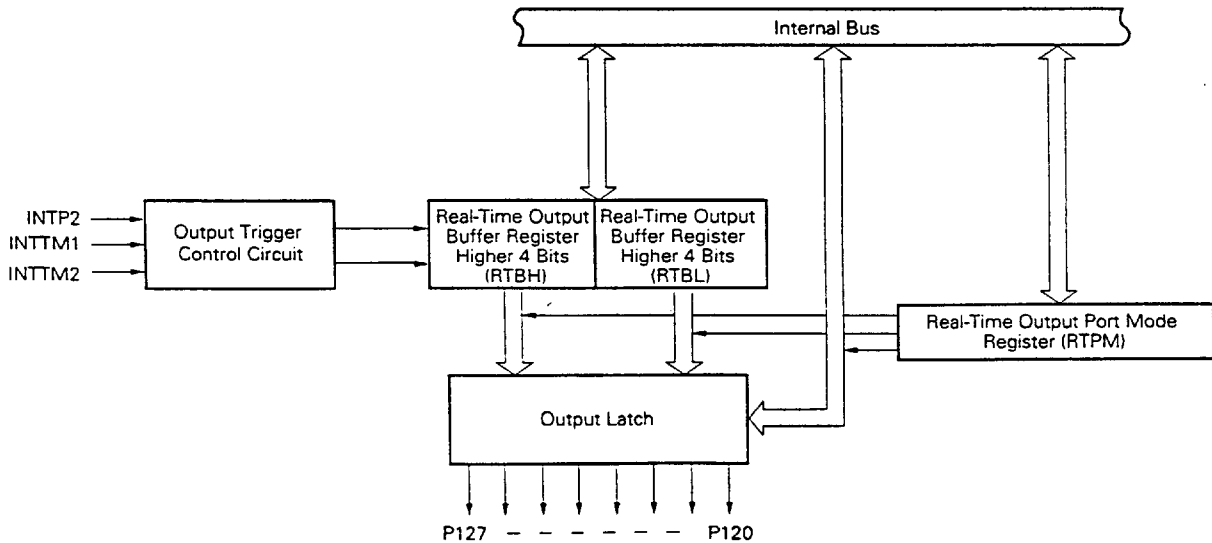


5.9 REAL-TIME OUTPUT PORT FUNCTIONS

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt and external interrupt generation in order to output to off-chip. This is real-time output function. And pins to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motor, etc.

Figure 5-13. Real-Time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are 22 interrupt functions of three different kinds, as shown below.

- Non-maskable interrupt: 1
- Maskable interrupt: 20
- Software interrupt: 1

Table 6-1. Interrupt Source List (1/2)

Interrupt Type	Note 1 Default Priority	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2		
		Name	Trigger					
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	A		
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			External	0006H 0008H 000AH 000CH 000EH 0010H 0012H	B
	1	INTP0	Pin input edge detection	C				
	2	INTP1						
	3	INTP2						
	4	INTP3						
	5	INTP4						
	6	INTP5						
	7	INTP6						
	8	INTCSI0			End of serial interface channel 0 transfer			Internal
	9	INTCSI1	End of serial interface channel 1 transfer					
	10	INTSER	Generation of serial interface chan- nel 2 UART receive error					
	11	INTSR	End of serial interface channel 2 UART reception					
		INTCSI2	End of serial interface channel 2 3- wire transfer					
	12	INTS	End of serial interface channel 2 UART transmission					

- Notes 1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.
2. Basic configuration types A to E correspond to A to E in Fig. 6-1, respectively.

Table 6-1. Interrupt Source List (2/2)

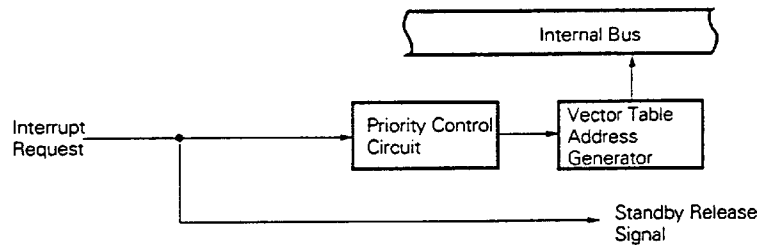
Interrupt Type	Note 1 Default Priority	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
	13	INTTM3	Reference time interval signal from watch timer	Internal	001EH	B
	14	INTTM00	Generation of match signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of match signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of match signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of match signal of 8-bit timer/event counter 2		0026H	
	18	INTAD	End of conversion by A/D converter		0028H	
Software	—	BRK	BRK instruction execution	Internal	003EH	E

Notes 1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.

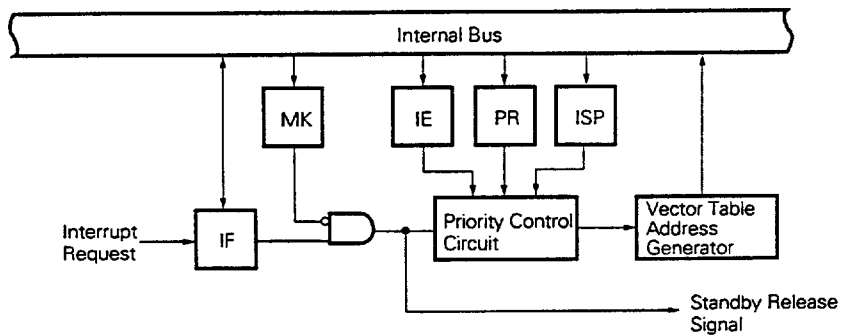
2. Basic configuration types A to E correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Interrupt Function Basic Configuration(1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

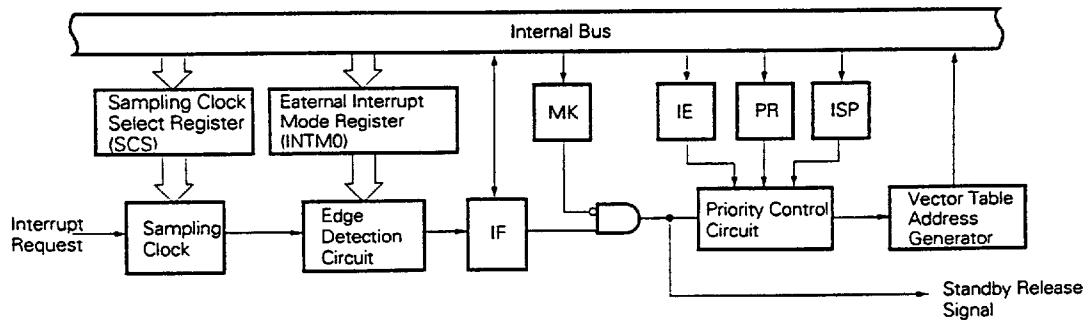
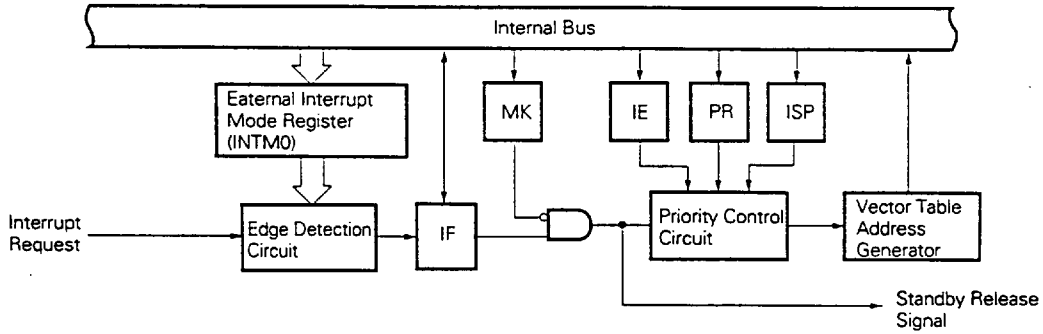
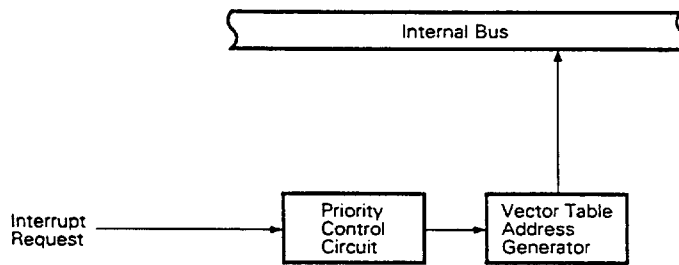


Figure 6-1. Interrupt Function Basic Configuration(2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

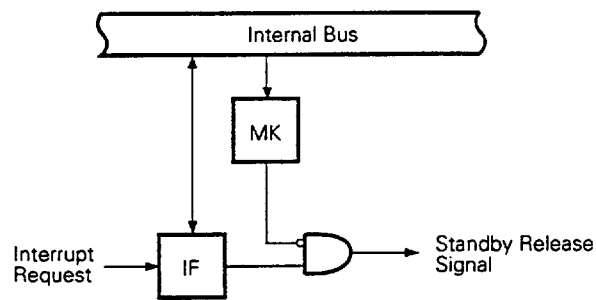
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
 MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

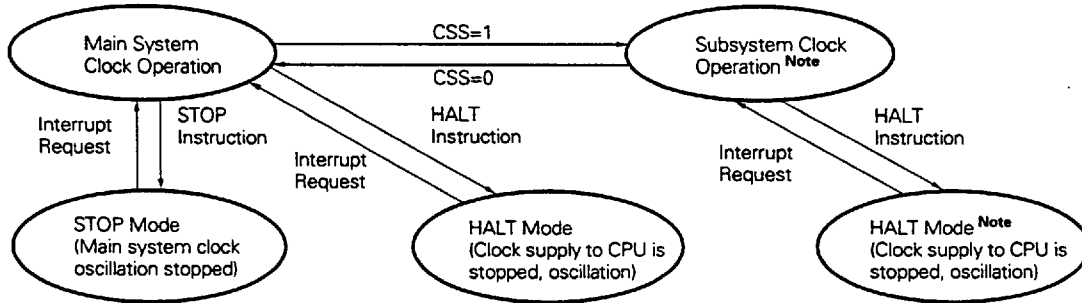
The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operating clock is stopped.
The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Stand-by Function



Note The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by RESET pin
- Internal reset by watchdog time runaway time detection

10. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand First Operand	#byte	A	r Note	sfr	saddr	laddr16	PSW	[DE]	[HL]	[HL + Byte] [HL + B] [HL + C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
laddr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + Byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instruction

MOV, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second instruction First instruction	#word	AX	rp ^{Note}	sfrp	saddrp	laddr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW ^{Note}						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
laddr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second instruction First instruction	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	\$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second instruction First instruction	AX	laddr16	laddr11	[addr5]	\$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit	
Supply voltage	V _{DD}		-0.3 to + 7.0	V	
	AV _{DD}		-0.3 to V _{DD} + 0.3	V	
	AV _{REF0}		-0.3 to V _{DD} + 0.3	V	
	AV _{REF1}		-0.3 to V _{DD} + 0.3	V	
	AV _{SS}		-0.3 to + 0.3	V	
Input voltage	V _{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2 RESET	-0.3 to V _{DD} + 0.3	V	
	V _{I2}	P60 to P63 N-ch Open-drain	-0.3 to +16	V	
Output voltage	V _O		-0.3 to V _{DD} + 0.3	V	
Analog input voltage	V _{AN}	P10 to P17 Analog input pin	AV _{SS} -0.3 to AV _{REF0} + 0.3	V	
Output current high	I _{OH}	1 pin	-10	mA	
		P01 to P06, P30-P37, P56, P57, P60 to P67, P120 to P127 total	-15	mA	
		P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131 total	-15	mA	
Output current low	I _{OL} Note 2	1 pin	Peak value	30	mA
			Effective value	15	mA
		P50 to P55 total	Peak value	100	mA
			Effective value	70	mA
		P56, P57, P60 to P63 total	Peak value	100	mA
			Effective value	70	mA
		P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131 total	Peak value	50	mA
			Effective value	20	mA
P01 to P06, P30 to P37, P64 to P67, P120 to P127 total	Peak value	50	mA		
	Effective value	20	mA		
Operating ambient temperature	T _A		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

Note Effective value should be calculated as follows: [Effective value] = [Peak value] × √duty

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = -40 to 85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f _X) <i>Note 1</i>	V _{DD} = Oscillator voltage range	1.0		5.0	MHz
		Oscillation stabilization time <i>Note 2</i>	After V _{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f _X) <i>Note 1</i>		1.0		5.0	MHz
		Oscillation stabilization time <i>Note 2</i>	V _{DD} = 4.5 to 6.0 V			10 30	ms
External clock		X1 input frequency (f _X) <i>Note 1</i>		1.0		5.0	MHz
		X1 input high/low level width (t _{XH} , t _{XL})		85		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.

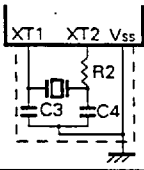
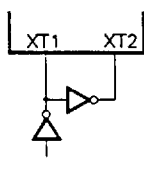
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V_{SS}.
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

SUBSYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f _{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V _{DD} = 4.5 to 6.0 V		1.2	2	s
External clock		XT1 input frequency (f _{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t _{XTH} , t _{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor should be the same as V_{SS}.
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock.

RECOMMENDED OSCILLATION CIRCUIT CONSTANT

(1) μPD78052, 78053, 78054, 78055, 78056

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (TA = -40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSA5.00MG	5.00	30	30	0	2.0	6.0	
	CST5.00MGW	5.00	On chip	On chip	0	2.0	6.0	Capacitor on chip
Kyocera	KBR-5.0MSA	5.00	33	33	0	2.0	6.0	Lead type
	KBR-5.0MKS	5.00	On chip	On chip	0	2.0	6.0	Capacitor on chip, lead type
	KBR-5.0MWS	5.00	On chip	On chip	0	2.0	6.0	Capacitor on chip, lead type
	PBRC 5.00A	5.00	33	33	0	2.0	6.0	Chip type
★ TDK Corp.	CCR4.0MC3	4.00	On chip	On chip	0	2.0	6.0	Capacitor on chip
	CCR5.0MC3	5.00	On chip	On chip	0	2.0	6.0	Capacitor on chip

MAIN SYSTEM CLOCK: CRYSTAL RESONATOR (TA = -10 to + 70 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	SMD-49	3.579545	27	27	1.5	2.0	6.0

★ SUBSYSTEM CLOCK: CRYSTAL RESONATOR (TA = -10 to + 70 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	DT-38 (1TA252E00)	32.768	27	20	330	2.0	6.0

MAIN SYSTEM CLOCK: CRYSTAL RESONATOR (T_A = -40 to + 85 °C)

★

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Kyocera	PBRC4.19A	4.19	33	33	0	2.0	6.0	
	PBRC4.19B	4.19	On chip	On chip	0	2.0	6.0	Capacitor on chip
	KBR-4.19MSA	4.19	33	33	0	2.0	6.0	
	KBR-4.19MKS	4.19	On chip	On chip	0	2.0	6.0	Capacitor on chip
	PBRC4.91A	4.91	33	33	0	2.0	6.0	
	PBRC4.91B	4.91	On chip	On chip	0	2.0	6.0	Capacitor on chip
	KBR-4.91MSA	4.91	33	33	0	2.0	6.0	
	KBR-4.91MKS	4.91	On chip	On chip	0	2.0	6.0	Capacitor on chip

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input capacitance	C _{IN}	f = 1 MHz Measured pins returned to 0 V.			15	pF	
Input/Output	C _{IO}	f = 1 MHz Measured pins returned to 0 V.	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage high	V _{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V _{DD} = 2.7 to 6.0 V	0.7V _{DD}		V _{DD}	V
				0.8V _{DD}		V _{DD}	V
	V _{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 6.0 V	0.8V _{DD}		V _{DD}	V
				0.85V _{DD}		V _{DD}	V
	V _{IH3}	P60 to P63 (N-ch Open-drain)	V _{DD} = 2.7 to 6.0 V	0.7V _{DD}		15	V
				0.8V _{DD}		15	V
	V _{IH4}	X1, X2	V _{DD} = 2.7 to 6.0 V	V _{DD} -0.5		V _{DD}	V
				V _{DD} -0.2		V _{DD}	V
	V _{IH5}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 6.0 V	0.8V _{DD}		V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0.9V _{DD}		V _{DD}	V
2.0 V ≤ V _{DD} < 2.7 V ^{Note}			0.9V _{DD}		V _{DD}	V	
Input voltage low	V _{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V _{DD} = 2.7 to 6.0 V	0		0.3 V _{DD}	V
				0		0.2V _{DD}	V
	V _{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 6.0 V	0		0.2 V _{DD}	V
				0		0.15 V _{DD}	V
	V _{IL3}	P60 to P63	4.5 V ≤ V _{DD} ≤ 6.0 V	0		0.3 V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.2 V _{DD}	V
				0		0.1 V _{DD}	V
	V _{IL4}	X1, X2	V _{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V _{IL5}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 6.0 V	0		0.2 V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.1 V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V ^{Note}	0		0.1 V _{DD}	V
Output voltage high	V _{OH}	V _{DD} = 4.5 to 6.0 V, I _{OH} = -1mA	V _{DD} -1.0			V	
		I _{OH} = -100 μA	V _{DD} -0.5			V	
Output voltage low	V _{OL1}	P50 to P57, P60 to P63	V _{DD} = 4.5 to 6.0 V, I _{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V _{DD} = 4.5 to 6.0 V, I _{OL} = 1.6 mA			0.4	V
	V _{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V _{DD} = 4.5 to 6.0 V, open-drain pulled-up (R = 1 KΩ)			0.2 V _{DD}	V
	V _{OL3}	I _{OL} = 400 μA				0.5	V

Note For use as P07, use an inverter to input the reverse phase of P07 to the XT2 pin.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I _{LIH1}	V _{IN} = V _{DD}	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, <u>RESET</u>			3	μA
	I _{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I _{LIH3}	V _{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I _{LIL1}	V _{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, <u>RESET</u>			-3	μA
	I _{LIL2}		X1, X2, XT1/P07, XT2			-20	μA
	I _{LIL3}		P60 to P63			-3 ^{Note 1}	μA
Output leakage current high	I _{LOH}	V _{OUT} = V _{DD}				3	μA
Output leakage current low	I _{LOL1}	V _{OUT} = 0 V				-3	μA
Mask option pull-up resistor	R ₁	V _{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resistor ^{Note 2}	R ₂	V _{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 V ≤ V _{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V _{DD} < 4.5 V	20		500	kΩ

- Notes** 1. When an input instruction is executed, the low-level input leakage current for P60 to P63 becomes -200 μA (MAX.) only in one clock cycle (no wait). It remains at -3 μA (MAX.) for other than an input instruction.
 2. A software pull-up resistor can be used only in the range of V_{DD} = 2.7 to 6.0 V.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC CHARACTERISTICS (TA = -40 to +85 °C, VDD = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Power supply current Note 5	I _{DD1}	5.0 MHz Crystal oscillation operating mode (f _{xx} = 2.5 MHz) Note 3	V _{DD} = 5.0 V ± 10 % Note 1		4	12	mA
			V _{DD} = 3.0 V ± 10 % Note 2		0.6	1.8	mA
			V _{DD} = 2.2 V ± 10 % Note 2		0.35	1.05	mA
		5.0 MHz Crystal oscillation operating mode (f _{xx} = 5.0 MHz) Note 4	V _{DD} = 5.0 V ± 10 % Note 1		6.5	19.5	mA
			V _{DD} = 3.0 V ± 10 % Note 2		0.8	2.4	mA
	I _{DD2}	5.0 MHz Crystal oscillation HALT mode (f _{xx} = 2.5 MHz) Note 3	V _{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V _{DD} = 3.0 V ± 10 %		0.5	1.5	mA
			V _{DD} = 2.2 V ± 10 %		280	840	μA
		5.0 MHz Crystal oscillation HALT mode (f _{xx} = 5.0 MHz) Note 4	V _{DD} = 5.0 V ± 10 %		1.6	4.8	mA
			V _{DD} = 3.0 V ± 10 %		0.65	1.95	mA
	I _{DD3}	32.768 kHz Crystal oscillation operating mode Note 5	V _{DD} = 5.0 V ± 10 %		60	120	μA
			V _{DD} = 3.0 V ± 10 %		32	64	μA
			V _{DD} = 2.2 V ± 10 %		24	48	μA
I _{DD4}	32.768 kHz Crystal oscillation HALT mode Note 6	V _{DD} = 5.0 V ± 10 %		25	55	μA	
		V _{DD} = 3.0 V ± 10 %		5	15	μA	
		V _{DD} = 2.2 V ± 10 %		2.5	12.5	μA	
I _{DD5}	XT1 = 0 V STOP mode When feedback resistor is used	V _{DD} = 5.0 V ± 10 %		1	30	μA	
		V _{DD} = 3.0 V ± 10 %		0.5	10	μA	
		V _{DD} = 2.2 V ± 10 %		0.3	10	μA	
I _{DD6}	XT1 = 0 V STOP mode When feedback resistor is unused	V _{DD} = 5.0 V ± 10 %		0.1	30	μA	
		V _{DD} = 3.0 V ± 10 %		0.05	10	μA	
		V _{DD} = 2.2 V ± 10 %		0.05	10	μA	

- Notes**
1. Operating in high-speed mode (when set the processor clock control register to 00H).
 2. Operating in low-speed mode (when set the processor clock control register to 04H).
 3. Operation with f_{xx} = f_x/2 (when oscillation mode selection register is set to 00H)
 4. Operation with f_{xx} = f_x (when oscillation mode selection register is set to 01H)
 5. The AV_{REF0}, AV_{REF1}, AV_{DD} currents and port current (including a current flowing in the on-chip pull-up resistor) are not included.
 6. When the main system clock is halted

- Remarks**
1. f_{xx}: Main system clock frequency (f_x or f_x/2)
 2. f_x: Main system clock oscillator frequency

AC CHARACTERISTICS

(1) BASIC OPERATION (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

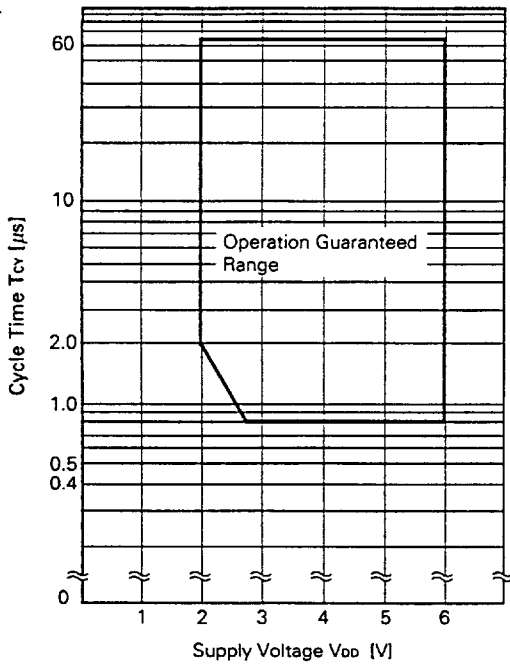
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (Min. instruction execution time)	T _{cy}	Operating on main system clock	f _{xx} = f _x /2 ^{Note 1}	V _{DD} = 2.7 to 6.0 V	0.8	64	μs
					2.2	64	μs
			f _{xx} = f _x ^{Note 2}	4.5 V ≤ V _{DD} ≤ 6.0 V	0.4	32	μs
				2.7 V ≤ V _{DD} < 4.5 V	0.8	32	μs
		Operating on sub systema clock		40	122	125	μs
TI00, TI01, TI1, TI2 input frequency	f _{ri}	V _{DD} = 4.5 to 6.0 V		0	4	MHz	
				0	275	kHz	
TI00 input high/ low level width	t _{TIH} , t _{TIL}		8/f _{sam} ^{Note 3}			μs	
TI01, TI1, TI2 input high/ low-level width	t _{TIH} , t _{TIL}	V _{DD} = 4.5 to 6.0 V		100		ns	
				1.8		μs	
Interrupt input high/low-level width	t _{INTH} , t _{INTL}	INTP0		8/f _{sam} ^{Note 3}		μs	
		INTP1 to INTP6, KR0 to KR7	V _{DD} = 2.7 to 6.0 V		10		μs
					20		μs
RESET low level width	t _{ASL}	V _{DD} = 2.7 to 6.0 V		10		μs	
				20		μs	

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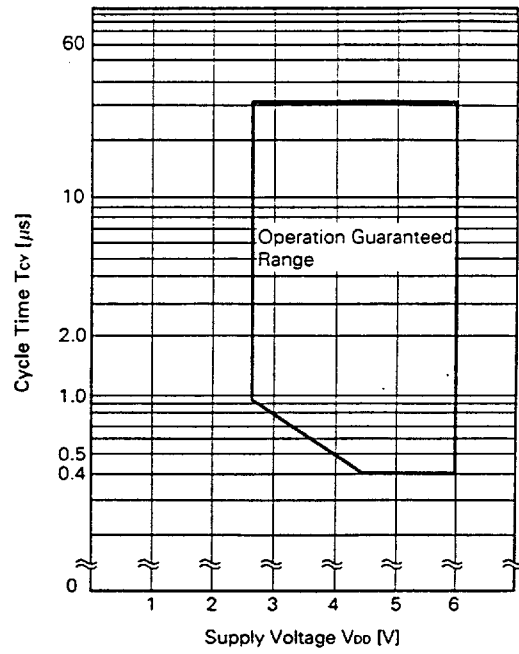
- Notes**
1. When oscillation mode selection register is set to 00H
 2. When oscillation mode selection register is set to 01H
 3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of f_{sam} is possible between f_{xx}/2^N, f_{xx}/32, f_{xx}/64 and f_{xx}/128 (when N= 0 to 4).

- Remarks**
1. f_{xx}: Main system clock frequency (f_x or f_x/2)
 2. f_x: Main system clock oscillation frequency

T_{cy} vs V_{DD} (At f_{xx} = f_x/2 main system clock operation)



T_{cy} vs V_{DD} (At f_{xx} = f_x main system clock operation)



(2) READ/WRITE OPERATION

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to + 85 °C, V_{DD} = 4.5 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}		0.85t _{cy} - 50		ns
Address setup time	t _{ADS}		0.85t _{cy} - 50		ns
Address hold time	t _{ADH}		50		ns
Data input time from address	t _{ADD1}			(2.85+2n)t _{cy} -80	ns
	t _{ADD2}			(4+2n)t _{cy} -100	ns
Data input time from RD↓	t _{RDD1}			(2+2n)t _{cy} -100	ns
	t _{RDD2}			(2.85+2n)t _{cy} -100	ns
Read data hold time	t _{RDH}		0		ns
RD low-level width	t _{RDL1}		(2+2n)t _{cy} -60		ns
	t _{RDL2}		(2.85+2n)t _{cy} -60		ns
WAIT↓ input time from RD↓	t _{RWWT1}			0.85t _{cy} -50	ns
	t _{RWWT2}			2t _{cy} -60	ns
WAIT↓ input time from WR↓	t _{WRWT}			2t _{cy} -60	ns
WAIT low-level width	t _{WTL}		(1.15+2n)t _{cy}	(2+2n)t _{cy}	ns
Write data setup time	t _{WDS}		(2.85+2n)t _{cy} -100		ns
Write data hold time	t _{WDH}		20		ns
WR low-level width	t _{WRL}		(2.85+2n)t _{cy} -60		ns
RD↓ delay time from ASTB↓	t _{ASTRD}		25		ns
WR↓ delay time from ASTB↓	t _{ASTWR}		0.85t _{cy} + 20		ns
ASTB↑ delay time from RD↑ in external fetch	t _{RDAST}		0.85t _{cy} - 10	1.15t _{cy} + 20	ns
Address hold time from RD↑ in external fetch	t _{RDADH}		0.85t _{cy} - 50	1.15t _{cy} + 50	ns
Write data output time from RD↑	t _{RDWD}		40		ns
Write data output time from WR↓	t _{WRWD}		0	50	ns
Address hold time from WR↑	t _{WRADH}		0.85t _{cy}	1.15t _{cy} + 40	ns
RD↑ delay time from WAIT↑	t _{WTRD}		1.15t _{cy} + 40	3.15t _{cy} + 40	ns
WR↑ delay time from WAIT↑	t _{WTWR}		1.15t _{cy} + 30	3.15t _{cy} + 30	ns

- Remarks
1. MCS: Oscillation mode selection register bit 0
 2. PCC2 to PCC0: Processor clock control register bit 2 to bit 0
 3. t_{cy} = T_{cy}/4
 4. n indicates number of waits.

(b) When except MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to + 85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}	V _{DD} = 2.7 to 6.0 V	t _{cy} - 80		ns
			t _{cy} - 150		ns
Address setup time	t _{ADS}	V _{DD} = 2.7 to 6.0 V	t _{cy} - 80		ns
			t _{cy} - 150		ns
Address hold time	t _{ADH}	V _{DD} = 2.7 to 6.0 V	0.4t _{cy} - 10		ns
			0.37t _{cy} - 40		ns
Data input time from address	t _{ADD1}	V _{DD} = 2.7 to 6.0 V		(3+2n)t _{cy} -160	ns
				(3+2n)t _{cy} -320	ns
	t _{ADD2}	V _{DD} = 2.7 to 6.0 V		(4+2n)t _{cy} -200	ns
				(4+2n)t _{cy} -300	ns
Data input time from $\overline{RD}\downarrow$	t _{RDD1}	V _{DD} = 2.7 to 6.0 V		(1.4+2n)t _{cy} -70	ns
				(1.37+2n)t _{cy} -120	ns
	t _{RDD2}	V _{DD} = 2.7 to 6.0 V		(2.4+2n)t _{cy} -70	ns
				(2.37+2n)t _{cy} -120	ns
Read data hold time	t _{RDH}		0		ns
\overline{RD} low-level width	t _{RDL1}	V _{DD} = 2.7 to 6.0 V	(1.4+2n)t _{cy} -20		ns
			(1.37+2n)t _{cy} -20		ns
	t _{RDL2}	V _{DD} = 2.7 to 6.0 V	(2.4+2n)t _{cy} -20		ns
			(2.37+2n)t _{cy} -20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t _{RDWT1}	V _{DD} = 2.7 to 6.0 V		t _{cy} -100	ns
				t _{cy} -200	ns
	t _{RDWT2}	V _{DD} = 2.7 to 6.0 V		2t _{cy} -100	ns
				2t _{cy} -200	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t _{WRWT}	V _{DD} = 2.7 to 6.0 V		2t _{cy} -100	ns
				2t _{cy} -200	ns
\overline{WAIT} low-level width	t _{WTL}		(1+2n)t _{cy}	(2+2n)t _{cy}	ns
Write data setup time	t _{WDS}	V _{DD} = 2.7 to 6.0 V	(2.4+2n)t _{cy} -60		ns
			(2.37+2n)t _{cy} -100		ns
Write data hold time	t _{WDH}		20		ns
\overline{WR} low-level width	t _{WRL}	V _{DD} = 2.7 to 6.0 V	(2.4+2n)t _{cy} -20		ns
			(2.37+2n)t _{cy} -20		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t _{ASTRD}	V _{DD} = 2.7 to 6.0 V	0.4t _{cy} - 30		ns
			0.37t _{cy} - 50		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t _{ASTWR}	V _{DD} = 2.7 to 6.0 V	1.4t _{cy} - 30		ns
			1.37t _{cy} - 50		ns

- Remarks
1. MCS: Oscillation mode selection register bit 0
 2. PCC2 to PCC0: Processor clock control register bit 2 to bit 0
 3. t_{cy} = T_{cy}/4
 4. n indicates number of waits.

(b) When except MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to + 85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB↑ delay time from RD↑ in external fetch	tRDAST		t _{cy} - 10	t _{cy} + 20	ns
Address hold time from RD↑ in external fetch	tRDADH		t _{cy} - 50	t _{cy} + 50	ns
Write data output time from RD↑	tRDWD	V _{DD} = 2.7 to 6.0 V	0.4t _{cy} - 20		ns
			0.37t _{cy} - 40		ns
Write data output time from WR↓	tWRWD	V _{DD} = 2.7 to 6.0 V	0	60	ns
			0	120	ns
Address hold time from WR↑	tWRADH	V _{DD} = 2.7 to 6.0 V	t _{cy}	t _{cy} + 60	ns
			t _{cy}	t _{cy} + 120	ns
RD↑ delay time from WAIT↑	tWTRD	V _{DD} = 2.7 to 6.0 V	0.6t _{cy} + 180	2.6t _{cy} + 180	ns
			0.63t _{cy} + 350	2.63t _{cy} + 350	ns
WR↑ delay time from WAIT↑	tWTWR	V _{DD} = 2.7 to 6.0 V	0.6t _{cy} + 120	2.8t _{cy} + 120	ns
			0.63t _{cy} + 240	2.63t _{cy} + 240	ns

- Remarks**
1. MCS: Oscillation mode selection register bit 0
 2. PCC2 to PCC0: Processor clock control register bit 2 to bit 0
 3. t_{cy} = T_{cy}/4
 4. n indicates number of waits.

(3) SERIAL INTERFACE (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(a) 3-wire serial I/O mode ($\overline{\text{SCK}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkcy1	4.5 V ≤ V _{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{\text{SCK}}$ high/low-level width	tkH1, tkL1	V _{DD} = 4.5 to 6.0 V	tkcy1/2-50			ns
			tkcy1/2-100			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$)	tsik1	4.5 V ≤ V _{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V _{DD} < 4.5 V	150			ns
			300			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$)	tkS11		400			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	tkSO1	C = 100 pF ^{Note}			300	ns

Note C is the load capacitance of SO output line.

(b) 3-wire serial I/O mode ($\overline{\text{SCK}}$... Internal clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkcy2	4.5 V ≤ V _{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{\text{SCK}}$ high/low-level width	tkH2, tkL2	4.5 V ≤ V _{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V _{DD} < 4.5 V	800			ns
			1600			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$)	tsik2		100			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$)	tkS12		400			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	tkSO2	C = 100 pF ^{Note}			300	ns
$\overline{\text{SCK}}$ rise, fall time	tr2, tf2	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of SO output line.

(c) SBI mode ($\overline{\text{SCK}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkcy3	V _{DD} = 4.5 to 6.0 V	800			ns
			3200			ns
$\overline{\text{SCK}}$ high/low-level width	tkH3 tkL3	V _{DD} = 4.5 to 6.0 V	tkcy3/2-50			ns
			tkcy3/2-150			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$)	tsik3	V _{DD} = 4.5 to 6.0 V	100			ns
			300			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}\downarrow$)	tksi3		tkcy3/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkso3	R = 1 kΩ , C = 100 pF <small>Note</small>	V _{DD} = 4.5 to 6.0 V	0	250	ns
				0	1000	ns
SB0, SB1↓ from $\overline{\text{SCK}}\uparrow$	tkse		tkcy3			ns
$\overline{\text{SCK}}\downarrow$ from SB0, SB1↓	tsbk		tkcy3			ns
SB0, SB1 high-level width	tsbh		tkcy3			ns
SB0, SB1 low-level width	tsbl		tkcy3			ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(d) SBI mode ($\overline{\text{SCK}}$... Internal clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK}}$ cycle time	tkcy4	V _{DD} = 4.5 to 6.0 V	800			ns	
			3200			ns	
$\overline{\text{SCK}}$ high/low-level width	tkH4 tkL4	V _{DD} = 4.5 to 6.0 V	400			ns	
			1600			ns	
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$)	tsik4	V _{DD} = 4.5 to 6.0 V	100			ns	
			300			ns	
SB0, SB1 hold time (from $\overline{\text{SCK}}\uparrow$)	tkSH4		tkcy4/2			ns	
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkSO4	R = 1 kΩ , C = 100 pF Note	V _{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK}}\uparrow$	tkSB		tkcy4			ns	
$\overline{\text{SCK}}\downarrow$ from SB0, SB1↓	tsBK		tkcy4			ns	
SB0, SB1 high-level width	tsBH		tkcy4			ns	
SB0, SB1 low-level width	tsBL		tkcy4			ns	
$\overline{\text{SCK}}$ rise, fall time	tr4, tf4	When using external device expansion function			160	ns	
		When not using external device expansion function			1000	ns	

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Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(e) 2-wire serial I/O mode ($\overline{\text{SCK}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkcys	R = 1 kΩ, C = 100 pF Note	V _{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{\text{SCK}}$ high-level width	tkH5		V _{DD} = 2.7 to 6.0 V	tkcys/2-160			ns
				tkcys/2-190			ns
$\overline{\text{SCK}}$ low-level width	tkL5		V _{DD} = 4.5 to 6.0 V	tkcys/2-50			ns
				tkcys/2-100			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$)	tSIK5	4.5 V ≤ V _{DD} ≤ 6.0 V	300			ns	
		2.7 V ≤ V _{DD} < 4.5 V	350			ns	
			400			ns	
SB0, SB1 hold time (from $\overline{\text{SCK}}\uparrow$)	tkSIS		600			ns	
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkSOS		0		300	ns	

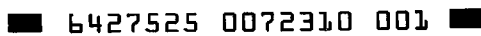
Note R and C are the load resistors and load capacitance of the $\overline{\text{SCK}}$, SB0 and SB1 output line.

(f) 2-wire serial I/O mode ($\overline{\text{SCK}}$... Internal clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkcys	V _{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{\text{SCK}}$ high-level width	tkH6	V _{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{\text{SCK}}$ low-level width	tkL6	V _{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$)	tSIK6			100			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}\uparrow$)	tkSIS			tkcys/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkSOS	R = 1 kΩ, C = 100 pF Note	V _{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{\text{SCK}}$ rise, fall time	tr6, tf6	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistors and load capacitance of the $\overline{\text{SCK}}$, SB0 and SB1 output line.

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(g) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK}}$...Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK}}$ high/low-level width	t_{KH7}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	$t_{\text{KCY7}}/2-50$			ns
	t_{KL7}		$t_{\text{KCY7}}/2-100$			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$)	t_{SIK7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
			300			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$)	t_{KSI7}		400			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	t_{KSO7}	$C = 100 \text{ pF}$ Note			300	ns
STB \uparrow from $\overline{\text{SCK}}\uparrow$	t_{SBD}		$t_{\text{KCY7}}/2-100$		$t_{\text{KCY7}}/2+100$	ns
Strobe signal high-level width	t_{SBW}	$V_{\text{DD}} = 2.7 \text{ to } 6.0\text{V}$	$t_{\text{KCY7}}-30$		$t_{\text{KCY7}}+30$	ns
			$t_{\text{KCY7}}-60$		$t_{\text{KCY7}}+60$	ns
Busy signal setup time (to busy signal detection timing)	t_{EVS}		100			ns
Busy signal hold time (from busy signal detection timing)		$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
			200			ns
$\overline{\text{SCK}}\downarrow$ from busy inactive	t_{SPS}				$2t_{\text{KCY7}}$	ns

Note C is the load capacitance of the SO output line.

(h) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK}}$...External clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK}}$ high/low-level width	t_{KH8} t_{KL8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	400			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
			1600			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$)	t_{SIK8}		100			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$)	t_{KIS8}		400			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	t_{KSO8}	$C = 100 \text{ pF}$ Note			300	ns
$\overline{\text{SCK}}$ rise, fall time	$t_{\text{R8}}, t_{\text{F8}}$	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO output line.

(i) UART mode (Dedicated baud rate generator output)

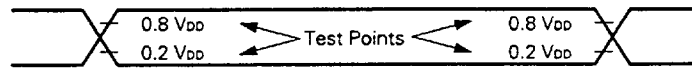
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V _{DD} ≤ 6.0 V			78125	bps
		2.7 V ≤ V _{DD} < 4.5 V			39063	bps
					19531	bps

(j) UART mode (External clock input)

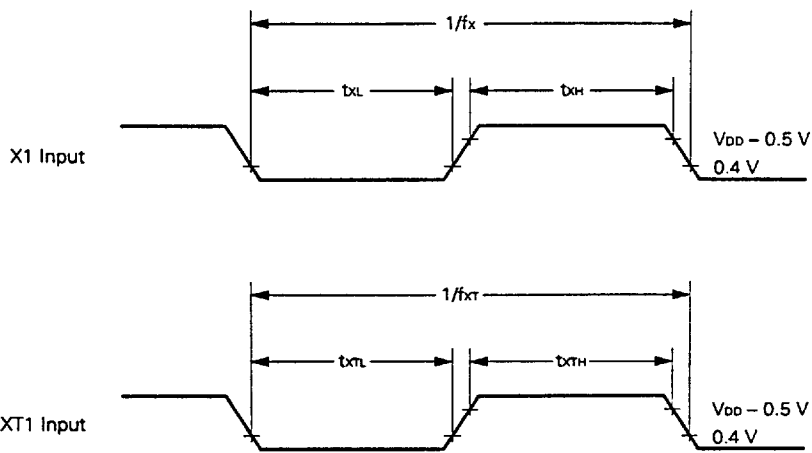
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t _{KCY9}	4.5 V ≤ V _{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high-/low-level width	t _{KHS} , t _{KL9}	4.5 V ≤ V _{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V _{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V _{DD} ≤ 6.0 V			39063	bps
		2.7 V ≤ V _{DD} < 4.5 V			19531	bps
					9766	bps
ASCK rise, fall time	t _{RS} , t _{FS}	V _{DD} = 4.5 to 6.0 V, when not using external device expansion function.			1000	ns
					160	ns

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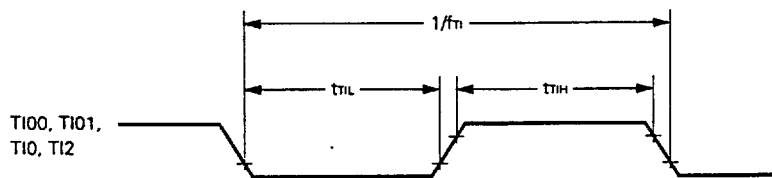
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

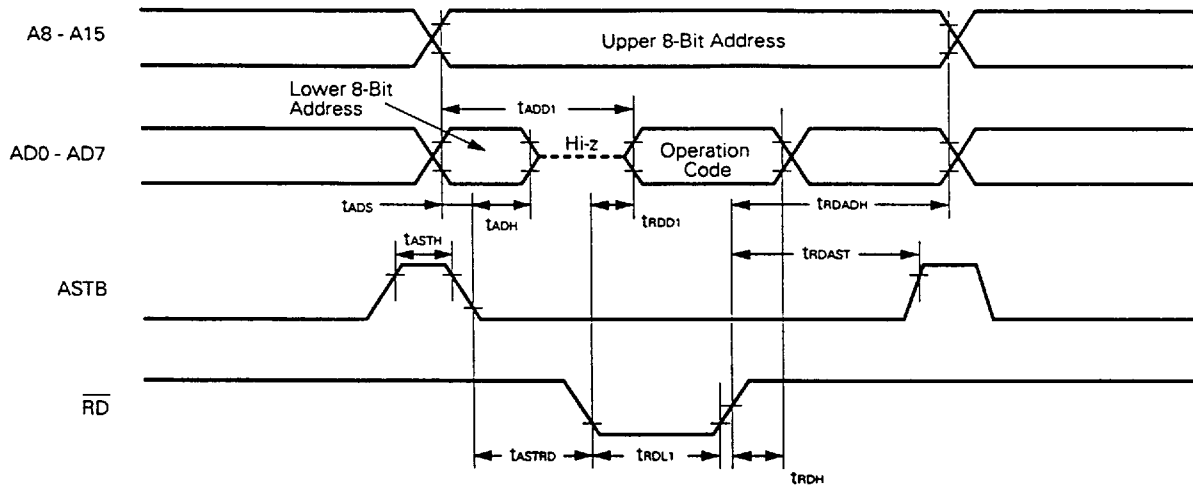


T1 Timing

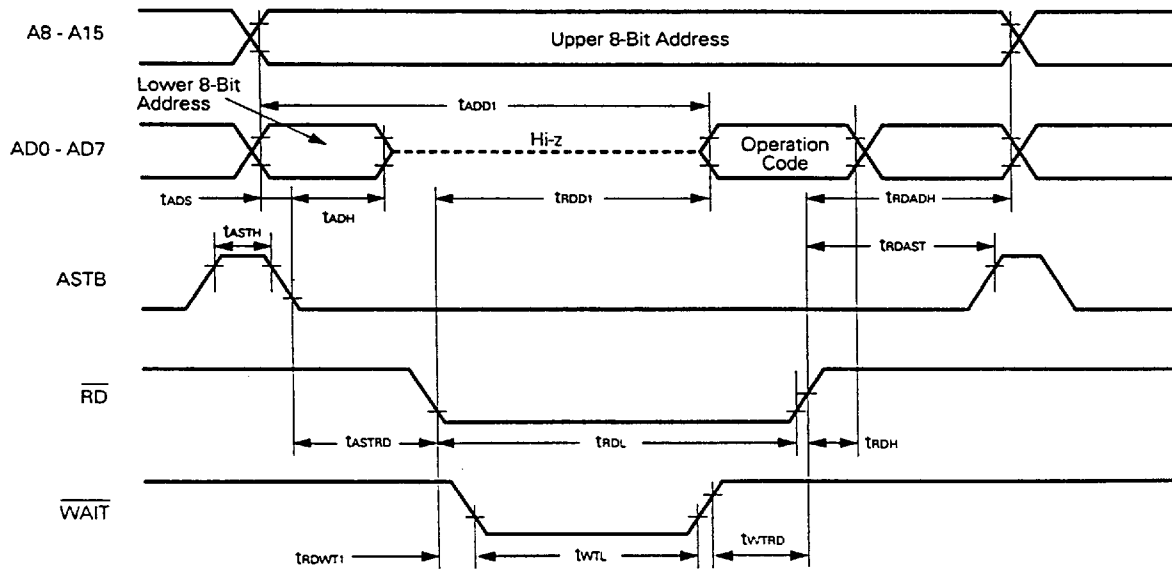


Read/Write Operation

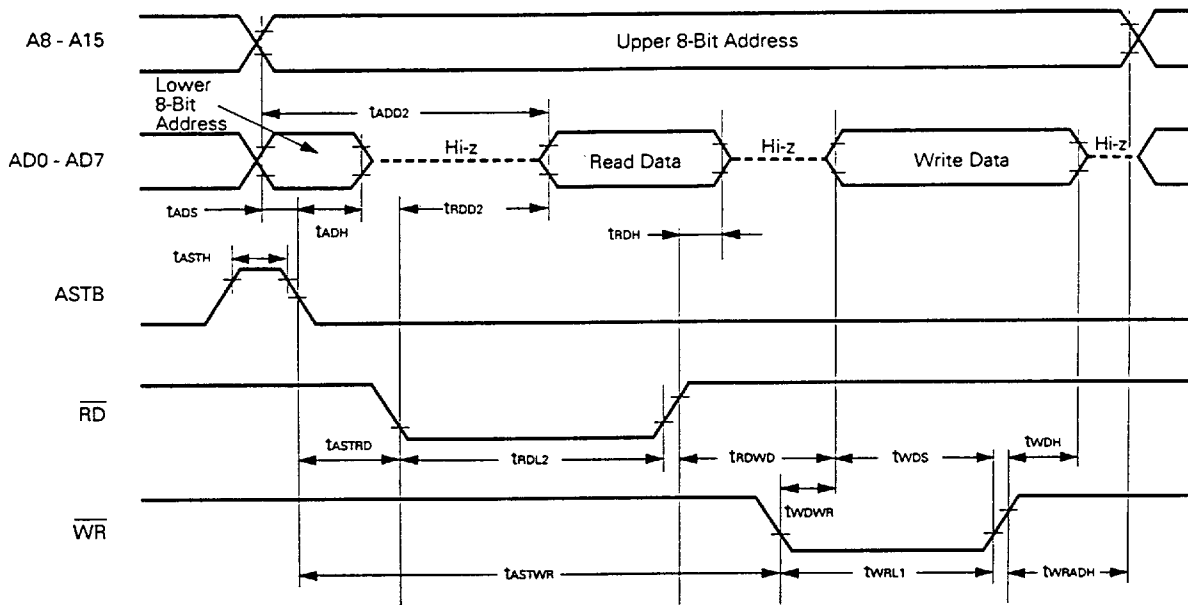
External Fetch (No Wait) :



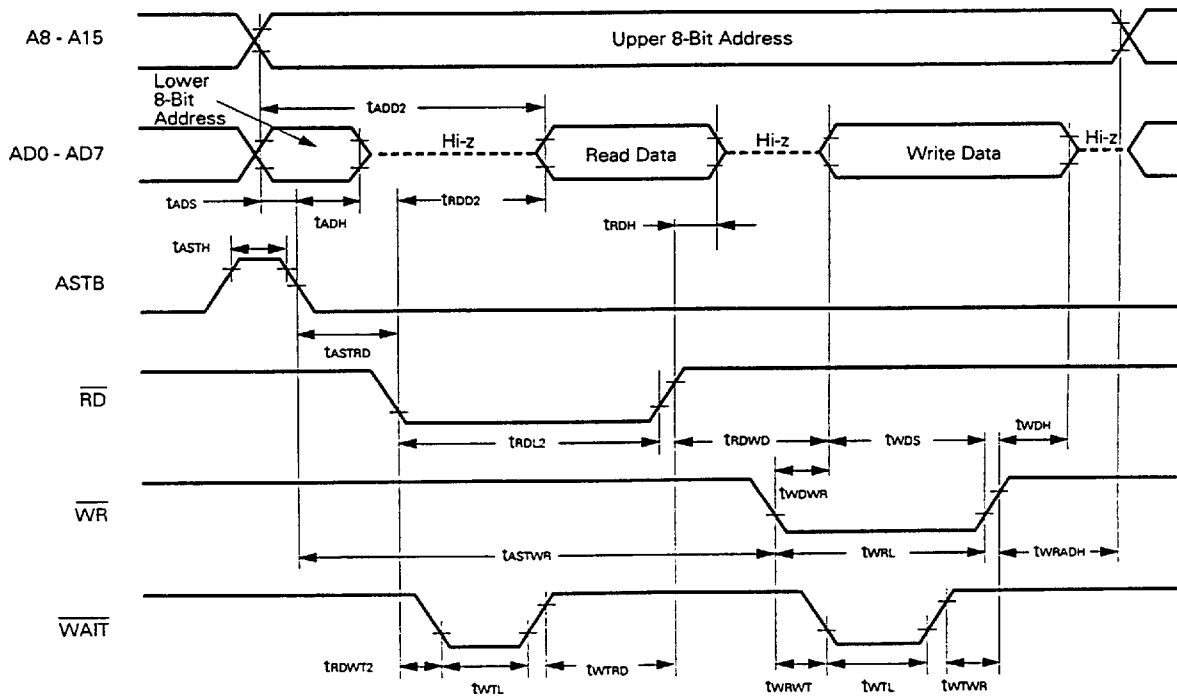
External Fetch (Wait Insertion) :



External Data Access (No Wait) :



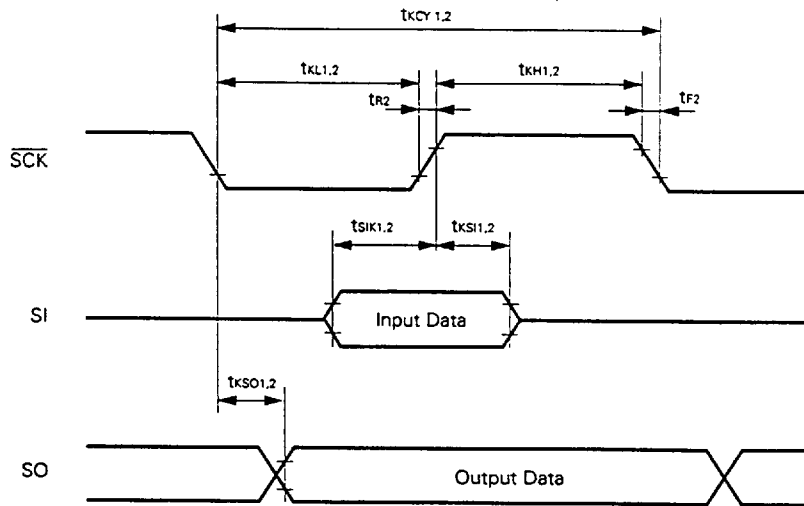
External Data Access (Wait Insertion) :



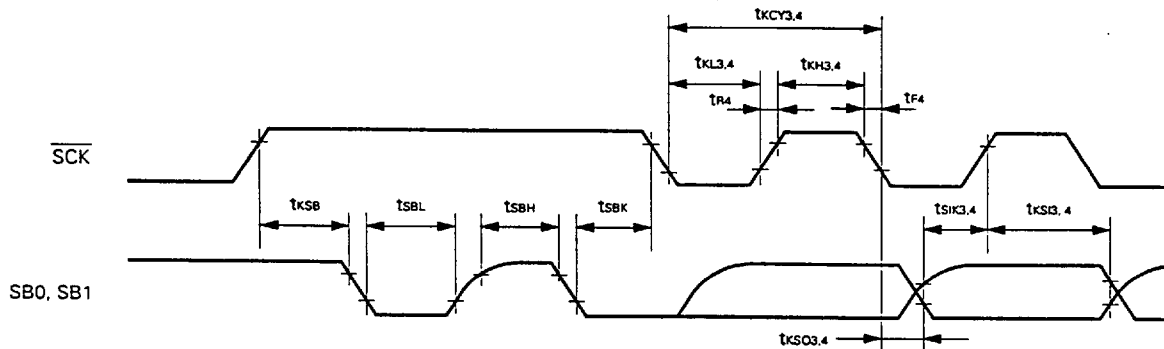
Serial Transfer Timing

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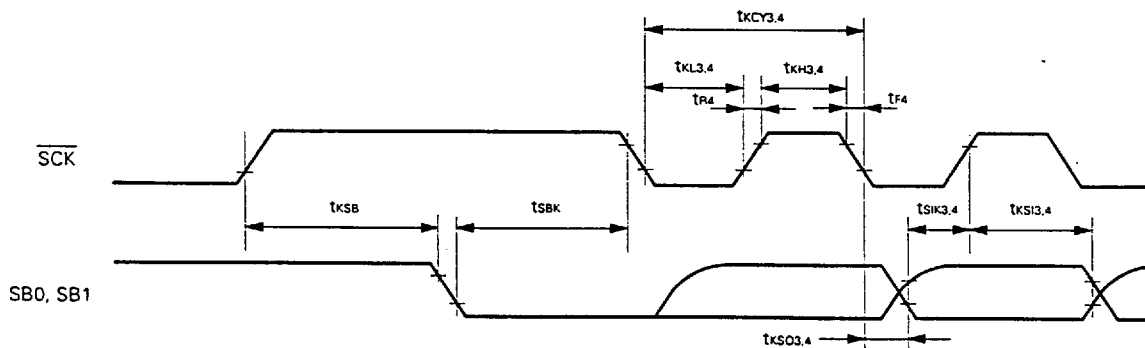
3-Wire Serial I/O Mode :



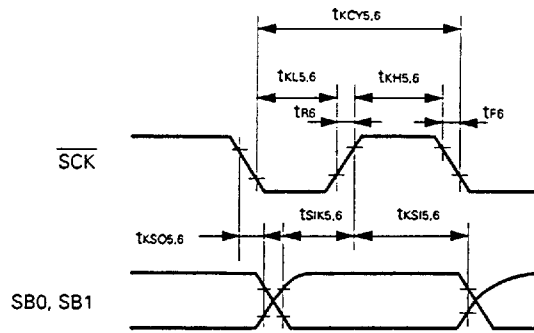
SBI Mode (Bus Release Signal Transfer) :



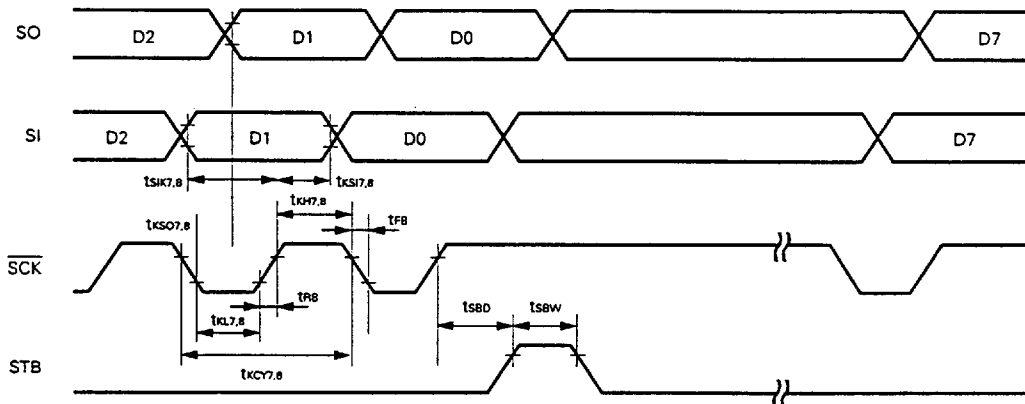
SBI Mode (COmmand Signal Transfer) :



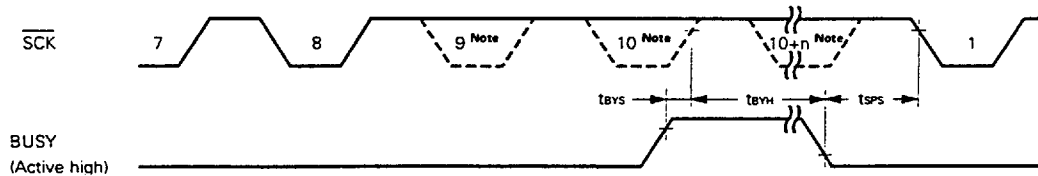
2-Wire Serial I/O Mode :



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function :

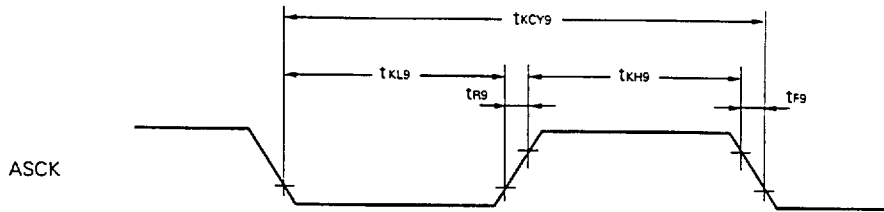


3-Wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing) :



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART Mode (External Clock Input) :



A/D CONVERTER CHARACTERISTICS (TA = -40 to +85 °C, AVDD = VDD = 2.0 to 6.0 V, AVSS = VSS = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error <i>Note</i>		2.7 V ≤ AVREF0 ≤ AVDD			0.6	%
		2.0 V ≤ AVREF0 < 2.7 V			1.4	%
Conversion time	tCONV		19.1		200	μs
Sampling time	tsAMP		12/fxx			μs
Analog input voltage	VIAN		AVSS		AVREF0	V
Reference voltage	AVREF0		2.0		AVDD	V
Resistance between AVREF0 and AVSS	RAIREFO		4	14		kΩ

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

- Remarks**
1. fxx: Main system clock frequency (fx or fx/2)
 2. fx: Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (TA = -40 to +85 °C, VDD = 2.0 to 6.0 V, AVSS = VSS = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error		R = 2MΩ <i>Note 1</i>			1.2	%
		R = 4MΩ <i>Note 1</i>			0.8	%
		R = 10MΩ <i>Note 1</i>			0.6	%
Settling time		<i>Note</i> C=30pF, 4.5 V ≤ AVREF1 ≤ 6.0 V			10	μs
		2.7 V ≤ AVREF1 < 4.5 V			15	μs
		2.0 V ≤ AVREF1 < 2.7 V			20	μs
Output resistance	Ro	DACS0, DACS1 = 55H <i>Note 2</i>		10		kΩ
Analog reference voltage	AVREF1		2.0		VDD	V
AVREF1 current	IREF1	<i>Note 2</i>			1.5	mA

- Notes**
1. R and C denote D/A converter output pin load resistance and load capacitance, respectively.
 2. Value for 1 D/A converter channel

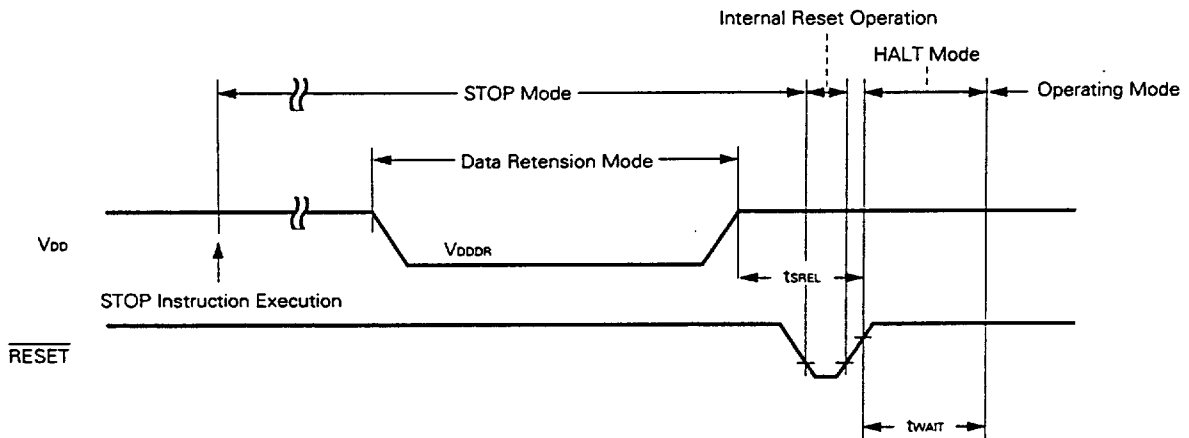
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = -40 to + 85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V _{DDDR}		1.8		6.0	V
Data retention power supply current	I _{DDDR}	V _{DDDR} = 1.8 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabiliation wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _x		ms
		Release by interrupt		Note		ms

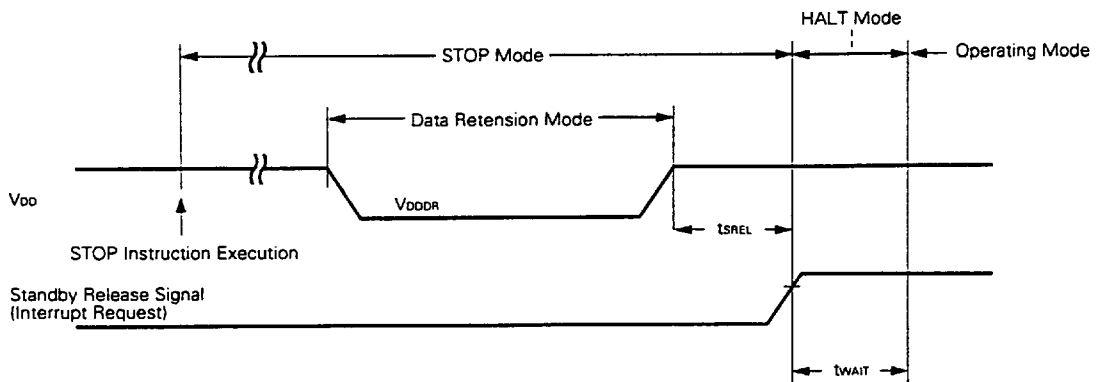
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of 2¹²/f_{xx} and 2¹⁴/f_{xx} to 2¹⁷/f_{xx} is possible.

Remark f_{xx}: Main system clock frequency (f_x or f_x/2)
x: Main system clock oscillator frequency

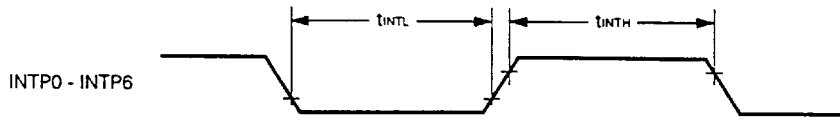
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



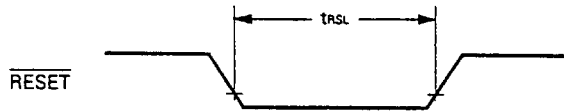
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



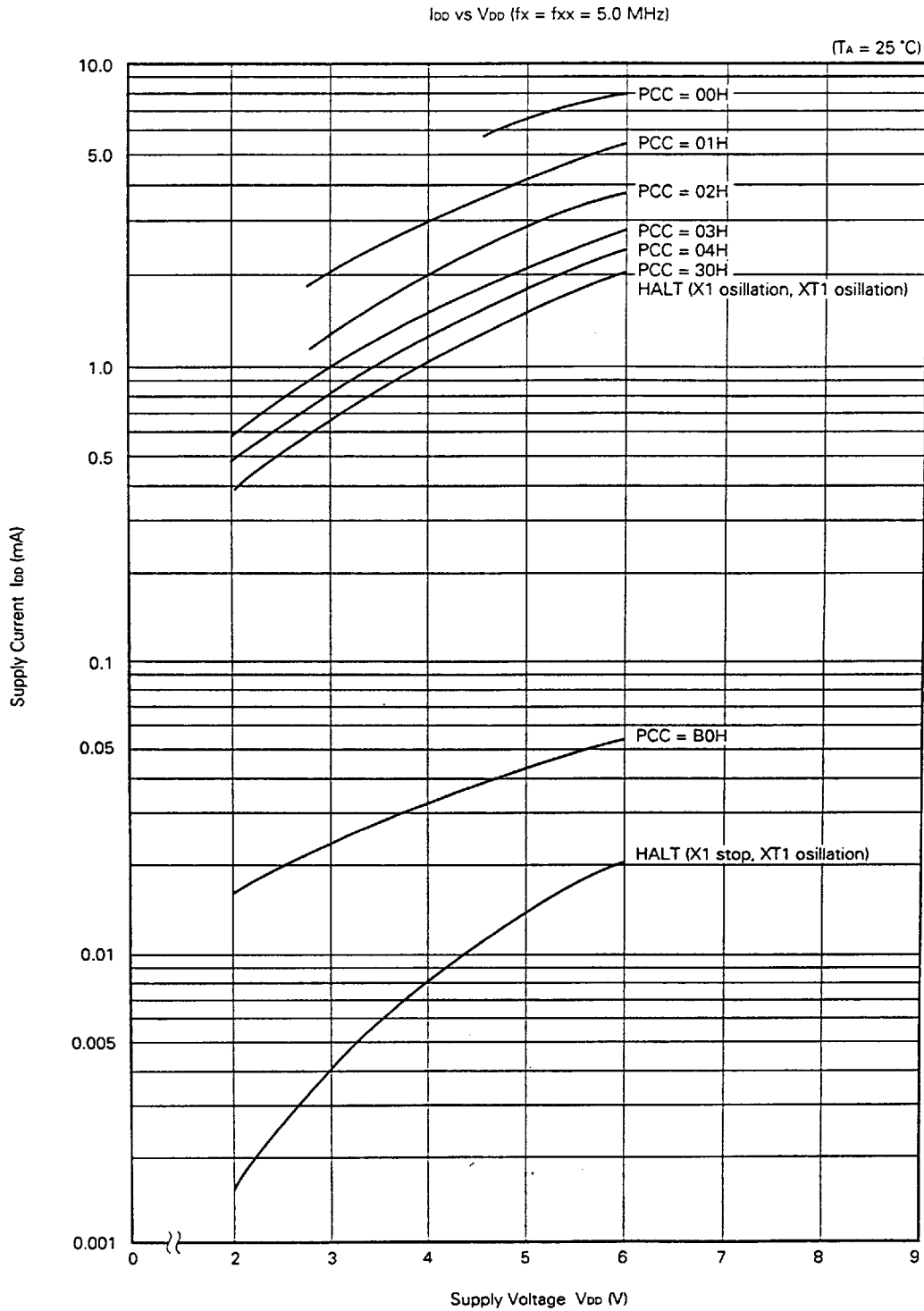
Interrupt Input Timing

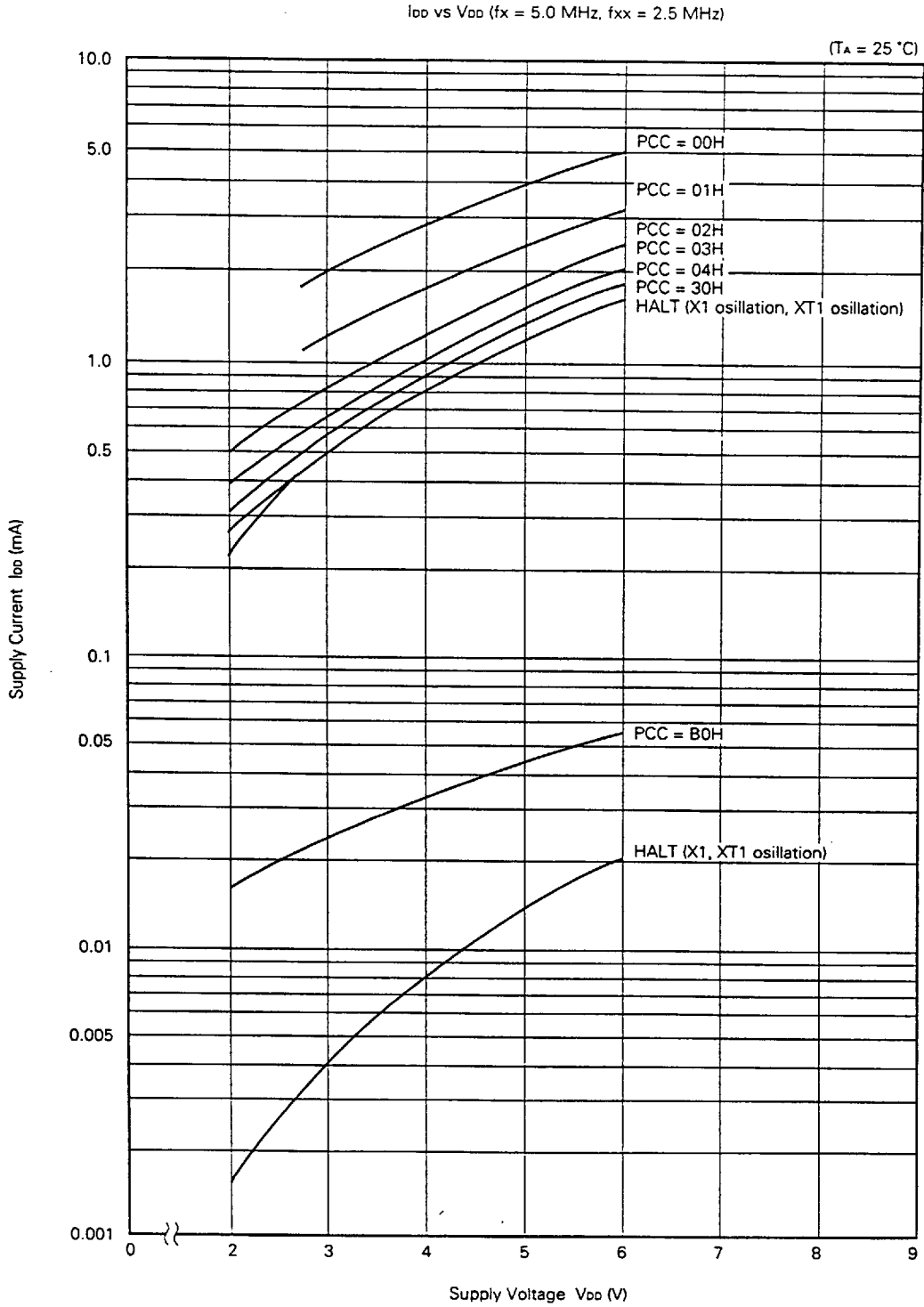


RESET Input Timing



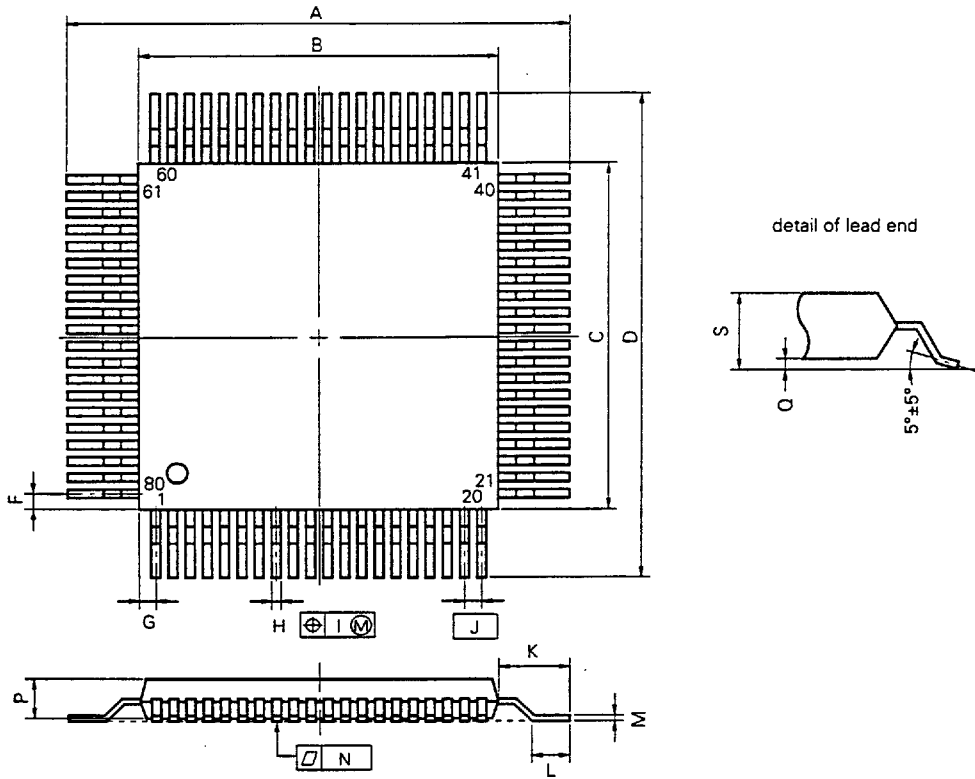
12. CHARACTERISTIC CURVES (REFERENCE VALUE)





13. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14 × 14)



NOTE

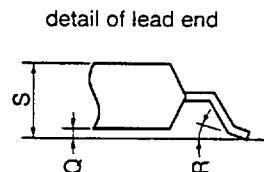
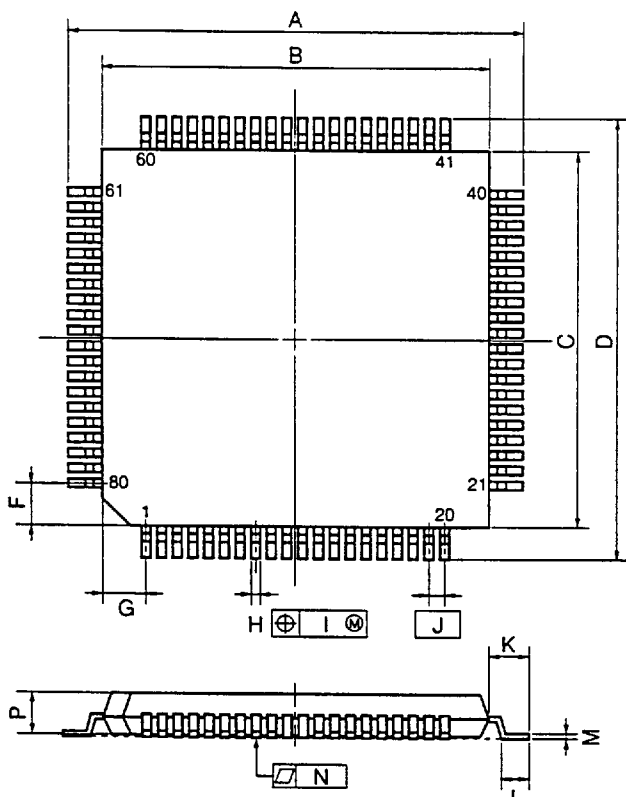
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S80GC-65-3B9-3

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

★ Remark Dimensions and materials of ES product are the same as those of mass-production products.

80 PIN PLASTIC TQFP (FINE PITCH) (12 × 12)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551 ^{+0.009} _{-0.008}
B	12.0±0.2	0.472 ^{+0.009} _{-0.008}
C	12.0±0.2	0.472 ^{+0.009} _{-0.008}
D	14.0±0.2	0.551 ^{+0.009} _{-0.008}
F	1.25	0.049
G	1.25	0.049
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.145 ^{+0.055} _{-0.045}	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

Remark Dimensions and materials of ES product are the same as those of mass-production products.

★

14. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.
 For detail of recommended soldering conditions, refer to the information document "Semiconductor Device Mounting Technology Manual" (IEI-1207).
 For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 14-1. Surface Mounting Type Soldering Conditions (1/2)

- (1) μPD78052GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm)
- μPD78053GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm)
- μPD78054GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm)
- ★ μPD78055GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm)
- ★ μPD78056GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm)
- ★ μPD78058GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max. <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Twice max. <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature : 260 °C max., Duration : 10 sec. max., Number of times : once, Preheating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Table 14-1. Surface Mounting Type Soldering Conditions (2/2)

- (2) μPD78052GK-xxx-BE9 : 80-pin plastic QFP (12 × 12 mm)
- μPD78053GK-xxx-BE9 : 80-pin plastic QFP (12 × 12 mm)
- μPD78054GK-xxx-BE9 : 80-pin plastic QFP (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max., Time limit: 7 days ^{Note} (thereafter 10 hours 125 °C prebaking required) <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-107-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Twice max., Time limit: 7 days ^{Note} (thereafter 10 hours 125 °C prebaking required) <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-107-2
Pin Part Heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Note For the storage period after dry-pack decompression storage conditions are max. 25 °C, 65 % RH.

Caution Use of more than one soldering method should be avoided (except in the case of pin part heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78054.

Language Processing Software

RA78K/0 <i>Note 1, 2, 3</i>	78K/0 series common assembler package
CC78K/0 <i>Note 1, 2, 3</i>	78K/0 series common C compiler package
★ DF78054 <i>Note 1, 2, 3</i>	μPD78054 subseries device file
CC78K/0-L <i>Note 1, 2, 3</i>	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054GK PA-78P054KK-T	Programmer adapters connected to PG-1500
PG-1500 controlle <i>Note 1, 2</i>	PG-1500 control program

Debugging Tools

IE-78000-R	In-circuit emulator common to 78K/0 series
IE-78000-R-BK	Break board common to 78K/0 series
IE-78064-R-EM	Emulation board common to μPD78064 subseries
EP-78230GC-R	Emulation probe common to μPD78234 subseries
EP-78054GK-R	Emulation probe for μPD78054 subseries
EV-9200GC-80	Socket to be mounted on the user system board manufactured for 80-pin plastic QFP
EV-9200GK-80	Adapter to be mounted in the user system board manufactured for 80-pin plastic TQFP
SD78K/0 <i>Note 1, 2</i>	IE-78000-R screen debugger
★ DF78054 <i>Note 1, 2, 4, 5</i>	μPD78054 Subseries device file
SM78K/0 <i>Note 4, 5, 6</i>	78K/0 series common system simulator

Real-Time OS

★ RX78K/0 <i>Note 1, 2, 3</i>	78K/0 series common real-time OS
MX78K/0 <i>Note 1, 2, 3, 4</i>	78K/0 series common real-time OS

Notes 1. PC-9800 series (MS to DOST™) based

2. IBM PC/AT™ (PC DOS™) based

3. HP9000 series 300™, HP9000 series 700™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series (EWS-UX/V) based

★ 4. PC-9800 series (MS-DOS + Windows™) based

★ 5. IBM PC/AT (PC DOS + Windows) based

6. Under development

Fuzzy Inference Development Support System

FE9000 Note 1/ FE9200 Note 2	Fuzzy knowledge data creation tool
FT9080 Note 1/ FT9085 Note 3	Translator
FI78K/0 Note 1, 3	Fuzzy inference module
FD78K/0 Note 1, 3	Fussy inference debugger

- Notes**
1. PC-9800 series (MS-DOS™) based
 2. IBM PC/AT (PC DOS + Windows) based
 3. IBM PC/AT (PC DOS) based

- Remarks**
1. For third party development tools, see the 78K/0 Series Selection Guide (IF-1185).
 2. RA78K/0, CC78K/0, SD78K/0 and SM78K/0 are used in combination with DF78054.

★

★ APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No. (Japanese)	Document No. (English)
User's Manual		IEU-824	IEU-1356
78K/0 Series User's Manual Instruction		IEU-849	IEU-1372
78K/0 Series Application Note	Introduction (II)	IEA-740	IEA-1299
	Floating point operation program volume	IEA-718	IEA-1289

Development Tool Related Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78064-R-EM		EEU-905	EEU-1443
EP-78054GK-R		EEU-932	EEU-1468
SD78K/0 Screen Debugger	Primer	EEU-852	EEU-1414
	Reference	EEU-816	EEU-1413

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

Embedded Software Documents (User's Manual)

Document Name	Document No. (Japanese)	Document No. (English)
Fuzzy Knowledge Data Creation Tool	EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy, Inference Development Support System -Translator	EEU-862	EEU-1444

Other Documents

Document Name	Document No. (Japanese)	Document No. (English)
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grades on Semiconductor Devices	IEI-620	IEI-1209
Semiconductor Devices Quality Guarantee Guide	MEI-603	MEI-1202

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