FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21373-1E

ASSP

Dual Serial Input PLL Frequency Synthesizer

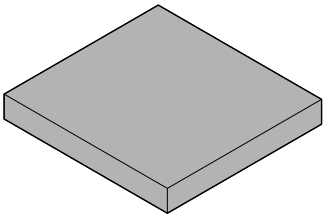
MB15F76UL

■ DESCRIPTION

The Fujitsu MB15F76UL is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 6.0 GHz and a 1.5 GHz prescalers. Both prescalers for RF and IF have a 1/4 divider. A 16/17 or a 32/33 for the 6.0 GHz prescaler, and a 4/5 or a 8/9 for the 1.5 GHz prescaler can be selected for the prescaler that enables pulse swallow operation. The BiCMOS process is used, as a result a supply current is typically 8.5 mA at 3.0 V. The supply voltage range is from 2.5 V to 3.6 V. A refined charge pump supplies well-balanced output current with 1.5 mA and 6 mA selectable by serial date. The pin assignments are is the same as the MB15F78UL. Fast locking is achieved for adopting the new circuit.
The new package (BCC20) decreases a mount area of MB15F76UL more than 30% comparing with the former BCC16 (for dual PLL) .

■ PACKAGE

20-pad plastic BCC



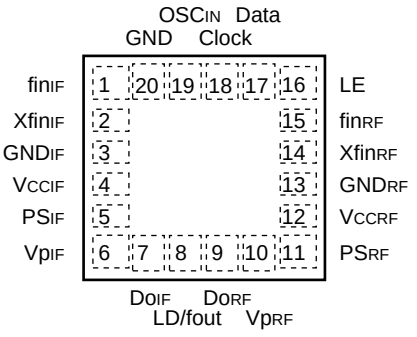
(LCC-20P-M05)

■ FEATURES

- High frequency operation : RF synthesizer : 6.0 GHz Max
  : IF synthesizer : 1.5 GHz Max
- Low power supply voltage : V_{CC} = 2.5 V to 3.6 V
- Ultra low power supply current : I_{CC} = 8.5 mA Typ
  (V_{CC} = Vp = 3.0 V, Ta = +25 °C, SW_{IF} = SW_{RF} = 0 in IF/RF locking state)
- Direct power saving function : Power supply current in power saving mode
  Typ. 0.1 µA (V_{CC} = Vp = 3.0 V, Ta = +25 °C)
  Max. 10 µA (V_{CC} = Vp = 3.0 V)
- Software selectable charge pump current : 1.5 mA/6.0 mA Typ
- Dual modulus prescaler : 6.0 GHz prescaler (1/4 divider and 16/17 or 32/33) /
  1.5 GHz prescaler (1/4 divider and 4/5 or 8/9)
- 23-bit shift register
- Serial input binary 14-bit programmable reference divider : R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 5-bit swallow counter : 0 to 31
  - Binary 13-bit programmable counter : 3 to 8,191
- Built-in high-speed tuning, low-noise phase comparator, current-switching type constant current circuit
- On-chip phase control for phase comparator
- On-chip phase comparator for fast lock and low noise
- Built-in digital locking detector circuit to detect PLL locking and unlocking
- Operating temperature : Ta = –40 °C to +85 °C

■ PIN ASSIGNMENT

(BCC-20)
TOP VIEW

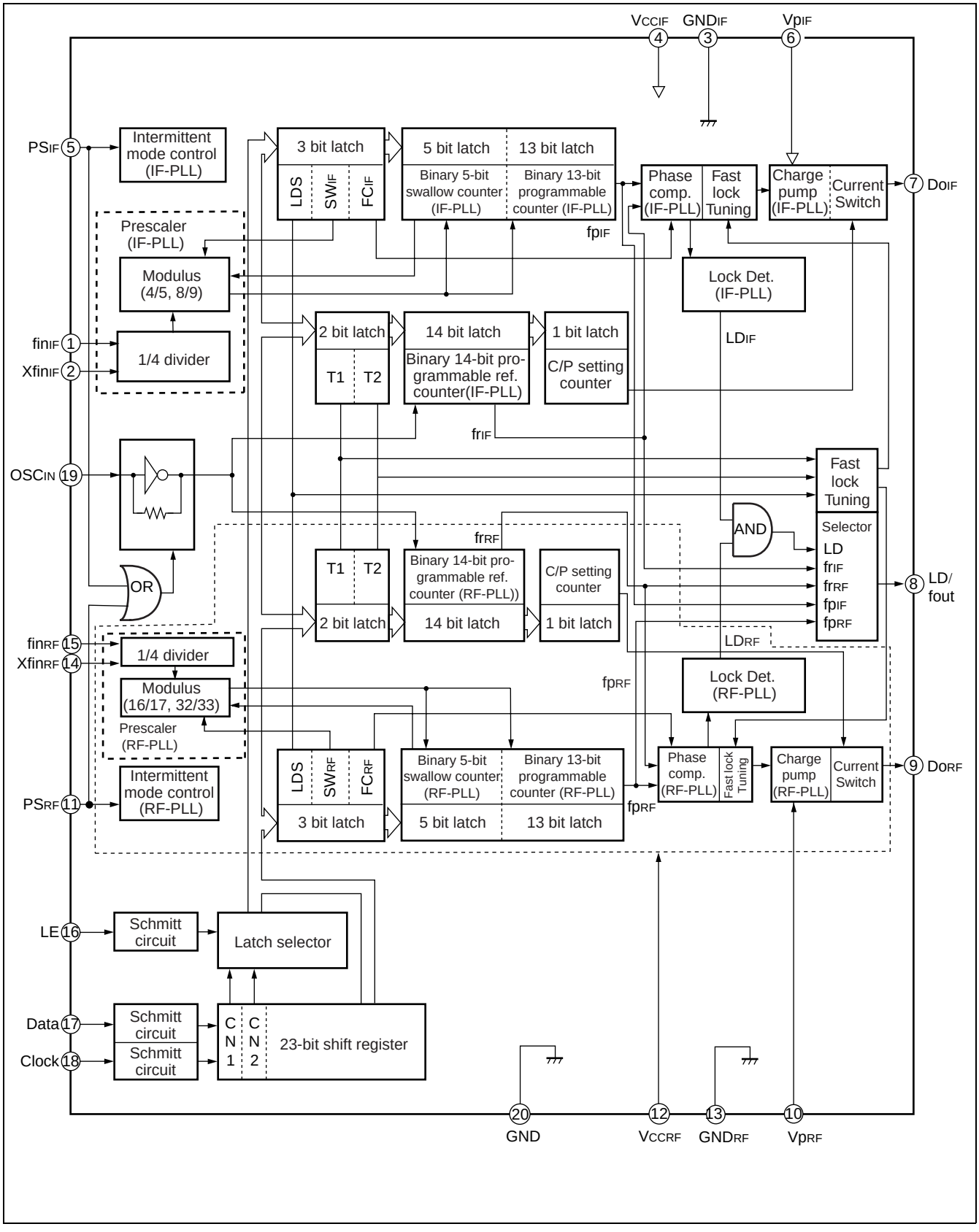


(LCC-20P-M05)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O	Descriptions
1	fin_{IF}	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be AC coupling.
2	$Xfin_{IF}$	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
3	GND_{IF}	—	Ground pin for the IF-PLL section.
4	V_{CCIF}	—	Power supply voltage input pin for the IF-PLL section (except for the charge pump circuit), the shift register and the oscillator input buffer.
5	PS_{IF}	I	Power saving mode control pin for the IF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS_{IF} = “H” ; Normal mode/PS_{IF} = “L” ; Power saving mode
6	Vp_{IF}	—	Power supply voltage input pin for the IF-PLL charge pump.
7	Do_{IF}	O	Charge pump output for the IF-PLL section.
8	LD/fout	O	Lock detect signal output (LD) /phase comparator monitoring output (fout) pin. The output signal is selected by LDS bit in a serial data. LDS bit = “H” ; outputs fout signal/LDS bit = “L” ; outputs LD signal
9	Do_{RF}	O	Charge pump output for the RF-PLL section.
10	Vp_{RF}	—	Power supply voltage input pin for the RF-PLL charge pump.
11	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS_{RF} = “H” ; Normal mode/PS_{RF} = “L” ; Power saving mode
12	V_{CCRF}	—	Power supply voltage input pin for the RF-PLL section (except for the charge pump circuit)
13	GND_{RF}	—	Ground pin for the RF-PLL section
14	$Xfin_{RF}$	I	Prescaler complimentary input pin for the RF-PLL section. This pin should be grounded via a capacitor.
15	fin_{RF}	I	Prescaler input pin for the RF-PLL. Connection to an external VCO should be via AC coupling.
16	LE	I	Load enable signal input pin (with the schmitt trigger circuit) When LE is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
17	Data	I	Serial data input pin (with the schmitt trigger circuit) Data is transferred to the corresponding latch (IF-ref. counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
18	Clock	I	Clock input pin for the 23-bit shift register (with the schmitt trigger circuit) One bit data is shifted into the shift register on a rising edge of the clock.
19	OSC_{IN}	I	The programmable reference divider input pin. TCXO should be connected with an AC coupling capacitor.
20	GND	—	Ground pin for OSC input buffer and the shift register circuit.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min.	Max.	
Power supply voltage		V_{CC}	–0.5	4.0	V
		Vp	V_{CC}	4.0	V
Input voltage		V_I	–0.5	V_{CC} + 0.5	V
Output voltage	LD/fout	V_O	GND	V_{CC}	V
	Do_{IF}, Do_{RF}	V_{DO}	GND	Vp	V
Storage temperature		Tstg	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.5	3.0	3.6	V	$V_{CCRF} = V_{CCIF}$
	Vp	V_{CC}	3.0	3.6	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	Ta	–40	—	+85	°C	

Note : • V_{CCRF}, Vp_{RF}, V_{CCIF} and Vp_{IF} must supply equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CCRF}, Vp_{RF}, V_{CCIF} and Vp_{IF} to keep them equal.
It is recommended that the non-use PLL is controlled by power saving function.

- Although this device contains an anti-static element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device.
  - When storing and transporting the device, put it in a conductive case.
  - Before handling the device, confirm the (jigs and) tools to be used have been uncharged (grounded) as well as yourself. Use a conductive sheet on working bench.
  - Before fitting the device into or removing it from the socket, turn the power supply off.
  - When handling (such as transporting) the device mounted board, protect the leads with a conductive sheet.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CCIF} *1	fin_{IF} = 570 MHz, V_{CCIF} = Vp_{IF} = 3.0 V	1.8	2.3	2.9	mA
		I_{CCRF} *1	fin_{RF} = 4750 MHz, V_{CCRF} = Vp_{RF} = 3.0 V	5.2	6.2	7.5	mA
Power saving current		I_{PSIF}	PS_{IF} = PS_{RF} = "L"	—	0.1 *2	10	µA
		I_{PSRF}	PS_{IF} = PS_{RF} = "L"	—	0.1 *2	10	µA
Operating frequency	fin_{IF} *3	fin_{IF}	IF PLL	100	—	1500	MHz
	fin_{RF} *3	fin_{RF}	RF PLL	2000	—	6000	MHz
	OSC_{IN}	f_{OSC}	—	3	—	40	MHz
Input sensitivity	fin_{IF}	$Pfin_{IF}$	IF PLL, 50 Ω system	–15	—	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF PLL, 50 Ω system	–10	—	+2	dBm
Input available voltage	OSC_{IN}	V_{OSC}	—	0.5	—	V_{CC}	V_{P-P}
"H" level input voltage	Data LE Clock	V_{IH}	Schmitt trigger input	0.7 V_{CC} + 0.4	—	—	V
"L" level input voltage		V_{IL}	Schmitt trigger input	—	—	0.3 V_{CC} – 0.4	V
"H" level input voltage	PS_{IF} PS_{RF}	V_{IH}	—	0.7 V_{CC}	—	—	V
"L" level input voltage		V_{IL}	—	—	—	0.3 V_{CC}	V
"H" level input current	Data LE Clock PS	I_{IH} *4	—	–1.0	—	+1.0	µA
"L" level input current		I_{IL} *4	—	–1.0	—	+1.0	µA
"H" level input current	OSC_{IN}	I_{IH}	—	0	—	+100	µA
"L" level input current		I_{IL} *4	—	–100	—	0	µA
"H" level output voltage	LD/ fout	V_{OH}	V_{CC} = Vp = 3.0 V, I_{OH} = –1 mA	V_{CC} – 0.4	—	—	V
"L" level output voltage		V_{OL}	V_{CC} = Vp = 3.0 V, I_{OL} = 1 mA	—	—	0.4	V
"H" level output voltage	Do_{IF} Do_{RF}	V_{DOH}	V_{CC} = Vp = 3.0 V, I_{DOH} = –0.5 mA	Vp – 0.4	—	—	V
"L" level output voltage		V_{DOL}	V_{CC} = Vp = 3.0 V, I_{DOL} = 0.5 mA	—	—	0.4	V
High impedance cutoff current	Do_{IF} Do_{RF}	I_{OFF}	V_{CC} = Vp = 3.0 V, V_{OFF} = 0.5 V to Vp – 0.5 V	—	—	2.5	nA
"H" level output current	LD/ fout	I_{OH} *4	V_{CC} = Vp = 3.0 V	—	—	–1.0	mA
"L" level output current		I_{OL}	V_{CC} = Vp = 3.0 V	1.0	—	—	mA

(Continued)

(Continued)

(V_{CC} = 2.5 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
"H" level output current	D_{OIF} *8 D_{ORF}	I_{DOH} *4	V_{CC} = Vp = 3.0 V, V_{DOH} = Vp / 2, Ta = +25 °C	CS bit = "H"	–8.2	–6.0	–4.1	mA
				CS bit = "L"	–2.2	–1.5	–0.8	mA
"L" level output current	D_{OIF} *8 D_{ORF}	I_{DOL}	V_{CC} = Vp = 3.0 V, V_{DOL} = Vp / 2, Ta = +25 °C	CS bit = "H"	4.1	6.0	8.2	mA
				CS bit = "L"	0.8	1.5	2.2	mA
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT} *5	V_{DO} = Vp / 2		—	3	10	%
	vs V_{DO}	I_{DOVD} *6	0.5 V ≤ V_{DO} ≤ Vp – 0.5 V		—	10	15	%
	vs Ta	I_{DOTA} *7	–40 °C ≤ Ta ≤ +85 °C, V_{DO} = Vp / 2		—	5	10	%

*1 : Conditions ; fosc = 10.0 MHz, Ta = +25 °C, SW = "L" in locking state.

*2 : V_{CCIF} = Vp_{IF} = V_{CCRF} = Vp_{RF} = 3.0 V, fosc = 10.0 MHz, Ta = +25 °C, in power saving mode.
PS_{IF} = PS_{RF} = GND
V_{IH} = V_{CC}, V_{IL} = GND (at CLK, Data, LE)

*3 : AC coupling. 1000 pF capacitor is connected under the condition of Min. operating frequency.

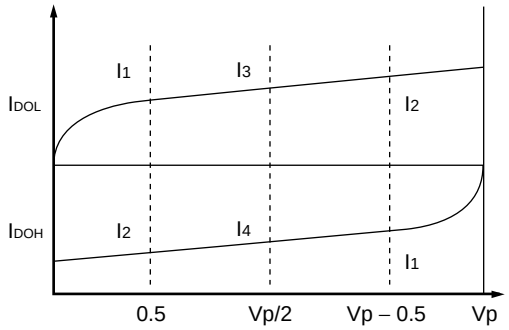
*4 : The symbol "–" (minus) means the direction of current flow.

*5 : V_{CC} = Vp = 3.0 V, Ta = +25 °C $(||I_3| - |I_4||) \ / \ [\ (|I_3| + |I_4|) \ / \ 2] \times 100$ (%)

*6 : V_{CC} = Vp = 3.0 V, Ta = +25 °C $[\ (||I_2| - |I_1||) \ / \ 2] \ / \ [\ (|I_1| + |I_2|) \ / \ 2] \times 100$ (%) (Applied to both I_{DOL} and I_{DOH})

*7 : V_{CC} = Vp = 3.0 V, $[||I_{DO}(+85\,°C)| - |I_{DO}(-40\,°C)|| \ / \ 2] \ / \ [|I_{DO}(+85\,°C)| + |I_{DO}(-40\,°C)| \ / \ 2] \times 100$ (%) (Applied to both I_{DOL} and I_{DOH})

*8 : When Charge pump current is measured, set LDS = "L" , T1 = "L" and T2 = "H".



Charge pump output voltage (V)

■ FUNCTIONAL DESCRIPTION

1. Pulse swallow function

$f_{VCO} = [(P \times N) + A] \times 4 \times f_{OSC} \div R$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
P : Preset divide ratio of dual modulus prescaler (4 or 8 for IF-PLL, 16 or 32 for RF-PLL)
N : Preset divide ratio of binary 13-bit programmable counter (3 to 8,191)
A : Preset divide ratio of binary 5-bit swallow counter ($0 \leq A \leq 31$, $A < N$)
f_{OSC} : Reference oscillation frequency (OSC_{IN} input frequency)
R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

2. Serial Data Input

The serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.
The serial data of binary data is entered through Data pin.
On rising edge of Clock, one bit of the serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latches depending upon the control bit data setting.

	The programmable reference counter for the IF-PLL	The programmable reference counter for the RF-PLL	The programmable counter and the swallow counter for the IF-PLL	The programmable counter and the swallow counter for the RF-PLL
CN1	0	1	0	1
CN2	0	0	1	1

(1) Shift Register Configuration

• **Programmable Reference Counter**

(LSB) ← Data Flow → (MSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	CS	X	X	X	X

CS : Charge pump current select bit
R1 to R14 : Divide ratio setting bits for the programmable reference counter (3 to 16,383)
T1, 2 : LD/fout output setting bit
CN1, 2 : Control bit
X : Dummy bits (Set “0” or “1”)

Note : Data input with MSB first.

• Programmable Counter

(LSB) Data Flow → (MSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	$SW_{IF/RF}$	$FC_{IF/RF}$	A1	A2	A3	A4	A5	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13

A1 to A5 : Divide ratio setting bits for the swallow counter (0 to 31)
N1 to N13 : Divide ratio setting bits for the programmable counter (3 to 8,191)
LDS : LD/fout signal select bit
$SW_{IF/RF}$: Divide ratio setting bit for the prescaler (IF : SW_{IF}, RF : SW_{RF})
$FC_{IF/RF}$: Phase control bit for the phase detector (IF : FC_{IF}, RF : FC_{RF})
CN1, 2 : Control bit

Note : Data input with MSB first.

(2) Data setting

• Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 13-bit Programmable Counter Data Setting

Divide ratio	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited

• Binary 5-bit Swallow Counter Data Setting

Divide ratio	A5	A4	A3	A2	A1
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
31	1	1	1	1	1

• Prescaler Data Setting

Divide ratio	SW = "H"	SW = "L"
Prescaler divide ratio IF-PLL	4/5	8/9
Prescaler divide ratio RF-PLL	16/17	32/33

• Charge Pump Current Setting

Current value	CS
±6.0 mA	1
±1.5 mA	0

• LD/fout output Selectable Bit Setting

LD/fout pin state		LDS	T1	T2
LD output		0	0	0
		0	1	0
		0	1	1
fout output	fr_{IF}	1	0	0
	fr_{RF}	1	1	0
	fp_{IF}	1	0	1
	fp_{RF}	1	1	1

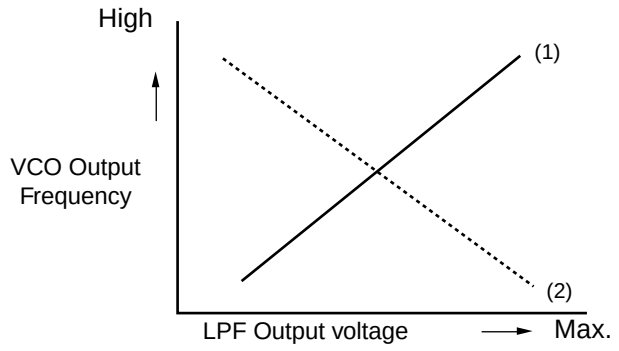
• Phase Comparator Phase Switching Data Setting

Phase comparator input	$FC_{IF, RF}$ = "H"	$FC_{IF, RF}$ = "L"
	$Do_{IF, RF}$	$Do_{IF, RF}$
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z

Z : High-impedance

Depending upon the VCO and LPF polarity, FC bit should be set.

(1) VCO polarity FC = "H"
(2) VCO polarity FC = "L"



Note : Give attention to the polarity for using active type LPF.

3. Power Saving Mode (Intermittent Mode Control Circuit)

Status	PS pin
Normal mode	H
Power saving mode	L

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

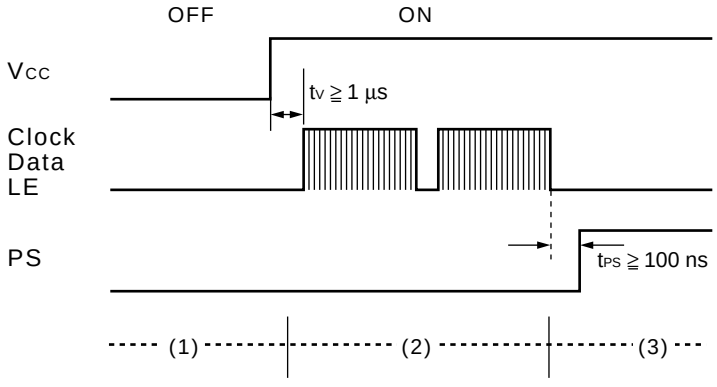
For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparaor output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

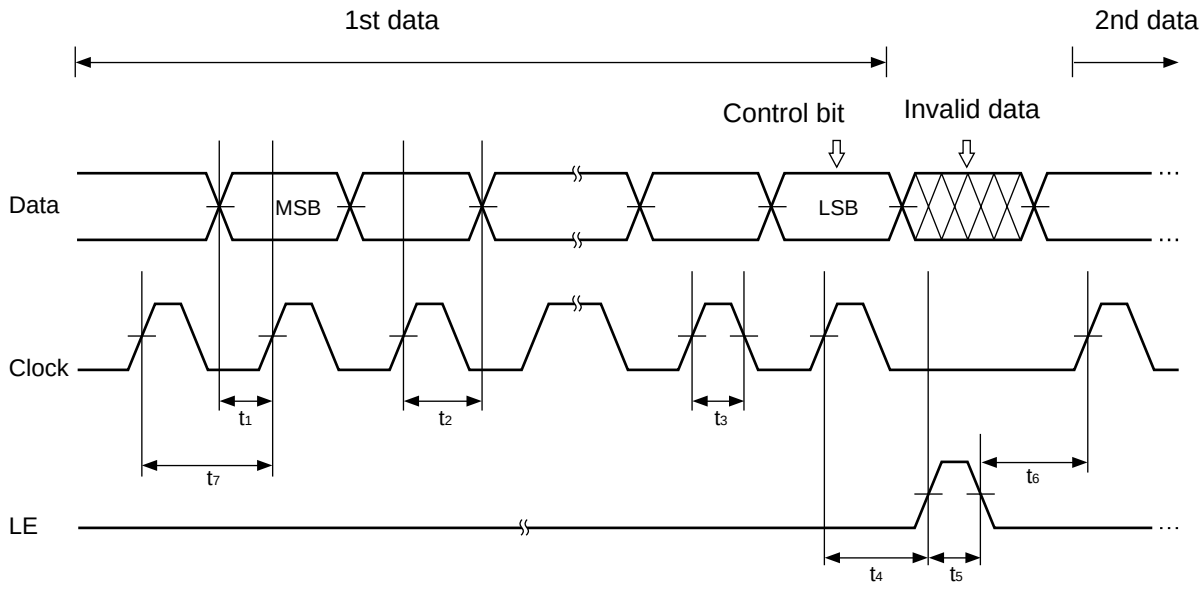
Notes : • When power (VCC) is first applied, the device must be in standby mode.
• PS pin must be set “L” at Power-ON.



(1) PS = L (power saving mode) at Power-ON
(2) Set serial data at least 1 µs after the power supply becomes stable ($V_{CC} \geq 2.2$ V) .
(3) Release power saving mode (PS_{IF}, PS_{RF} : “L” → “H”) at least 100 ns later after setting serial data.

4. Serial Data Input Timing

Divide ratio is performed through a serial interface using the Data pin, Clock pin, and LE pin.
Setting data is read into the shift register at the rise of the Clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.

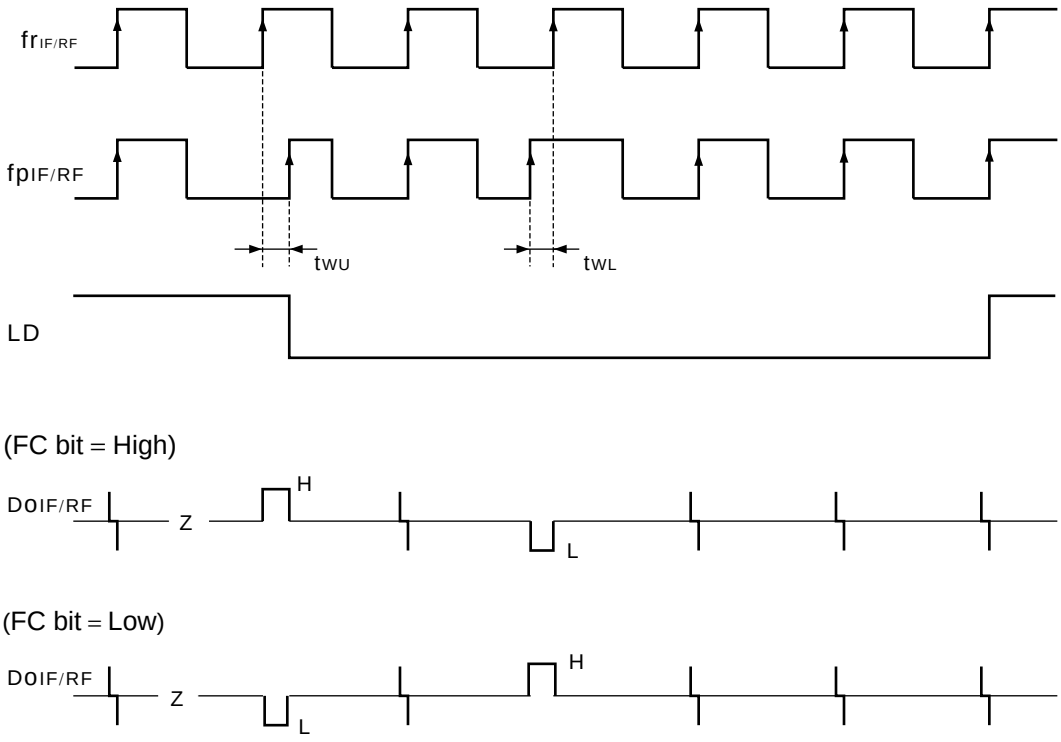


Parameter	Min	Typ	Max	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	30	—	—	ns

Parameter	Min	Typ	Max	Unit
t_5	100	—	—	ns
t_6	20	—	—	ns
t_7	100	—	—	ns

Note : LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



- LD Output Logic

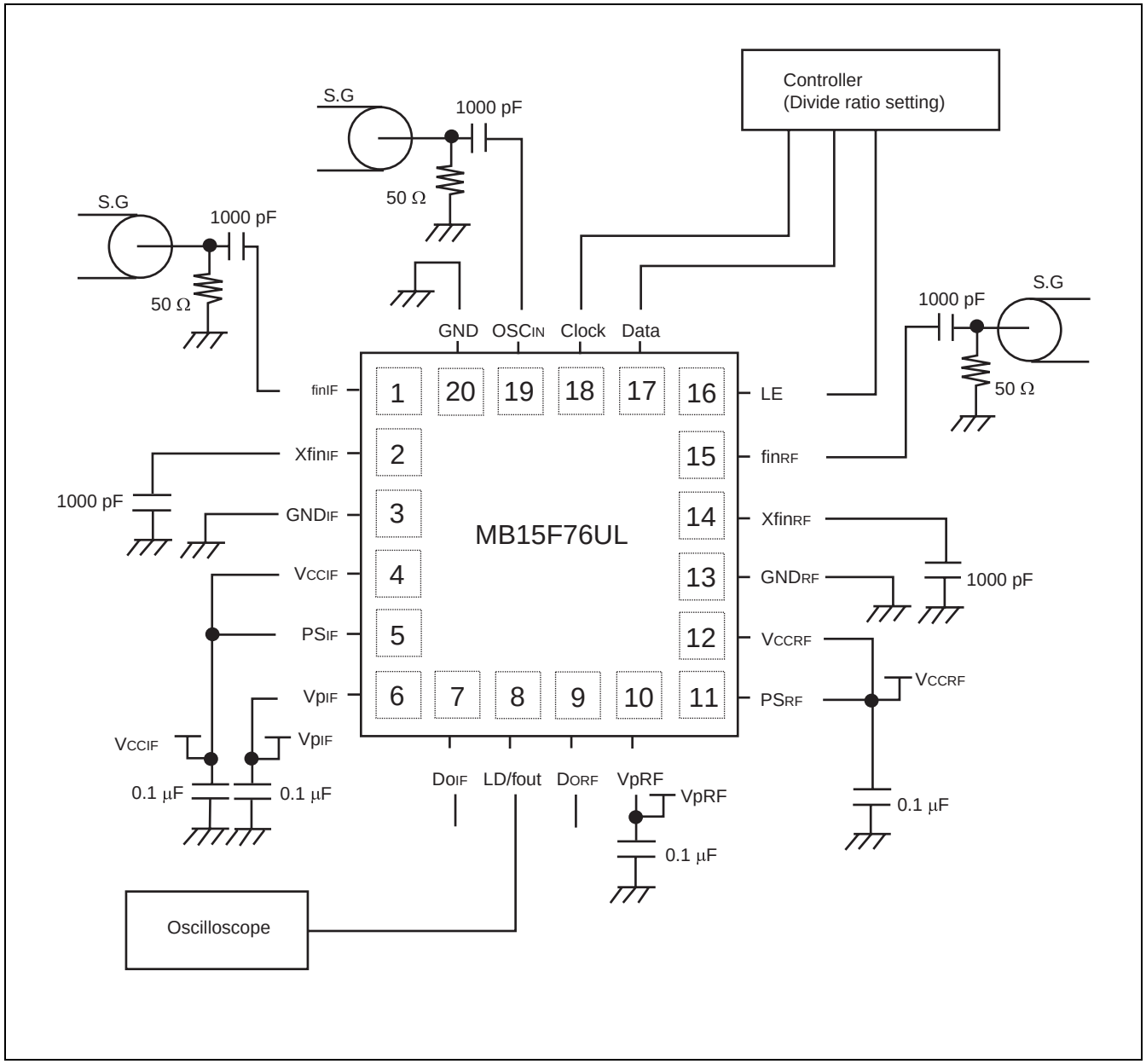
IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes : • Phase error detection range = -2π to $+2\pi$
- Pulses on $Do_{IF/RF}$ signals during locking state are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.

  $t_{WU} \geq 2/fosc$: e.g. $t_{WU} \geq 200$ ns when fosc = 10.0 MHz

  $t_{WU} \leq 4/fosc$: e.g. $t_{WL} \leq 400$ ns when fosc = 10.0 MHz

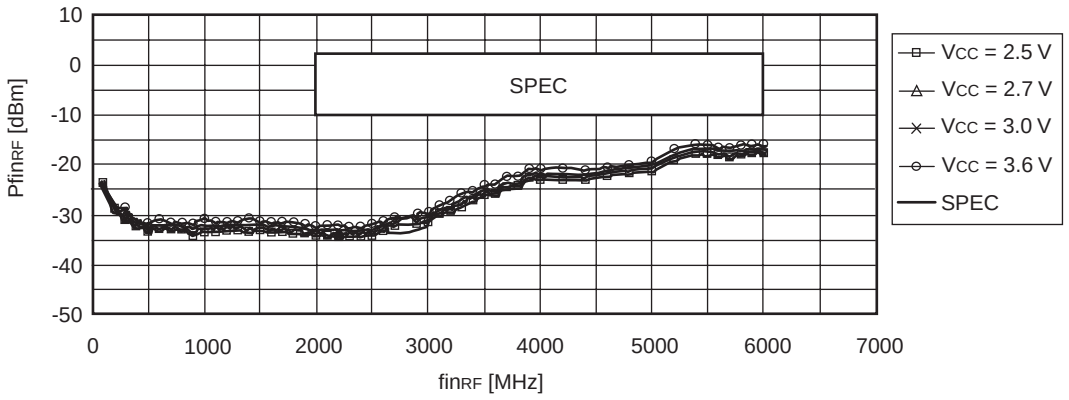
■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})



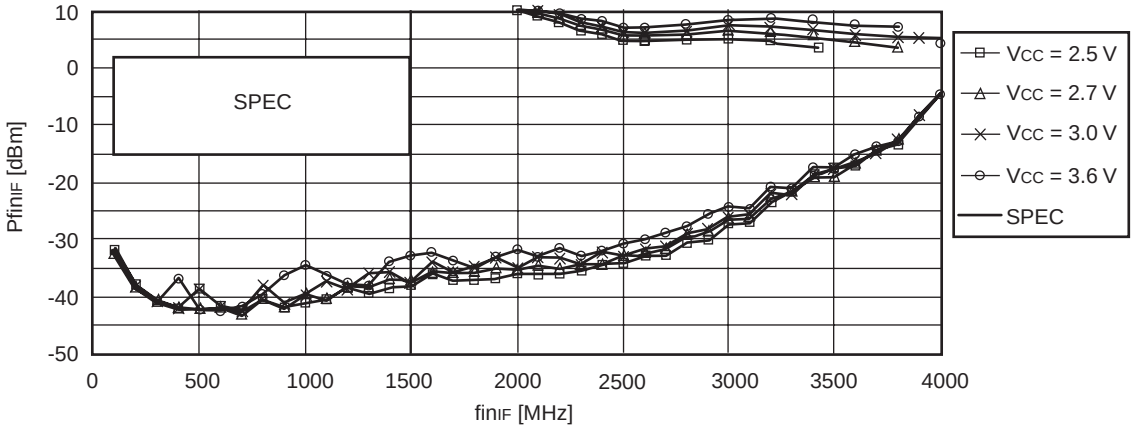
■ TYPICAL CHARACTERISTICS

1. fin input sensitivity

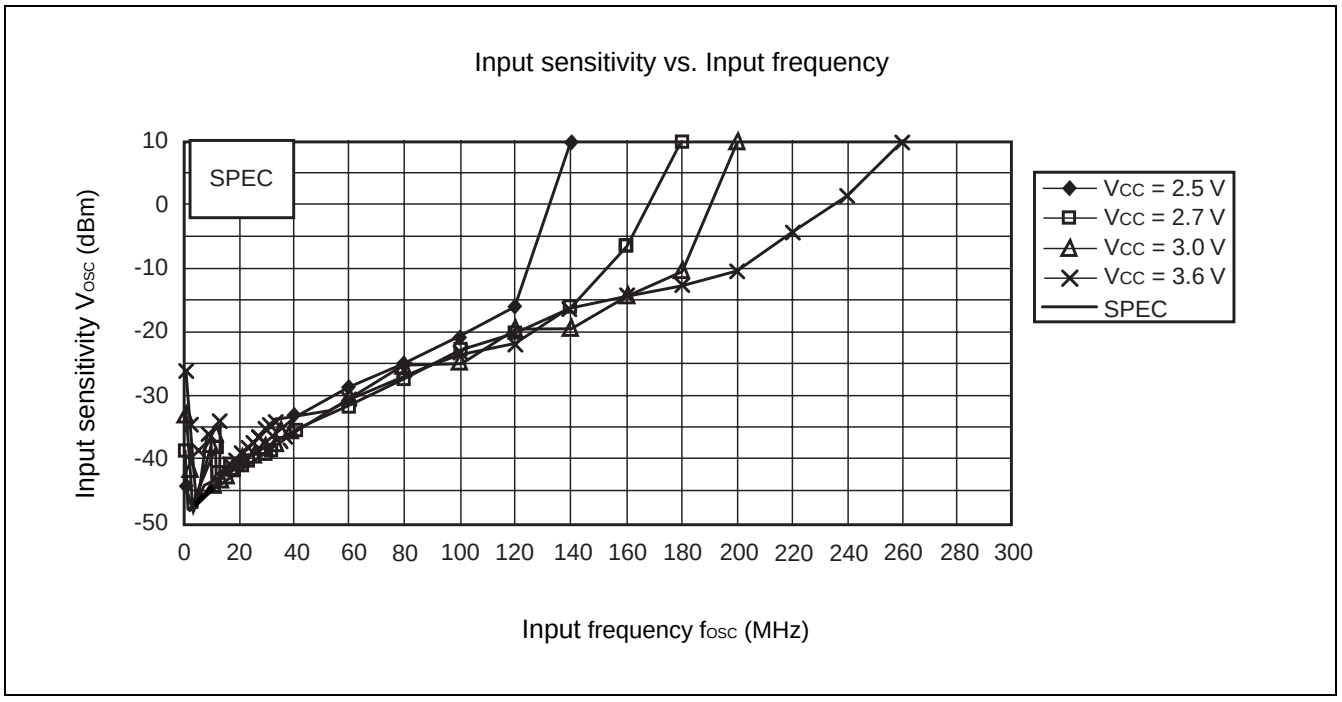
RF-PLL input sensitivity vs. Input frequency



IF-PLL input sensitivity vs. Input frequency



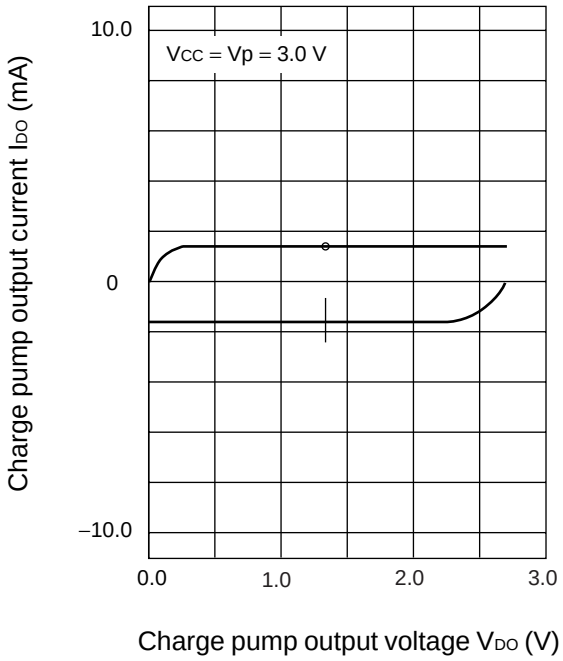
2. OSC_{IN} input sensitivity



3. RF-PLL Do output current

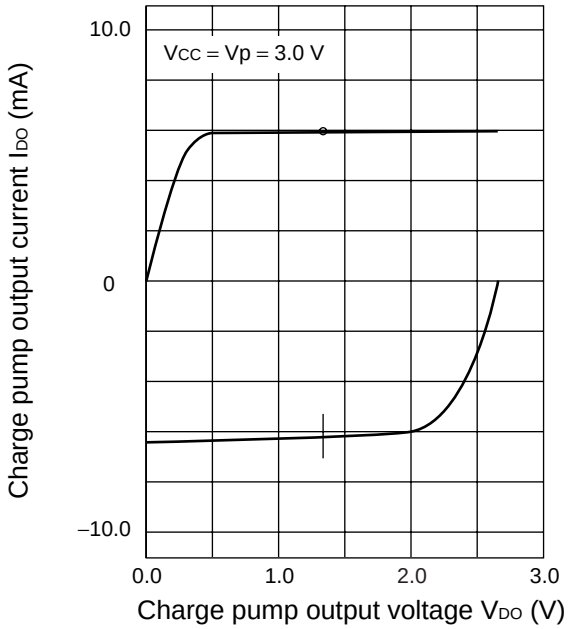
- 1.5 mA mode

$I_{DO} - V_{DO}$



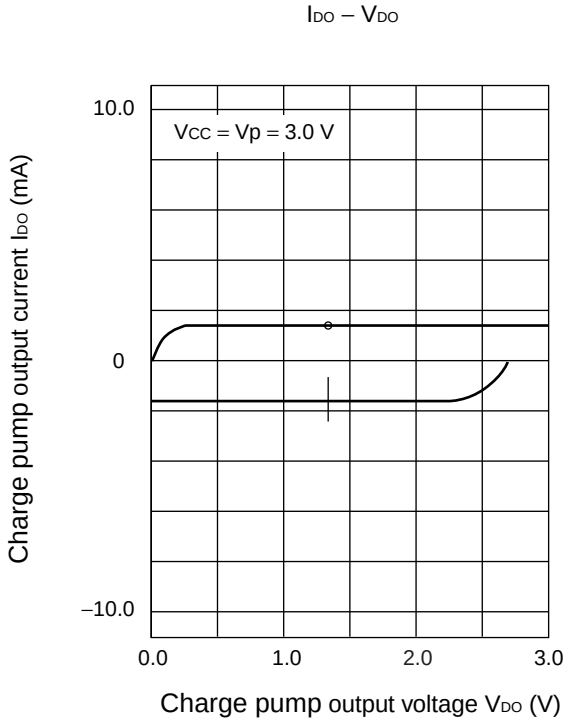
- 6.0 mA mode

$I_{DO} - V_{DO}$

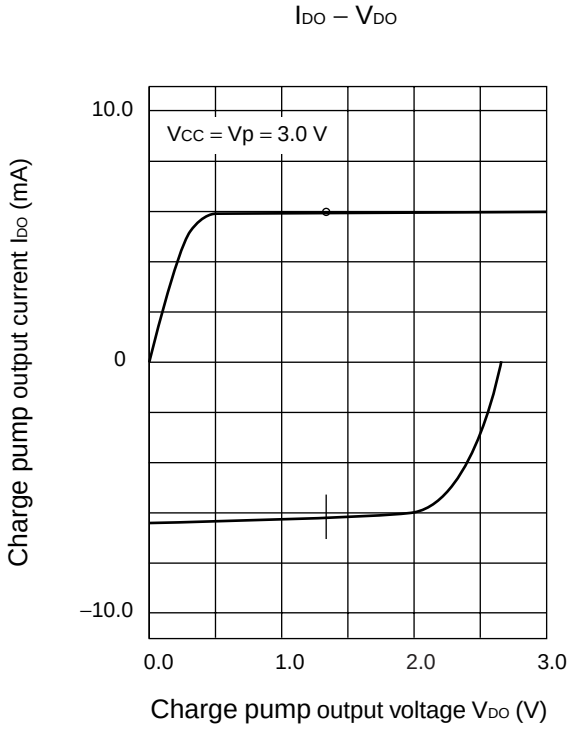


4. IF-PLL Do output current

- 1.5 mA mode

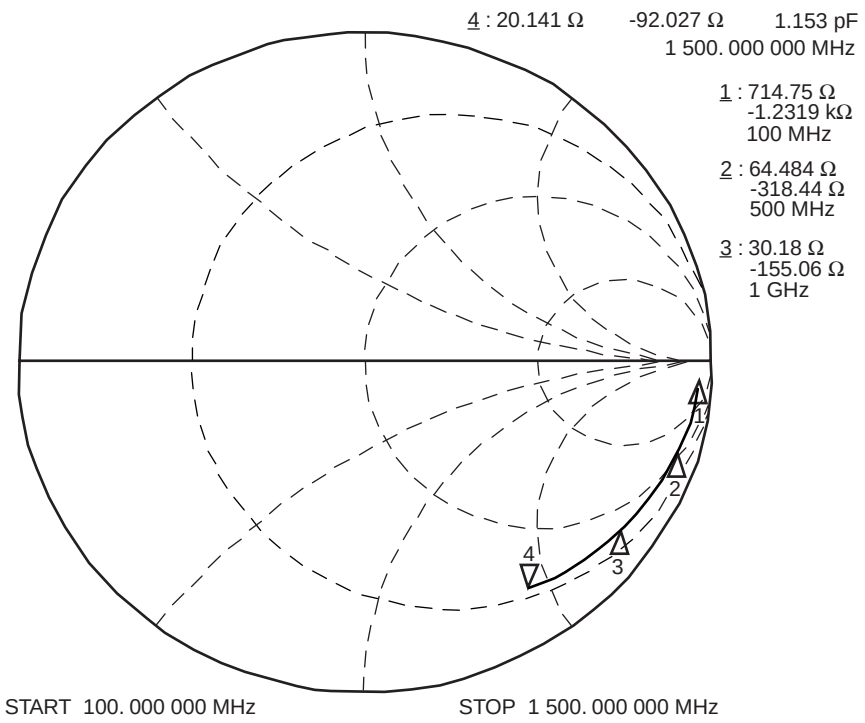


- 6.0 mA mode

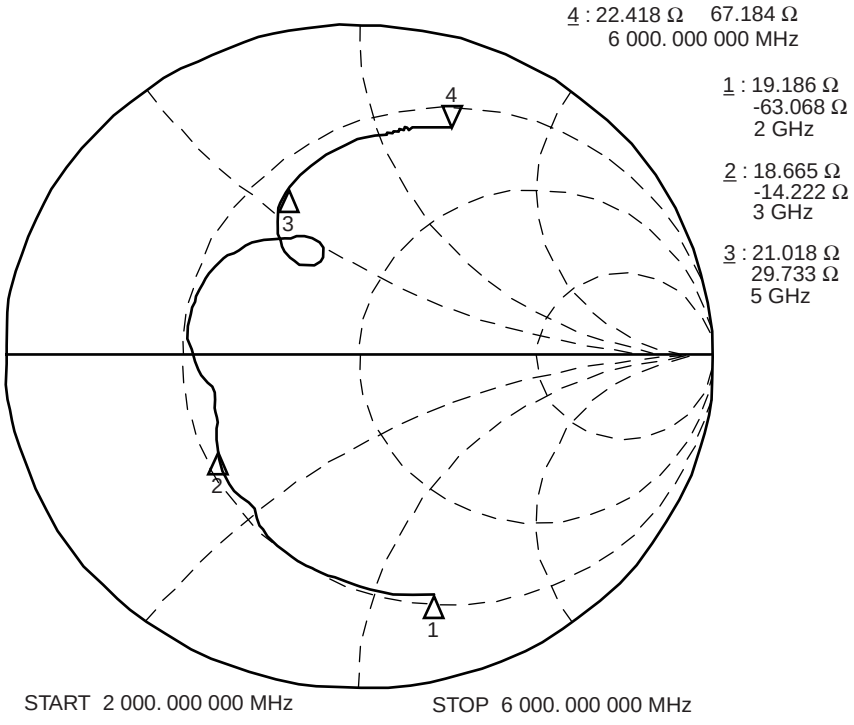


5. fin input impedance

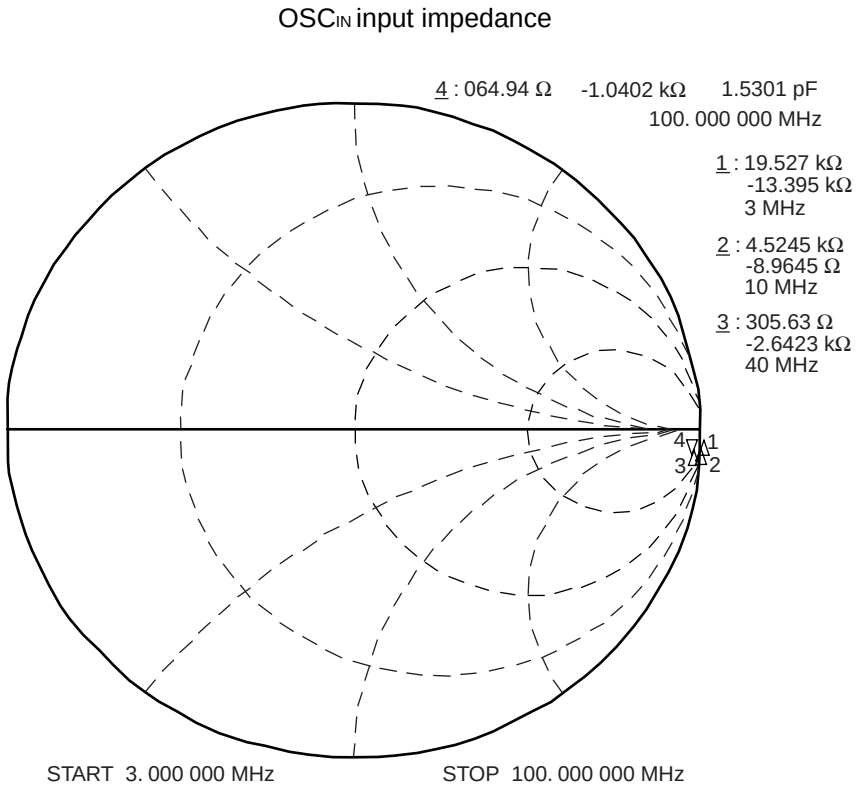
finIF input impedance



finRF input impedance



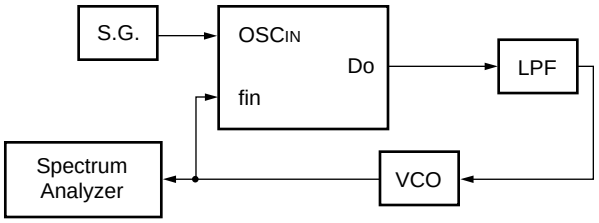
6. OSC_{IN} input impedance



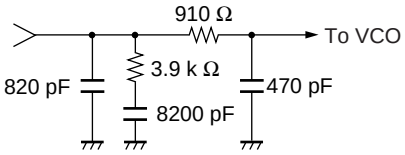
■ REFERENCE INFORMATION

(for Phase Noise and Reference Leakage)

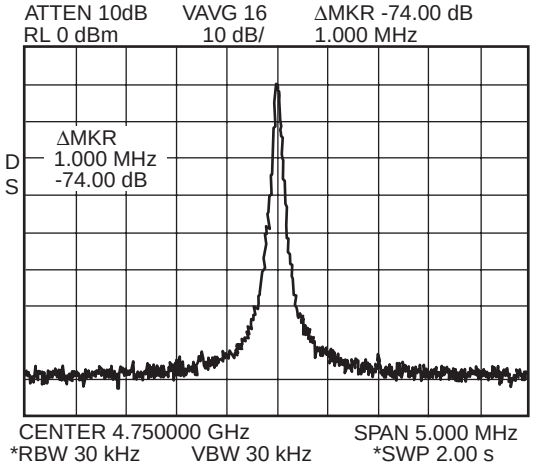
Test Circuit



f_{VCO} = 4750 MHz V_{CC} = 3.0 V Ta = + 25 °C
fr = 250 kHz (channel spacing = 1 MHz)
f_{OSC} = 13 MHz CP : 1.5 mA mode
LPF

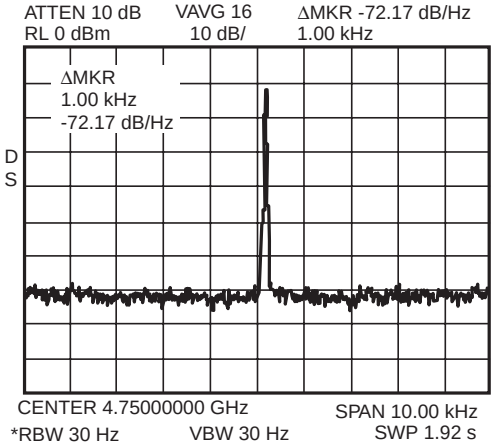


- PLL Reference Leakage

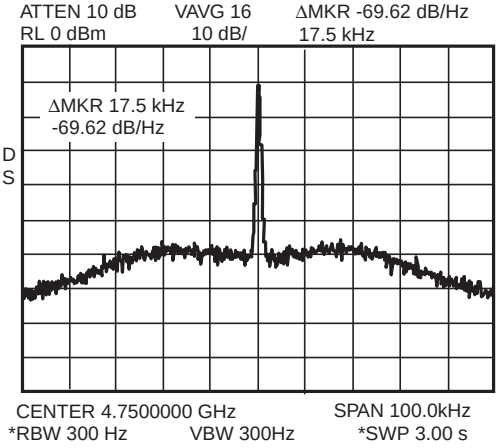


Reference Leak : -74.00 dBc

- PLL Phase Noise

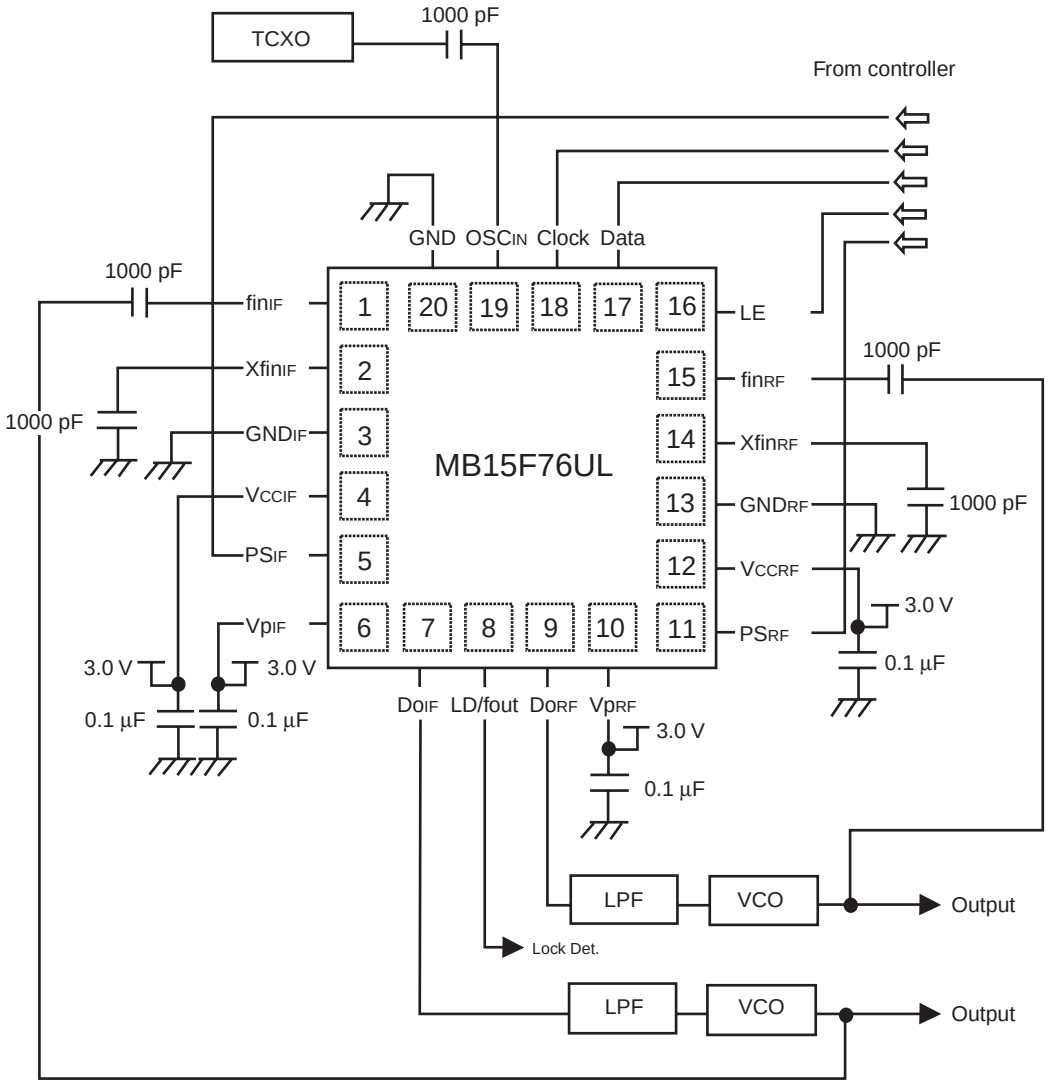


C/N Δ1 kHz : -72.17 dBc/Hz



C/N Peak : -69.62 dBc/Hz
BW : 33.5 kHz

■ APPLICATION EXAMPLE



Notes : Clock, Data, LE : The schmitt trigger circuit is provided (insert a pull-down or pull-up register to prevent oscillation when open-circuit in the input) .

■ USAGE PRECAUTIONS

(1) V_{CCRF}, Vp_{RF}, V_{CCIF} and Vp_{IF} must be equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CCRF}, Vp_{RF}, V_{CCIF} and Vp_{IF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

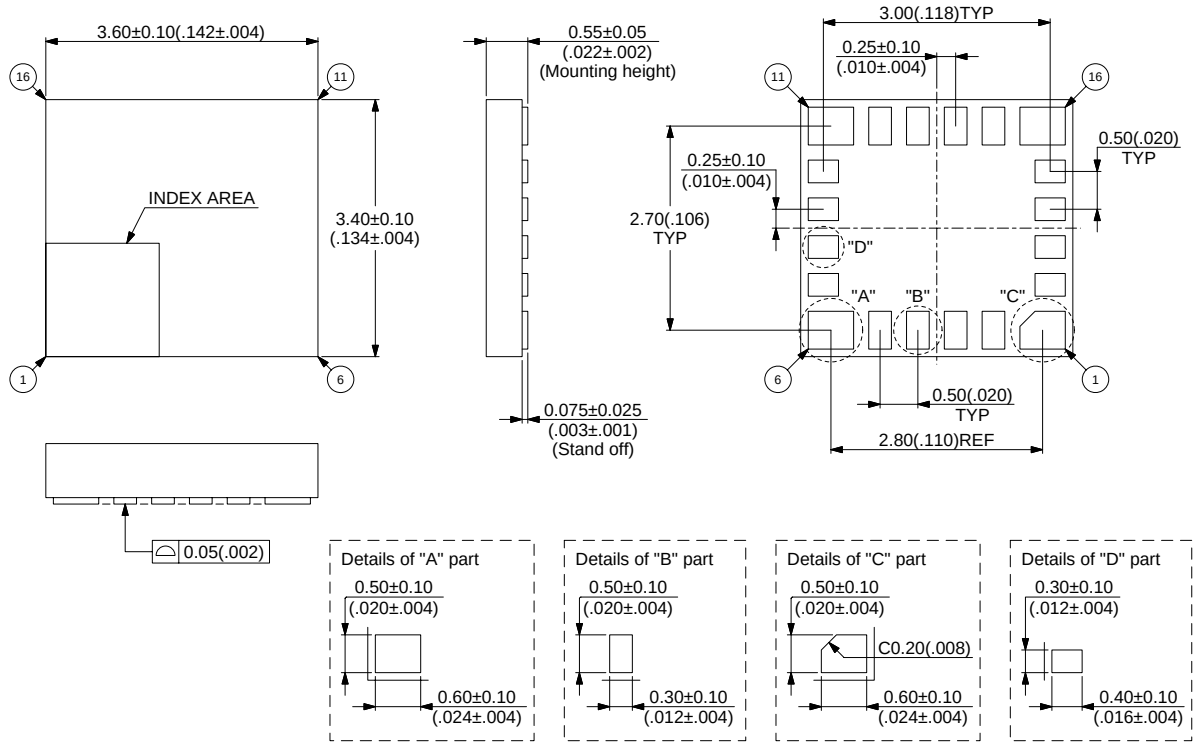
(2) To protect against damage by electrostatic discharge, note the following handling precautions :
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F76ULPVA	20-pad plastic BCC (LCC-20P-M05)	

■ PACKAGE DIMENSIONS

20-pad plastic BCC
(LCC-20P-M05)



Dimensions in mm (inches)

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