

# SDRAM Unbuffered Module

168pin Unbuffered Module based on 256Mb E-die  
62/72-bit Non ECC/ECC

Revision 1.4

May 2004

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## Revision History

### Revision 1.0 (June, 2003)

- First release

### Revision 1.1 (September, 2003)

- Corrected Typo

### Revision 1.2 (February, 2004)

- Corrected typo.

### Revision 1.3 (March, 2004)

- Modified DC Characteristics Notes.

### Revision 1.4 (May, 2004)

- Added Note 5. sentence of tRDL parameter

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## 168Pin Unbuffered DIMM based on 256Mb E-die (x8, x16)

### Ordering Information

| Part Number      | Density | Organization | Component Composition    | Component Package | Height   |
|------------------|---------|--------------|--------------------------|-------------------|----------|
| M366S1654ETS-C7A | 128MB   | 16M x 64     | 16Mx16(K4S561632E) * 4EA | 54-TSOP(II)       | 1,000mil |
| M366S3253ETS-C7A | 256MB   | 32M x 64     | 32Mx8(K4S560832E) * 8EA  |                   | 1,375mil |
| M366S3253ETU-C7A | 256MB   | 32M x 64     | 32Mx8(K4S560832E) * 8EA  |                   | 1,125mil |
| M374S3253ETS-C7A | 256MB   | 32M x 72     | 32Mx8(K4S560832E) * 9EA  |                   | 1,375mil |
| M374S3253ETU-C7A | 256MB   | 32M x 72     | 32Mx8(K4S560832E) * 9EA  |                   | 1,125mil |
| M366S6453ETS-C7A | 512MB   | 64M x 64     | 32Mx8(K4S560832E)*16EA   |                   | 1,375mil |
| M366S6453ETU-C7A | 512MB   | 64M x 64     | 32Mx8(K4S560832E)*16EA   |                   | 1,125mil |
| M374S6453ETS-C7A | 512MB   | 64M x 72     | 32Mx8(K4S560832E)*18EA   |                   | 1,375mil |
| M374S6453ETU-C7A | 512MB   | 64M x 72     | 32Mx8(K4S560832E)*18EA   |                   | 1,125mil |

### Operating Frequencies

|                         | 7A            |              |
|-------------------------|---------------|--------------|
|                         | @CL3          | @CL2         |
| Maximum Clock Frequency | 133MHz(7.5ns) | 100MHz(10ns) |
| CL-tRCD-tRP(clock)      | 3 - 3 - 3     | 2 - 2 - 2    |

### Feature

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs Latency (Access from column address)  
Burst length (1, 2, 4, 8 & Full page)  
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM

## PIN CONFIGURATIONS (Front side/back side)

| Pin | Front | Pin | Front  | Pin | Front  | Pin | Back | Pin | Back   | Pin | Back   |
|-----|-------|-----|--------|-----|--------|-----|------|-----|--------|-----|--------|
| 1   | VSS   | 29  | DQM1   | 57  | DQ18   | 85  | VSS  | 113 | DQM5   | 141 | DQ50   |
| 2   | DQ0   | 30  | **CS0  | 58  | DQ19   | 86  | DQ32 | 114 | **CS1  | 142 | DQ51   |
| 3   | DQ1   | 31  | DU     | 59  | VDD    | 87  | DQ33 | 115 | RAS    | 143 | VDD    |
| 4   | DQ2   | 32  | VSS    | 60  | DQ20   | 88  | DQ34 | 116 | VSS    | 144 | DQ52   |
| 5   | DQ3   | 33  | A0     | 61  | NC     | 89  | DQ35 | 117 | A1     | 145 | NC     |
| 6   | VDD   | 34  | A2     | 62  | *VREF  | 90  | VDD  | 118 | A3     | 146 | *VREF  |
| 7   | DQ4   | 35  | A4     | 63  | **CKE1 | 91  | DQ36 | 119 | A5     | 147 | REGE   |
| 8   | DQ5   | 36  | A6     | 64  | VSS    | 92  | DQ37 | 120 | A7     | 148 | VSS    |
| 9   | DQ6   | 37  | A8     | 65  | DQ21   | 93  | DQ38 | 121 | A9     | 149 | DQ53   |
| 10  | DQ7   | 38  | A10/AP | 66  | DQ22   | 94  | DQ39 | 122 | BA0    | 150 | DQ54   |
| 11  | DQ8   | 39  | BA1    | 67  | DQ23   | 95  | DQ40 | 123 | A11    | 151 | DQ55   |
| 12  | VSS   | 40  | VDD    | 68  | VSS    | 96  | VSS  | 124 | VDD    | 152 | VSS    |
| 13  | DQ9   | 41  | VDD    | 69  | DQ24   | 97  | DQ41 | 125 | **CLK1 | 153 | DQ56   |
| 14  | DQ10  | 42  | **CLK0 | 70  | DQ25   | 98  | DQ42 | 126 | A12    | 154 | DQ57   |
| 15  | DQ11  | 43  | VSS    | 71  | DQ26   | 99  | DQ43 | 127 | VSS    | 155 | DQ58   |
| 16  | DQ12  | 44  | DU     | 72  | DQ27   | 100 | DQ44 | 128 | **CKE0 | 156 | DQ59   |
| 17  | DQ13  | 45  | **CS2  | 73  | VDD    | 101 | DQ45 | 129 | **CS3  | 157 | VDD    |
| 18  | VDD   | 46  | DQM2   | 74  | DQ28   | 102 | VDD  | 130 | DQM6   | 158 | DQ60   |
| 19  | DQ14  | 47  | DQM3   | 75  | DQ29   | 103 | DQ46 | 131 | DQM7   | 159 | DQ61   |
| 20  | DQ15  | 48  | DU     | 76  | DQ30   | 104 | DQ47 | 132 | *A13   | 160 | DQ62   |
| 21  | CB0   | 49  | VDD    | 77  | DQ31   | 105 | CB4  | 133 | VDD    | 161 | DQ63   |
| 22  | CB1   | 50  | NC     | 78  | VSS    | 106 | CB5  | 134 | NC     | 162 | VSS    |
| 23  | VSS   | 51  | NC     | 79  | **CLK2 | 107 | VSS  | 135 | NC     | 163 | **CLK3 |
| 24  | NC    | 52  | CB2    | 80  | NC     | 108 | NC   | 136 | CB6    | 164 | NC     |
| 25  | NC    | 53  | CB3    | 81  | NC     | 109 | NC   | 137 | CB7    | 165 | SA0    |
| 26  | VDD   | 54  | VSS    | 82  | SDA    | 110 | VDD  | 138 | VSS    | 166 | SA1    |
| 27  | WE    | 55  | DQ16   | 83  | SCL    | 111 | CAS  | 139 | DQ48   | 167 | SA2    |
| 28  | DQM0  | 56  | DQ17   | 84  | VDD    | 112 | DQM4 | 140 | DQ49   | 168 | VDD    |

Note : 1. \* These pins are not used in this module.

2. Pins 82,83,165,166,167 should be NC in the system which does not support SPD.

3. Pins 21,22,52,53,105,106,136,137 are used only ECC(x72) Module.

4. \*\* About these pins, Refer to the Block Diagram of each.

## Pin Description

| Pin Name   | Function                     | Pin Name | Function                   |
|------------|------------------------------|----------|----------------------------|
| A0 ~ A12   | Address input (Multiplexed)  | DQM0 ~ 7 | DQM                        |
| BA0 ~ BA1  | Select bank                  | VDD      | Power supply (3.3V)        |
| DQ0 ~ DQ63 | Data input/output            | VSS      | Ground                     |
| CB0 ~ CB7  | Check bit (Data-in/data-out) | VREF     | Power supply for reference |
| CLK0 ~ 3   | Clock input                  | REGE     | Register enable            |
| CKE0, CKE1 | Clock enable input           | SDA      | Serial data I/O            |
| CS0 ~ CS3  | Chip select input            | SCL      | Serial clock               |
| RAS        | Row address strobe           | SA0 ~ 2  | Address in EEPROM          |
| CAS        | Column address strobe        | DU       | Don't use                  |
| WE         | Write enable                 | NC       | No connection              |

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## PIN CONFIGURATION DESCRIPTION

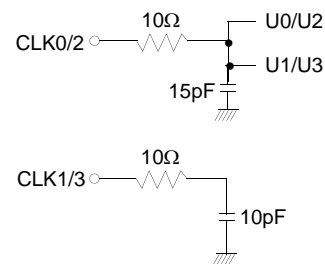
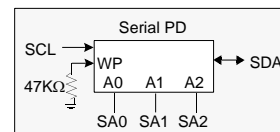
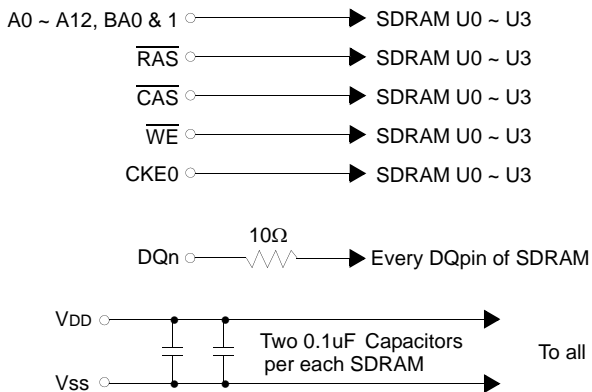
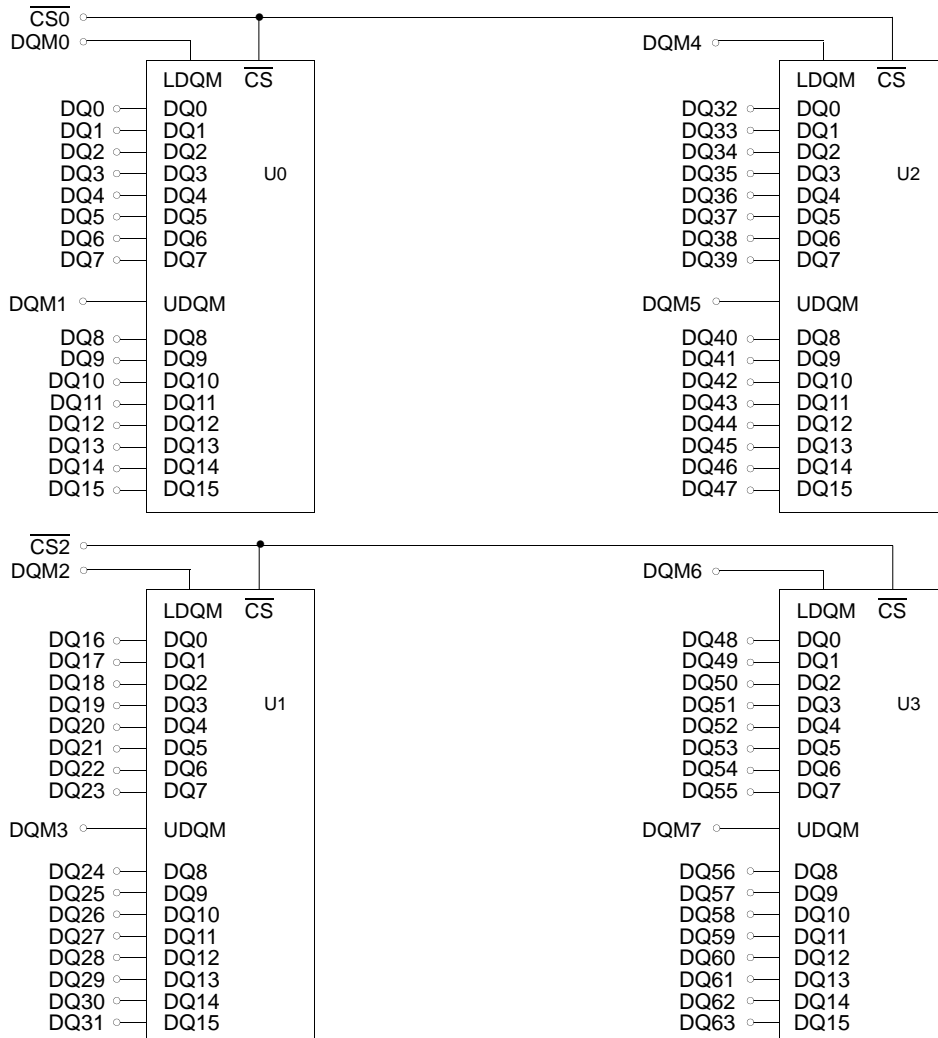
| Pin                     | Name                          | Input Function   |
|-------------------------|-------------------------------|--|
| CLK                     | <i>System clock</i>           | Active on the positive going edge to sample all inputs.  |
| $\overline{\text{CS}}$  | <i>Chip select</i>            | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM   |
| CKE                     | <i>Clock enable</i>           | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.   |
| A0 ~ A12                | <i>Address</i>                | Row/column addresses are multiplexed on the same pins.<br>Row address : RA0 ~ RA12<br>Column address : (x8 : CA0 ~ CA9), (x16 : CA0 ~ CA8)   |
| BA0 ~ BA1               | <i>Bank select address</i>    | Selects bank to be activated during row address latch time.<br>Selects bank for read/write during column address latch time.   |
| $\overline{\text{RAS}}$ | <i>Row address strobe</i>     | Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.  |
| $\overline{\text{CAS}}$ | <i>Column address strobe</i>  | Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.  |
| $\overline{\text{WE}}$  | <i>Write enable</i>           | Enables write operation and row precharge.<br>Latches data in starting from $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ active.   |
| DQM0 ~ 7                | <i>Data input/output mask</i> | Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)   |
| REGE                    | <i>Register enable</i>        | The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode. |
| DQ0 ~ 63                | <i>Data input/output</i>      | Data inputs/outputs are multiplexed on the same pins.  |
| CB0 ~ 7                 | <i>Check bit</i>              | Check bits for ECC.  |
| VDD/VSS                 | <i>Power supply/ground</i>    | Power and ground for the input buffers and the core logic.   |

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

128MB, 16Mx64 Module (M366S1654ETS) (Populated as 1 bank of x16 SDRAM Module)

## FUNCTIONAL BLOCK DIAGRAM

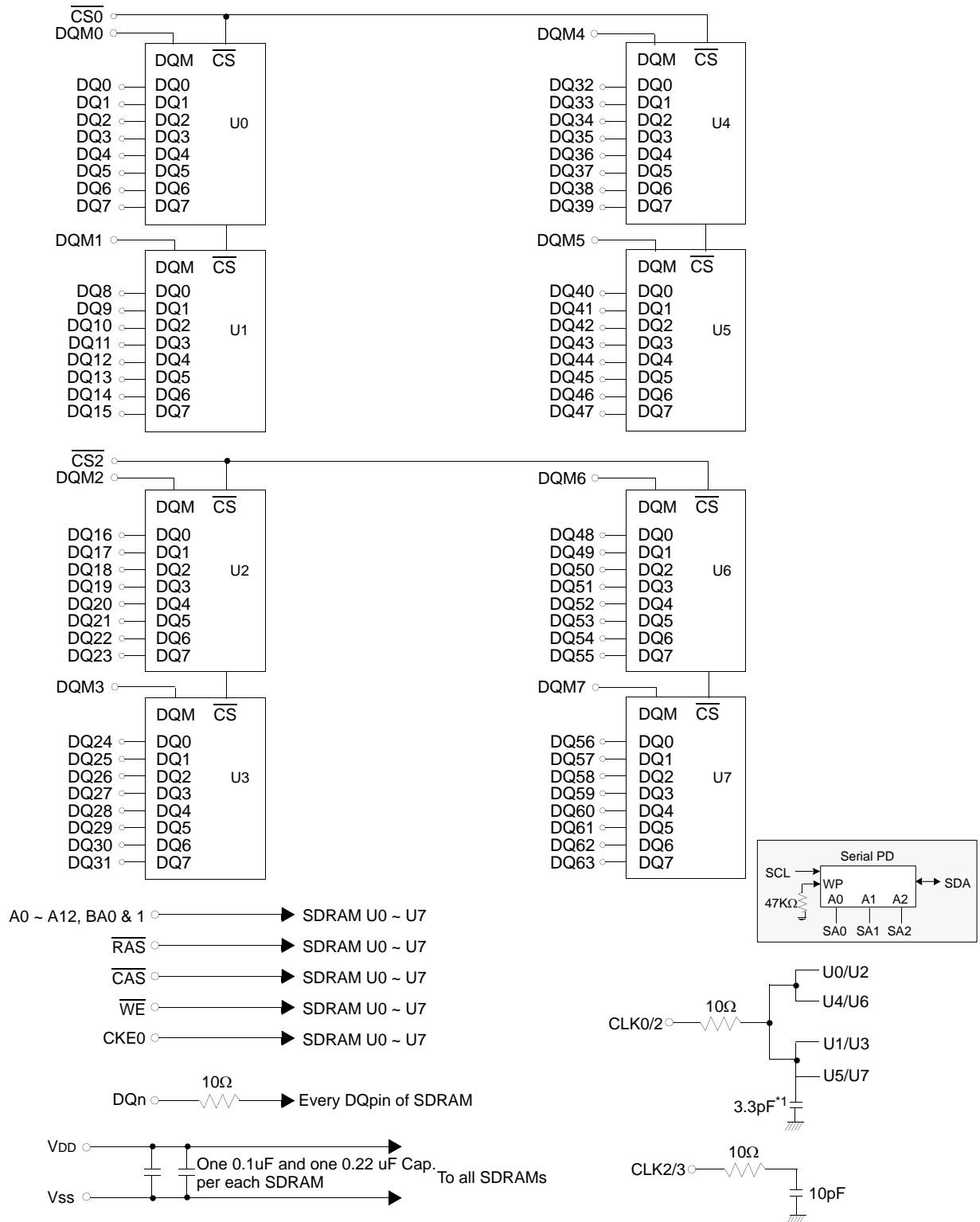


# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

256MB, 32Mx64 Non ECC Module(M366S3253ETS(U))(Populated as 1 bank of x8 SDRAM Module)

## FUNCTIONAL BLOCK DIAGRAM



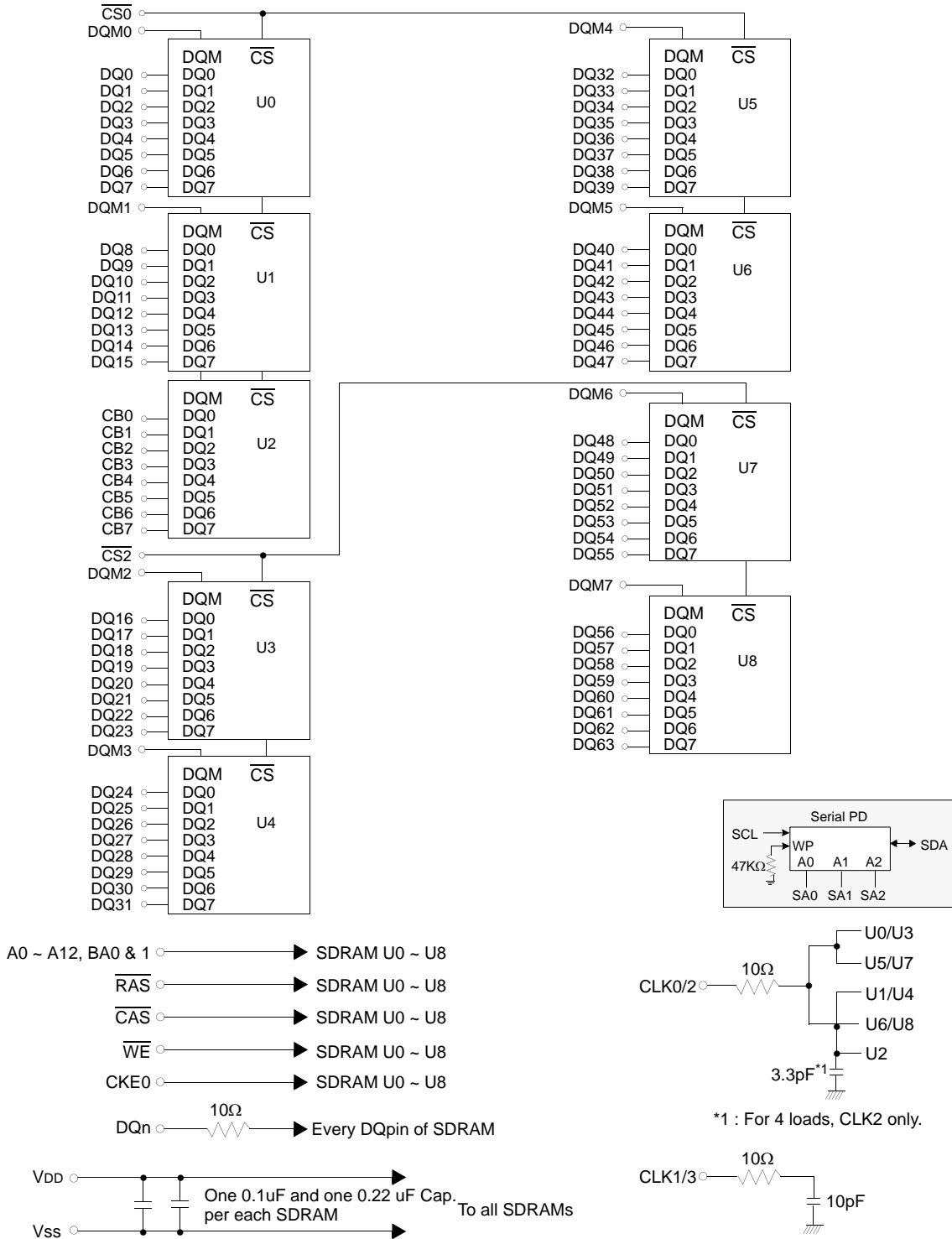
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# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## 256MB, 32Mx72 ECC Module (M374S3253ETS(U)) (Populated as 1 bank of x8 SDRAM Module) FUNCTIONAL BLOCK DIAGRAM

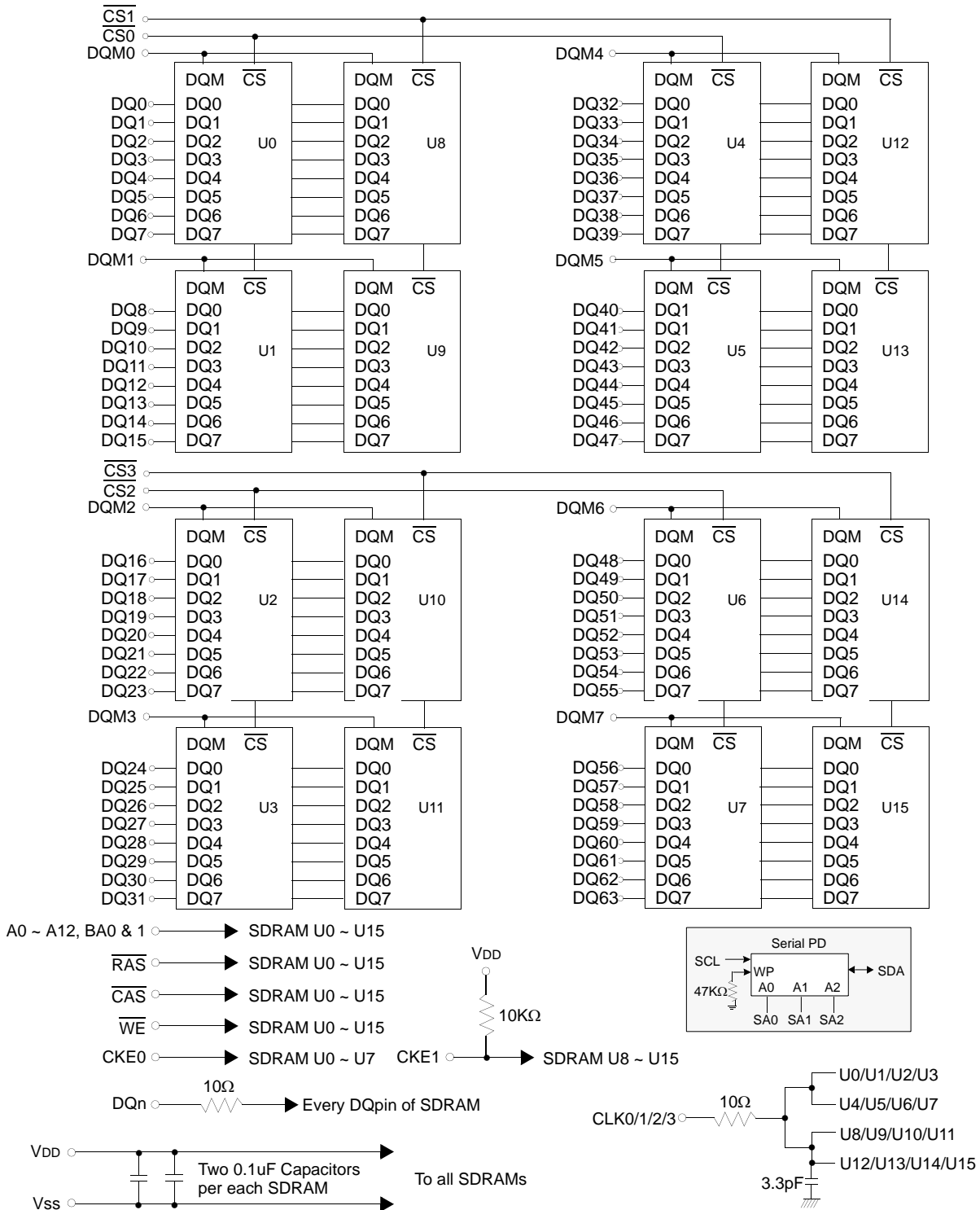




# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

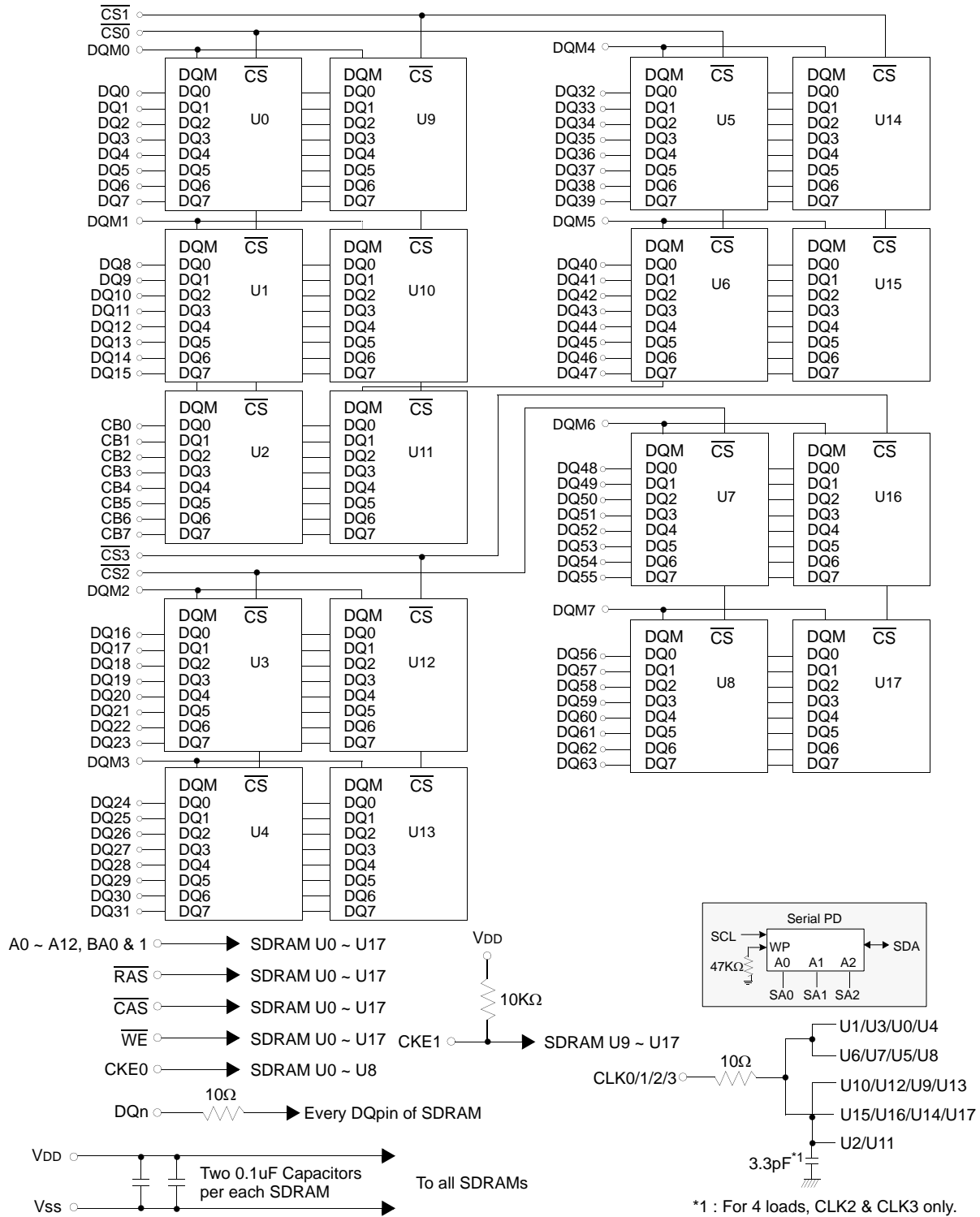
## 512MB, 64Mx64 Non ECC Module (M366S6453ETS(U)) (Populated as 2 bank of x8 SDRAM Module) FUNCTIONAL BLOCK DIAGRAM



# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## 512MB, 64Mx72 ECC Module (M374S6453ETS(U)) (Populated as 2 bank of x8 SDRAM Module) FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter   | Symbol                             | Value                | Unit |
|---|------------------------------------|----------------------|------|
| Voltage on any pin relative to V <sub>SS</sub>                | V <sub>IN</sub> , V <sub>OUT</sub> | -1.0 ~ 4.6           | V    |
| Voltage on V <sub>DD</sub> supply relative to V <sub>SS</sub> | V <sub>DD</sub> , V <sub>DDQ</sub> | -1.0 ~ 4.6           | V    |
| Storage temperature   | T <sub>STG</sub>                   | -55 ~ +150           | °C   |
| Power dissipation   | P <sub>D</sub>                     | 1.0 * # of component | W    |
| Short circuit current   | I <sub>OS</sub>                    | 50                   | mA   |

**Note :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70°C)

| Parameter             | Symbol          | Min  | Typ | Max                   | Unit | Note                   |
|-----------------------|-----------------|------|-----|-----------------------|------|------------------------|
| Supply voltage        | V <sub>DD</sub> | 3.0  | 3.3 | 3.6                   | V    |                        |
| Input high voltage    | V <sub>IH</sub> | 2.0  | 3.0 | V <sub>DDQ</sub> +0.3 | V    | 1                      |
| Input low voltage     | V <sub>IL</sub> | -0.3 | 0   | 0.8                   | V    | 2                      |
| Output high voltage   | V <sub>OH</sub> | 2.4  | -   | -                     | V    | I <sub>OH</sub> = -2mA |
| Output low voltage    | V <sub>OL</sub> | -    | -   | 0.4                   | V    | I <sub>OL</sub> = 2mA  |
| Input leakage current | I <sub>LI</sub> | -10  | -   | 10                    | uA   | 3                      |

**Notes :** 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V ± 200 mV)

| Parameter  | Sym-<br>bol      | M366S1654ETS |     | M366S3253ETS(U) |     | M366S6453ETS(U) |     | Unit |
|--|------------------|--------------|-----|-----------------|-----|-----------------|-----|------|
|  |                  | Min          | Max | Min             | Max | Min             | Max |      |
| Input capacitance (A <sub>0</sub> ~ A <sub>11</sub> )  | C <sub>IN1</sub> | 15           | 25  | 25              | 45  | 45              | 85  | pF   |
| Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ ) | C <sub>IN2</sub> | 15           | 25  | 25              | 45  | 45              | 85  | pF   |
| Input capacitance (CKE)  | C <sub>IN3</sub> | 15           | 25  | 25              | 45  | 25              | 45  | pF   |
| Input capacitance (CLK)  | C <sub>IN4</sub> | 10           | 13  | 15              | 21  | 15              | 21  | pF   |
| Input capacitance ( $\overline{\text{CS}}$ )   | C <sub>IN5</sub> | 10           | 15  | 15              | 25  | 15              | 25  | pF   |
| Input capacitance (DQM <sub>0</sub> ~ DQM <sub>7</sub> )   | C <sub>IN6</sub> | 8            | 10  | 8               | 12  | 10              | 15  | pF   |
| Data input/output capacitance (DQ <sub>0</sub> ~ DQ <sub>63</sub> )                              | C <sub>OUT</sub> | 9            | 12  | 9               | 12  | 13              | 18  | pF   |

| Pin  | Sym-<br>bol      | M374S3253ETS(U) |     | M374S6453ETS(U) |     | Unit |
|--|------------------|-----------------|-----|-----------------|-----|------|
|  |                  | Min             | Max | Min             | Max |      |
| Input capacitance (A <sub>0</sub> ~ A <sub>11</sub> )  | C <sub>IN1</sub> | 28              | 50  | 50              | 95  | pF   |
| Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ ) | C <sub>IN2</sub> | 28              | 50  | 50              | 95  | pF   |
| Input capacitance (CKE)  | C <sub>IN3</sub> | 28              | 50  | 28              | 50  | pF   |
| Input capacitance (CLK)  | C <sub>IN4</sub> | 18              | 25  | 18              | 25  | pF   |
| Input capacitance ( $\overline{\text{CS}}$ )   | C <sub>IN5</sub> | 18              | 30  | 18              | 30  | pF   |
| Input capacitance (DQM <sub>0</sub> ~ DQM <sub>7</sub> )   | C <sub>IN6</sub> | 8               | 10  | 13              | 20  | pF   |
| Data input/output capacitance (DQ <sub>0</sub> ~ DQ <sub>63</sub> )                              | C <sub>OUT</sub> | 9               | 12  | 13              | 18  | pF   |

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## DC CHARACTERISTICS

### M366S1654ETS (16M x 64, 128MB Module)

(Recommended operating condition unless otherwise noted,  $T_A = 0$  to  $70^\circ\text{C}$ )

| Parameter   | Symbol             | Test Condition   | Version | Unit | Note |
|---|--------------------|--|---------|------|------|
|   |                    |  | 7A      |      |      |
| Operating current<br>(One bank active)                                | I <sub>CC1</sub>   | Burst length = 1<br>$t_{RC} \geq t_{RC}(\text{min})$<br>$I_O = 0$ mA   | 360     | mA   | 1    |
| Precharge standby current<br>in power-down mode                       | I <sub>CC2P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 8       | mA   |      |
|   | I <sub>CC2PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 8       |      |      |
| Precharge standby current<br>in non power-down mode                   | I <sub>CC2N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 80      | mA   |      |
|   | I <sub>CC2NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 40      |      |      |
| Active standby current in<br>power-down mode                          | I <sub>CC3P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 25      | mA   |      |
|   | I <sub>CC3PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 25      |      |      |
| Active standby current in<br>non power-down mode<br>(One bank active) | I <sub>CC3N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 100     | mA   |      |
|   | I <sub>CC3NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 100     |      |      |
| Operating current<br>(Burst mode)                                     | I <sub>CC4</sub>   | $I_O = 0$ mA<br>Page burst<br>4Banks activated<br>$t_{CCD} = 2\text{CLKs}$   | 520     | mA   | 1    |
| Refresh current   | I <sub>CC5</sub>   | $t_{RC} \geq t_{RC}(\text{min})$   | 720     | mA   | 2    |
| Self refresh current  | I <sub>CC6</sub>   | $\text{CKE} \leq 0.2\text{V}$  | 12      | mA   |      |

### M366S3253ETS(U) (32M x 64, 256MB Module)

(Recommended operating condition unless otherwise noted,  $T_A = 0$  to  $70^\circ\text{C}$ )

| Parameter   | Symbol             | Test Condition   | Version | Unit | Note |
|---|--------------------|--|---------|------|------|
|   |                    |  | 7A      |      |      |
| Operating current<br>(One bank active)                                | I <sub>CC1</sub>   | Burst length = 1<br>$t_{RC} \geq t_{RC}(\text{min})$<br>$I_O = 0$ mA   | 640     | mA   | 1    |
| Precharge standby current<br>in power-down mode                       | I <sub>CC2P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 16      | mA   |      |
|   | I <sub>CC2PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 16      |      |      |
| Precharge standby current<br>in non power-down mode                   | I <sub>CC2N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 160     | mA   |      |
|   | I <sub>CC2NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 80      |      |      |
| Active standby current in<br>power-down mode                          | I <sub>CC3P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 50      | mA   |      |
|   | I <sub>CC3PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 50      |      |      |
| Active standby current in<br>non power-down mode<br>(One bank active) | I <sub>CC3N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 200     | mA   |      |
|   | I <sub>CC3NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 200     |      |      |
| Operating current<br>(Burst mode)                                     | I <sub>CC4</sub>   | $I_O = 0$ mA<br>Page burst<br>4Banks activated<br>$t_{CCD} = 2\text{CLKs}$   | 800     | mA   | 1    |
| Refresh current   | I <sub>CC5</sub>   | $t_{RC} \geq t_{RC}(\text{min})$   | 1,440   | mA   | 2    |
| Self refresh current  | I <sub>CC6</sub>   | $\text{CKE} \leq 0.2\text{V}$  | 24      | mA   |      |

**Notes :** 1. Measured with outputs open.

2. Refresh period is 64ms.

3. Unless otherwise noted, input swing level is CMOS( $V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$ )

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## DC CHARACTERISTICS

### M374S3253ETS(U) (32M x 72, 256MB Module)

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

| Parameter   | Symbol             | Test Condition  | Version | Unit | Note |
|---|--------------------|---|---------|------|------|
|   |                    |   | 7A      |      |      |
| Operating current<br>(One bank active)                                | I <sub>CC1</sub>   | Burst length = 1<br>t <sub>RC</sub> ≥ t <sub>RC</sub> (min)<br>I <sub>O</sub> = 0 mA  | 720     | mA   | 1    |
| Precharge standby current<br>in power-down mode                       | I <sub>CC2P</sub>  | CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns   | 18      | mA   |      |
|   | I <sub>CC2PS</sub> | CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞  | 18      |      |      |
| Precharge standby current<br>in non power-down mode                   | I <sub>CC2N</sub>  | CKE ≥ V <sub>IH</sub> (min), CS ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns<br>Input signals are changed one time during 20ns | 180     | mA   |      |
|   | I <sub>CC2NS</sub> | CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞<br>Input signals are stable                         | 90      |      |      |
| Active standby current in<br>power-down mode                          | I <sub>CC3P</sub>  | CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns   | 54      | mA   |      |
|   | I <sub>CC3PS</sub> | CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞  | 54      |      |      |
| Active standby current in<br>non power-down mode<br>(One bank active) | I <sub>CC3N</sub>  | CKE ≥ V <sub>IH</sub> (min), CS ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns<br>Input signals are changed one time during 20ns | 225     | mA   |      |
|   | I <sub>CC3NS</sub> | CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞<br>Input signals are stable                         | 225     |      |      |
| Operating current<br>(Burst mode)                                     | I <sub>CC4</sub>   | I <sub>O</sub> = 0 mA<br>Page burst<br>4Banks activated<br>t <sub>CCD</sub> = 2CLKs   | 900     | mA   | 1    |
| Refresh current   | I <sub>CC5</sub>   | t <sub>RC</sub> ≥ t <sub>RC</sub> (min)   | 1,620   | mA   | 2    |
| Self refresh current  | I <sub>CC6</sub>   | CKE ≤ 0.2V  | 27      | mA   |      |

### M366S6453ETS(U) (64M x 64, 512MB Module)

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

| Parameter   | Symbol             | Test Condition  | Version | Unit | Note |
|---|--------------------|---|---------|------|------|
|   |                    |   | 7A      |      |      |
| Operating current<br>(One bank active)                                | I <sub>CC1</sub>   | Burst length = 1<br>t <sub>RC</sub> ≥ t <sub>RC</sub> (min)<br>I <sub>O</sub> = 0 mA  | 840     | mA   | 1    |
| Precharge standby current<br>in power-down mode                       | I <sub>CC2P</sub>  | CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns   | 32      | mA   |      |
|   | I <sub>CC2PS</sub> | CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞  | 32      |      |      |
| Precharge standby current<br>in non power-down mode                   | I <sub>CC2N</sub>  | CKE ≥ V <sub>IH</sub> (min), CS ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns<br>Input signals are changed one time during 20ns | 320     | mA   |      |
|   | I <sub>CC2NS</sub> | CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞<br>Input signals are stable                         | 160     |      |      |
| Active standby current in<br>power-down mode                          | I <sub>CC3P</sub>  | CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns   | 96      | mA   |      |
|   | I <sub>CC3PS</sub> | CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞  | 96      |      |      |
| Active standby current in<br>non power-down mode<br>(One bank active) | I <sub>CC3N</sub>  | CKE ≥ V <sub>IH</sub> (min), CS ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns<br>Input signals are changed one time during 20ns | 400     | mA   |      |
|   | I <sub>CC3NS</sub> | CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞<br>Input signals are stable                         | 400     |      |      |
| Operating current<br>(Burst mode)                                     | I <sub>CC4</sub>   | I <sub>O</sub> = 0 mA<br>Page burst<br>4Banks activated<br>t <sub>CCD</sub> = 2CLKs   | 1,000   | mA   | 1    |
| Refresh current   | I <sub>CC5</sub>   | t <sub>RC</sub> ≥ t <sub>RC</sub> (min)   | 1,620   | mA   | 2    |
| Self refresh current  | I <sub>CC6</sub>   | CKE ≤ 0.2V  | 48      | mA   |      |

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

3. Unless otherwise noted, input swing level is CMOS(V<sub>IH</sub>/V<sub>IL</sub>=V<sub>DDQ</sub>/V<sub>SSQ</sub>)

## DC CHARACTERISTICS

## M374S6453ETS(U) (64M x 72, 512MB Module)

(Recommended operating condition unless otherwise noted,  $T_A = 0$  to  $70^\circ\text{C}$ )

| Parameter   | Symbol             | Test Condition   | Version | Unit | Note |
|---|--------------------|--|---------|------|------|
|   |                    |  | 7A      |      |      |
| Operating current<br>(One bank active)                                | I <sub>CC1</sub>   | Burst length = 1<br>$t_{RC} \geq t_{RC}(\text{min})$<br>$I_O = 0$ mA   | 945     | mA   | 1    |
| Precharge standby current<br>in power-down mode                       | I <sub>CC2P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 36      | mA   |      |
|   | I <sub>CC2PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 36      |      |      |
| Precharge standby current<br>in non power-down mode                   | I <sub>CC2N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 360     | mA   |      |
|   | I <sub>CC2NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 180     |      |      |
| Active standby current in<br>power-down mode                          | I <sub>CC3P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 108     | mA   |      |
|   | I <sub>CC3PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 108     |      |      |
| Active standby current in<br>non power-down mode<br>(One bank active) | I <sub>CC3N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 450     | mA   |      |
|   | I <sub>CC3NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 450     |      |      |
| Operating current<br>(Burst mode)                                     | I <sub>CC4</sub>   | $I_O = 0$ mA<br>Page burst<br>4Banks activated<br>$t_{CCD} = 2\text{CLKs}$   | 1,125   | mA   | 1    |
| Refresh current   | I <sub>CC5</sub>   | $t_{RC} \geq t_{RC}(\text{min})$   | 1,845   | mA   | 2    |
| Self refresh current  | I <sub>CC6</sub>   | $\text{CKE} \leq 0.2\text{V}$  | 54      | mA   |      |

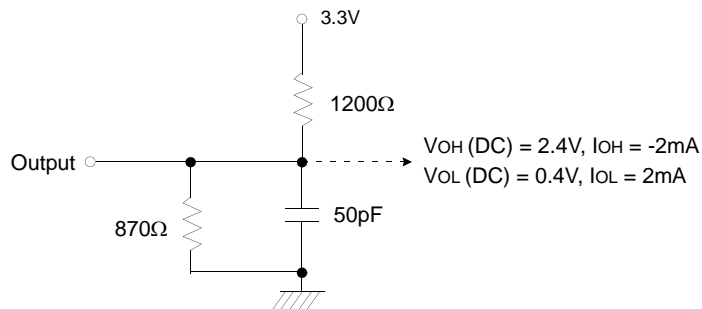
**Notes :** 1. Measured with outputs open.

2. Refresh period is 64ms.

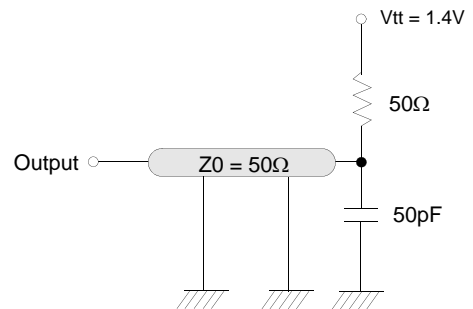
3. Unless otherwise noted, input swing level is CMOS( $V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$ )

## AC OPERATING TEST CONDITIONS (V<sub>DD</sub> = 3.3V ± 0.3V, T<sub>A</sub> = 0 to 70°C)

| Parameter   | Value       | Unit |
|---|-------------|------|
| AC input levels (V <sub>ih</sub> /V <sub>il</sub> ) | 2.4/0.4     | V    |
| Input timing measurement reference level            | 1.4         | V    |
| Input rise and fall time                            | tr/tf = 1/1 | ns   |
| Output timing measurement reference level           | 1.4         | V    |
| Output load condition                               | See Fig. 2  |      |



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

## OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| Parameter  | Symbol                 | Version                 | Unit | Note |
|--|------------------------|-------------------------|------|------|
|  |                        | 7A                      |      |      |
| Row active to row active delay                           | t <sub>RRD</sub> (min) | 15                      | ns   | 1    |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay | t <sub>RCD</sub> (min) | 20                      | ns   | 1    |
| Row precharge time                                       | t <sub>RP</sub> (min)  | 20                      | ns   | 1    |
| Row active time  | t <sub>RAS</sub> (min) | 45                      | ns   | 1    |
|  | t <sub>RAS</sub> (max) | 100                     | us   |      |
| Row cycle time   | t <sub>RC</sub> (min)  | 65                      | ns   | 1    |
| Last data in to row precharge                            | t <sub>RDL</sub> (min) | 2                       | CLK  | 2,5  |
| Last data in to Active delay                             | t <sub>DAL</sub> (min) | 2 CLK + t <sub>RP</sub> | -    | 5    |
| Last data in to new col. address delay                   | t <sub>CDL</sub> (min) | 1                       | CLK  | 2    |
| Last data in to burst stop                               | t <sub>BDL</sub> (min) | 1                       | CLK  | 2    |
| Col. address to col. address delay                       | t <sub>CCD</sub> (min) | 1                       | CLK  | 3    |
| Number of valid output data                              | CAS latency=3          | 2                       | ea   | 4    |
|  | CAS latency=2          | 1                       |      |      |

- Notes :**
- The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  - Minimum delay is required to complete write.
  - All parts allow every cycle column address change.
  - In case of row precharge interrupt, auto precharge and read burst stop.
  - In 100MHz and below 100MHz operating conditions, t<sub>RDL</sub>=1CLK and t<sub>DAL</sub>=1CLK + 20ns is also supported. SAMSUNG recommends t<sub>RDL</sub>=2CLK and t<sub>DAL</sub>=2CLK + t<sub>RP</sub>.

**AC CHARACTERISTICS** (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

| Parameter                 |               | Symbol | 7A  |      | Unit | Note |
|---------------------------|---------------|--------|-----|------|------|------|
|                           |               |        | Min | Max  |      |      |
| CLK cycle time            | CAS latency=3 | tCC    | 7.5 | 1000 | ns   | 1    |
|                           | CAS latency=2 |        | 10  |      |      |      |
| CLK to valid output delay | CAS latency=3 | tSAC   |     | 5.4  | ns   | 1,2  |
|                           | CAS latency=2 |        |     | 6    |      |      |
| Output data hold time     | CAS latency=3 | tOH    | 3   |      | ns   | 2    |
|                           | CAS latency=2 |        | 3   |      |      |      |
| CLK high pulse width      |               | tCH    | 2.5 |      | ns   | 3    |
| CLK low pulse width       |               | tCL    | 2.5 |      | ns   | 3    |
| Input setup time          |               | tSS    | 1.5 |      | ns   | 3    |
| Input hold time           |               | tSH    | 0.8 |      | ns   | 3    |
| CLK to output in Low-Z    |               | tSLZ   | 1   |      | ns   | 2    |
| CLK to output in Hi-Z     | CAS latency=3 | tSHZ   |     | 5.4  | ns   |      |
|                           | CAS latency=2 |        |     | 6    |      |      |

- Notes :**
- Parameters depend on programmed CAS latency.
  - If clock rising time is longer than 1ns,  $(tr/2-0.5)ns$  should be added to the parameter.
  - Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, i.e.,  $[(tr + tf)/2-1]ns$  should be added to the parameter.



# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

| Command                            |                        | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | BA0,1   | A10/AP      | A0 ~ A9,<br>A11, A12 | Note |   |
|------------------------------------|------------------------|--------|------|-----------------|------------------|------------------|-----------------|-----|---------|-------------|----------------------|------|---|
| Register                           | Mode register set      | H      | X    | L               | L                | L                | L               | X   | OP code |             |                      | 1,2  |   |
| Refresh                            | Auto refresh           | H      | H    | L               | L                | L                | H               | X   | X       |             |                      | 3    |   |
|                                    | Entry                  |        | L    |                 |                  |                  |                 |     |         |             |                      | 3    |   |
|                                    | Self refresh           | Exit   | L    | H               | L                | H                | H               | H   | X       | X           |                      |      | 3 |
|                                    |                        |        |      |                 | H                | X                | X               | X   |         |             |                      |      | 3 |
| Bank active & row addr.            |                        | H      | X    | L               | L                | H                | H               | X   | V       | Row address |                      |      |   |
| Read & column address              | Auto precharge disable | H      | X    | L               | H                | L                | H               | X   | V       | L           | Column address       | 4    |   |
|                                    | Auto precharge enable  |        |      |                 |                  |                  |                 |     |         | H           |                      | 4,5  |   |
| Write & column address             | Auto precharge disable | H      | X    | L               | H                | L                | L               | X   | V       | L           | Column address       | 4    |   |
|                                    | Auto precharge enable  |        |      |                 |                  |                  |                 |     |         | H           |                      | 4,5  |   |
| Burst stop                         |                        | H      | X    | L               | H                | H                | L               | X   | X       |             |                      | 6    |   |
| Precharge                          | Bank selection         | H      | X    | L               | L                | H                | L               | X   | V       | L           | X                    |      |   |
|                                    | All banks              |        |      |                 |                  |                  |                 |     | X       | H           |                      |      |   |
| Clock suspend or active power down | Entry                  | H      | L    | H               | X                | X                | X               | X   | X       |             |                      |      |   |
|                                    |                        |        |      | L               | V                | V                | V               |     |         |             |                      |      |   |
| Precharge power down mode          | Entry                  | H      | L    | H               | X                | X                | X               | X   | X       |             |                      |      |   |
|                                    |                        |        |      | L               | H                | H                | H               |     |         |             |                      |      |   |
|                                    | Exit                   | L      | H    | H               | X                | X                | X               | X   |         |             |                      |      |   |
|                                    |                        |        |      | L               | V                | V                | V               |     |         |             |                      |      |   |
| DQM                                |                        | H      | X    |                 |                  |                  |                 | V   | X       |             | 7                    |      |   |
| No operation command               |                        | H      | X    | H               | X                | X                | X               | X   | X       |             |                      |      |   |
|                                    |                        |        |      | L               | H                | H                | H               |     |         |             |                      |      |   |

**Notes :** 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

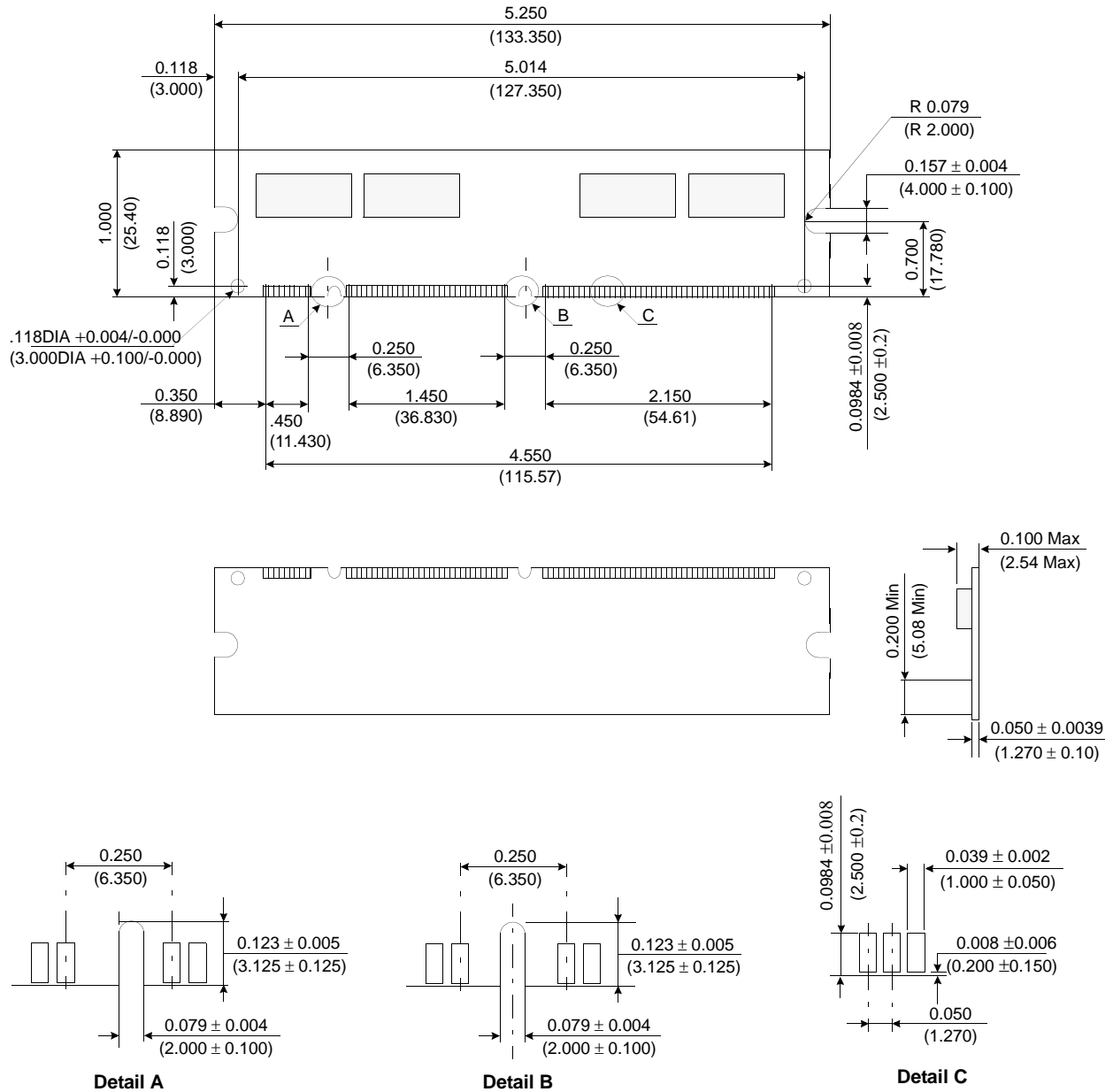
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## PACKAGE DIMENSIONS : 16Mx64 (M366S1654ETS)

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

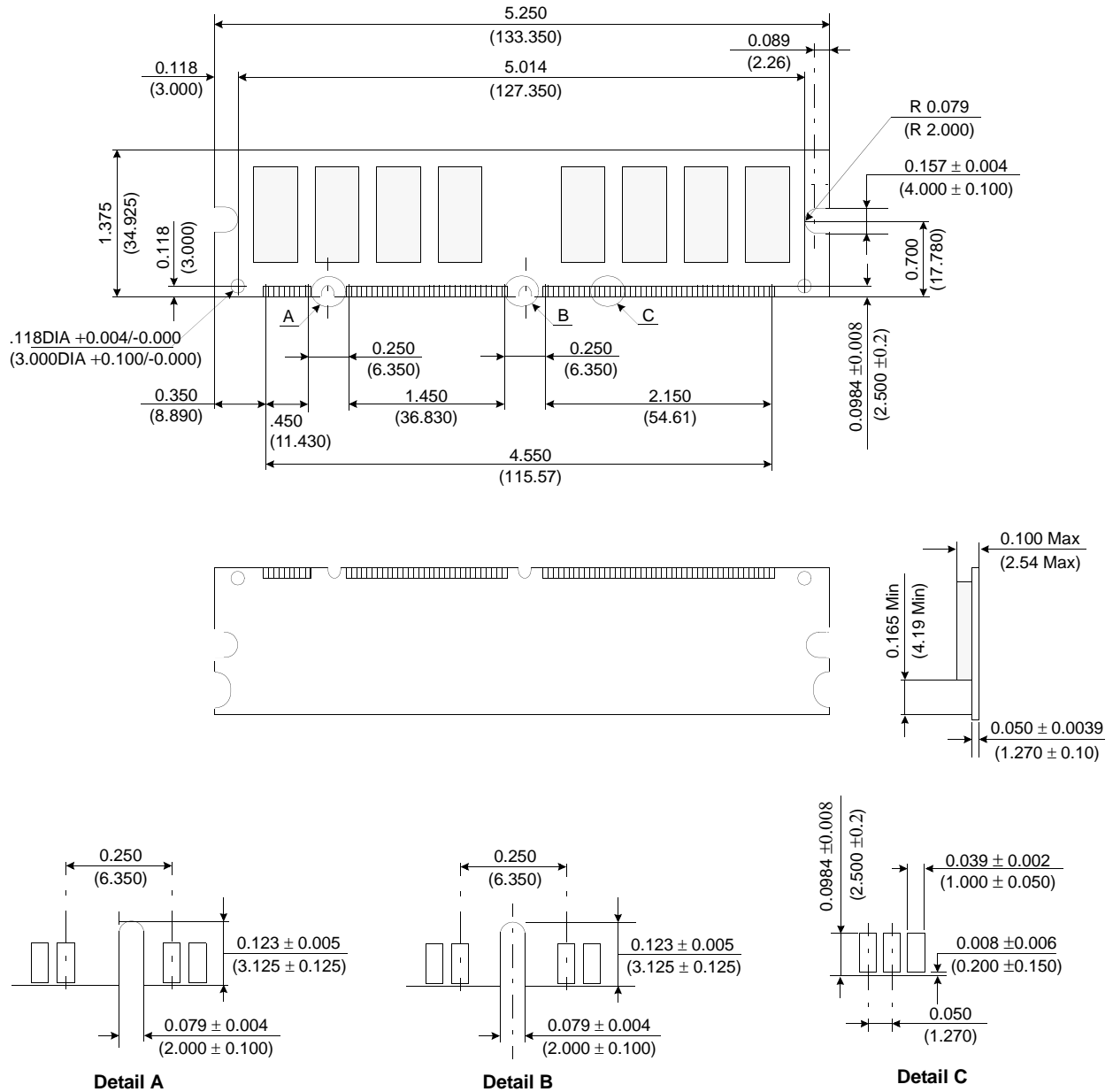
The used device is 16Mx16 SDRAM, TSOPII  
SDRAM Part No. : K4S561632E

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## PACKAGE DIMENSIONS : 32Mx64 (M366S3253ETS)

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

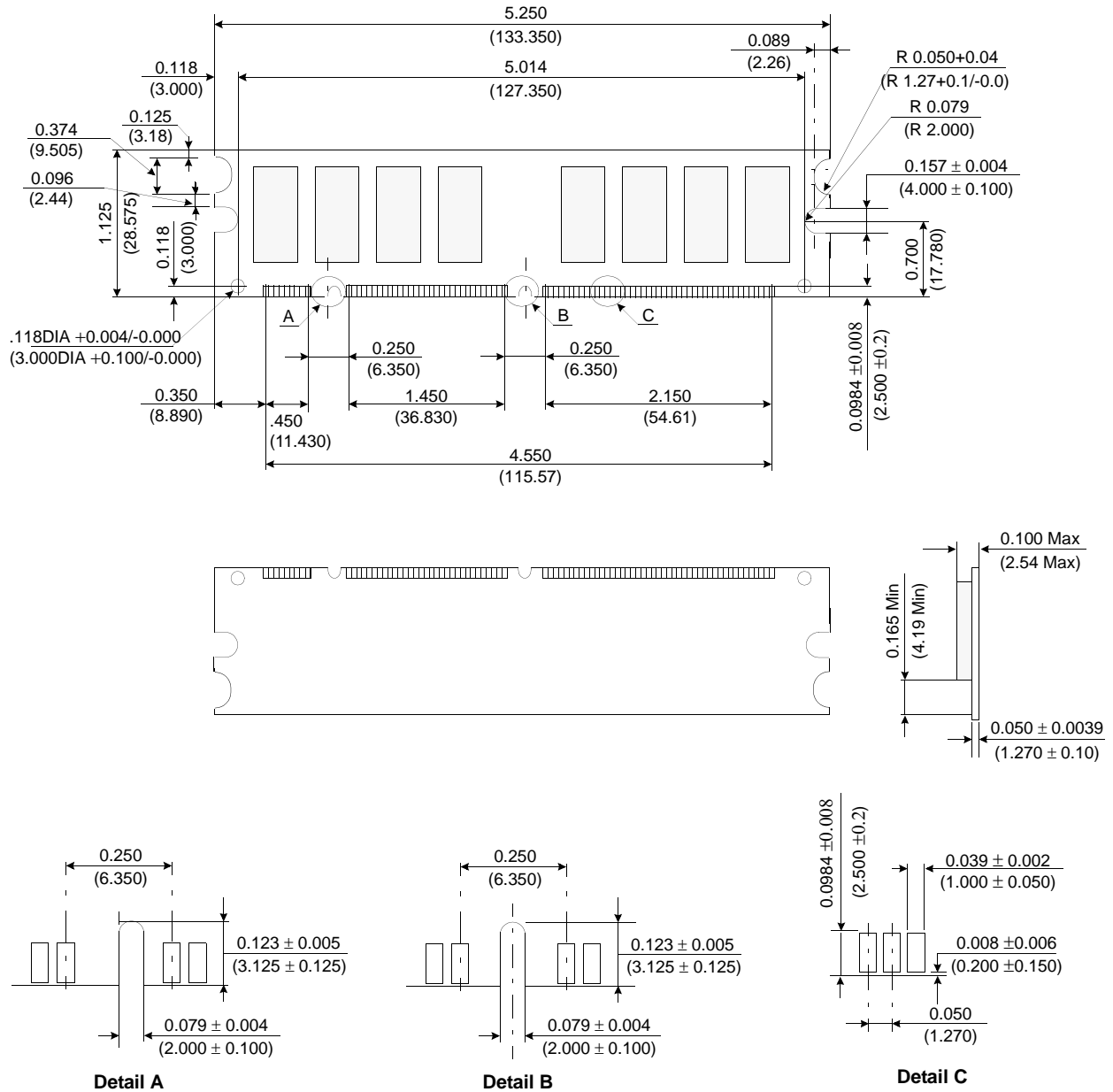
The used device is 32Mx8 SDRAM, TSOPII  
SDRAM Part No. : K4S560832E

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

## PACKAGE DIMENSIONS :32Mx64 (M366S3253ETU)

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

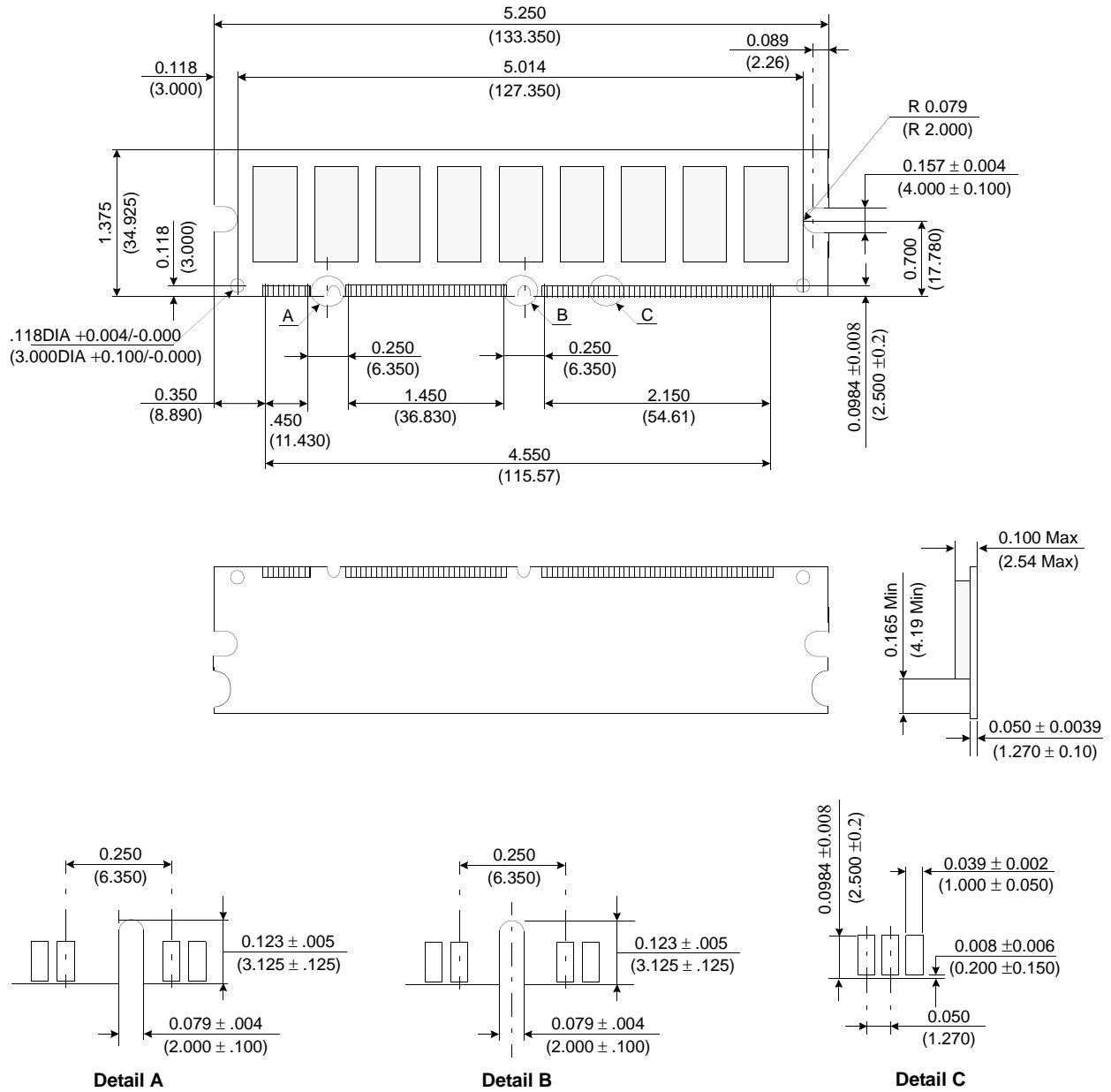
The used device is 32Mx8 SDRAM, TSOPII  
SDRAM Part No. : K4S560832E

# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

PACKAGE DIMENSIONS : 32Mx72 (M374S3253ETS)

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOPII  
SDRAM Part No. : K4S560832E

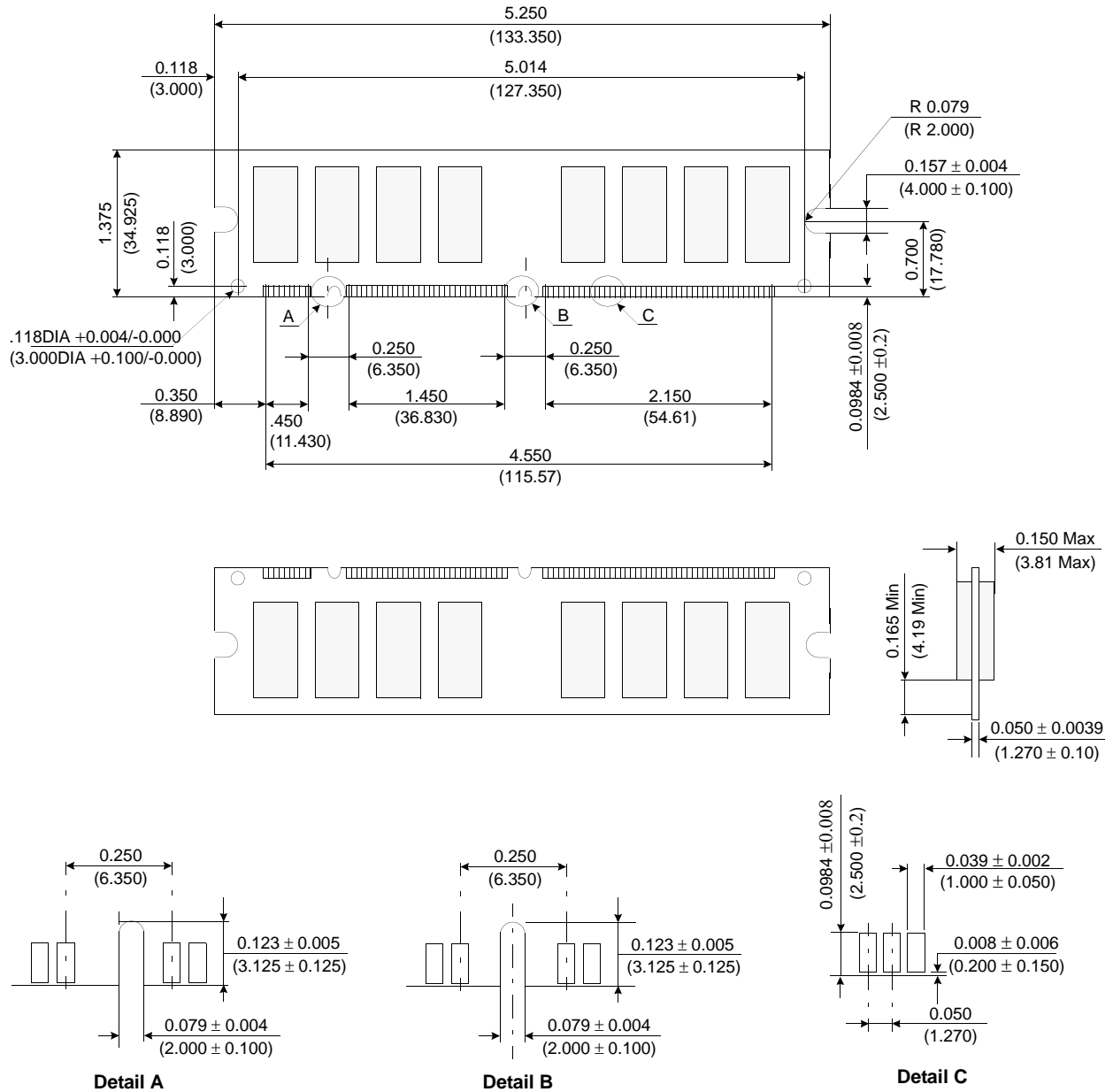


# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

PACKAGE DIMENSIONS : 64Mx64 (M366S6453ETS)

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOPII  
SDRAM Part No. : K4S560832E





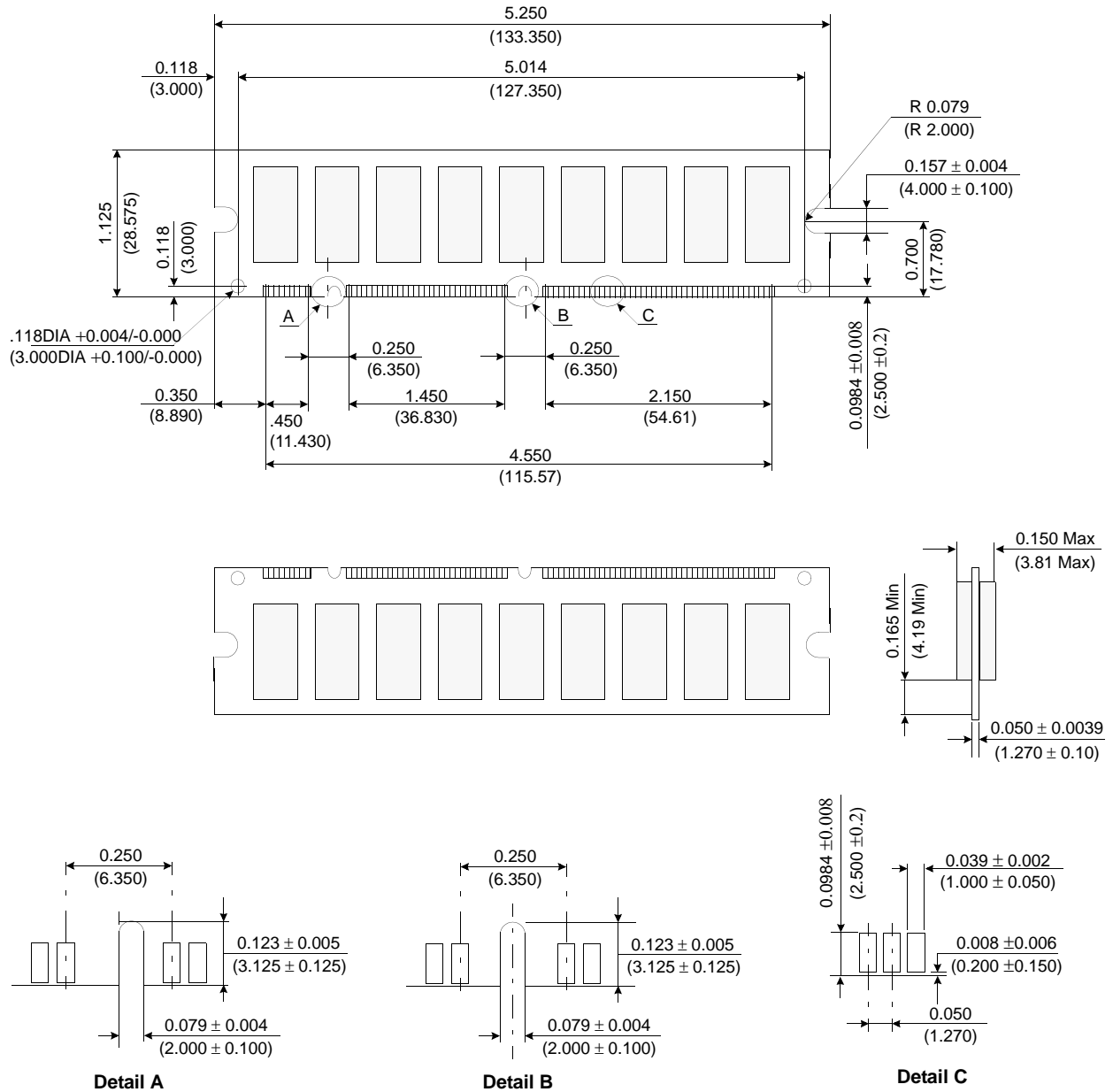


# 128MB, 256MB, 512MB Unbuffered DIMM

# SDRAM

PACKAGE DIMENSIONS : 64Mx72 (M374S6453ETU)

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOPII  
SDRAM Part No. : K4S560832E