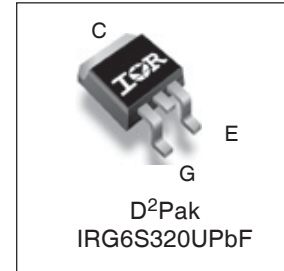
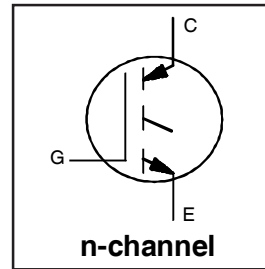


# IRG6S320UPbF

## Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low  $V_{CE(on)}$  and Energy per Pulse ( $E_{PULSE}^{TM}$ ) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
$V_{CE\ min}$	330	V
$V_{CE(ON)}\ typ.\ @\ I_C = 24A$	1.45	V
$I_{RP}\ max\ @\ T_C = 25^\circ C$	160	A
$T_J\ max$	150	$^\circ C$



G	C	E
Gate	Collector	Emitter

## Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low  $V_{CE(on)}$  and low  $E_{PULSE}^{TM}$  rating per silicon area which improve panel efficiency. Additional features are 150 $^\circ C$  operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

## Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{GE}$	Gate-to-Emitter Voltage	$\pm 30$	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	50 ④	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	25	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	160	
$P_D @ T_C = 25^\circ C$	Power Dissipation	114	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	45	
	Linear Derating Factor	0.91	W/ $^\circ C$
$T_J$	Operating Junction and	-40 to + 150	$^\circ C$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature for 10 seconds		

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	1.1	$^\circ C/W$

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{CES}$	Collector-to-Emitter Breakdown Voltage	330	—	—	V	$V_{GE} = 0V, I_{CE} = 500\mu A$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage <sup>③</sup>	30	—	—	V	$V_{GE} = 0V, I_{CE} = 1 A$
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.30	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_{CE} = 1\text{mA}$
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.20	—	V	$V_{GE} = 15V, I_{CE} = 12A$ <sup>③</sup>
		—	1.45	1.65		$V_{GE} = 15V, I_{CE} = 24A$ <sup>③</sup>
		—	1.95	—		$V_{GE} = 15V, I_{CE} = 48A$ <sup>③</sup>
		—	2.20	—		$V_{GE} = 15V, I_{CE} = 60A$ <sup>③</sup>
		—	2.26	—		$V_{GE} = 15V, I_{CE} = 48A, T_J = 150^\circ\text{C}$ <sup>③</sup>
$V_{GE(th)}$	Gate Threshold Voltage	2.6	—	5.0	V	$V_{CE} = V_{GE}, I_{CE} = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10	—	mV/ $^\circ\text{C}$	
$I_{CES}$	Collector-to-Emitter Leakage Current	—	1.0	10	$\mu A$	$V_{CE} = 330V, V_{GE} = 0V$
		—	5.0	—		$V_{CE} = 330V, V_{GE} = 0V, T_J = 100^\circ\text{C}$
		—	20	100		$V_{CE} = 330V, V_{GE} = 0V, T_J = 125^\circ\text{C}$
		—	75	—		$V_{CE} = 330V, V_{GE} = 0V, T_J = 150^\circ\text{C}$
$I_{GES}$	Gate-to-Emitter Forward Leakage	—	—	100	nA	$V_{GE} = 30V$
	Gate-to-Emitter Reverse Leakage	—	—	-100	nA	$V_{GE} = -30V$
$g_{fe}$	Forward Transconductance	—	28	—	S	$V_{CE} = 25V, I_{CE} = 12A$
$Q_g$	Total Gate Charge	—	46	—	nC	$V_{CE} = 200V, I_C = 12A, V_{GE} = 15V$ <sup>④</sup>
$Q_{gc}$	Gate-to-Collector Charge	—	7.7	—	nC	
$t_{d(on)}$	Turn-On delay time	—	24	—	ns	$I_C = 12A, V_{CC} = 196V$ $R_G = 10\Omega, L = 210\mu H, L_S = 150\text{nH}$ $T_J = 25^\circ\text{C}$
$t_r$	Rise time	—	20	—		
$t_{d(off)}$	Turn-Off delay time	—	89	—		
$t_f$	Fall time	—	70	—		
$t_{d(on)}$	Turn-On delay time	—	23	—	ns	$I_C = 12A, V_{CC} = 196V$ $R_G = 10\Omega, L = 200\mu H, L_S = 150\text{nH}$ $T_J = 150^\circ\text{C}$
$t_r$	Rise time	—	52	—		
$t_{d(off)}$	Turn-Off delay time	—	130	—		
$t_f$	Fall time	—	140	—		
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{CC} = 240V, V_{GE} = 15V, R_G = 5.1\Omega$
$E_{PULSE}$	Energy per Pulse	—	240	—	$\mu J$	$L = 220\text{nH}, C = 0.10\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$
		—	280	—		$L = 220\text{nH}, C = 0.10\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$
ESD	Human Body Model	Class 2 (Per JEDEC standard JESD22-A114)				
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)				
$C_{ies}$	Input Capacitance	—	1160	—	pF	$V_{GE} = 0V$ $V_{CE} = 30V$ $f = 1.0\text{MHz}$ , See Fig.13
$C_{oes}$	Output Capacitance	—	61	—		
$C_{res}$	Reverse Transfer Capacitance	—	38	—		
$L_C$	Internal Collector Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_E$	Internal Emitter Inductance	—	13	—		

④ Packaging limitation for this device is 42A.

### Notes:

- ① Half sine wave with duty cycle  $\leq 0.05$ ,  $t_{on} = 2\mu\text{sec}$ .
- ②  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

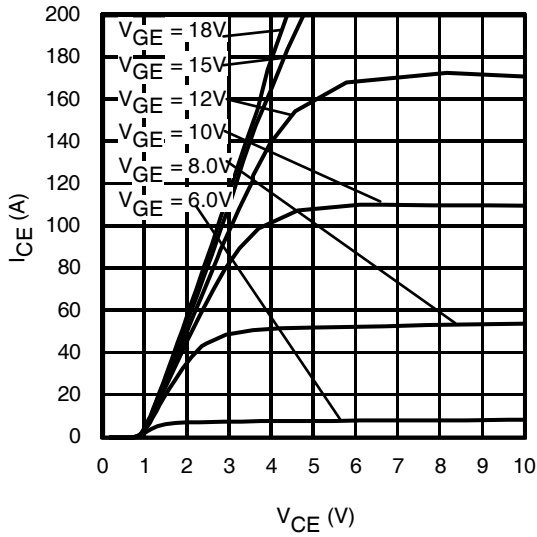


Fig 1. Typical Output Characteristics @ 25°C

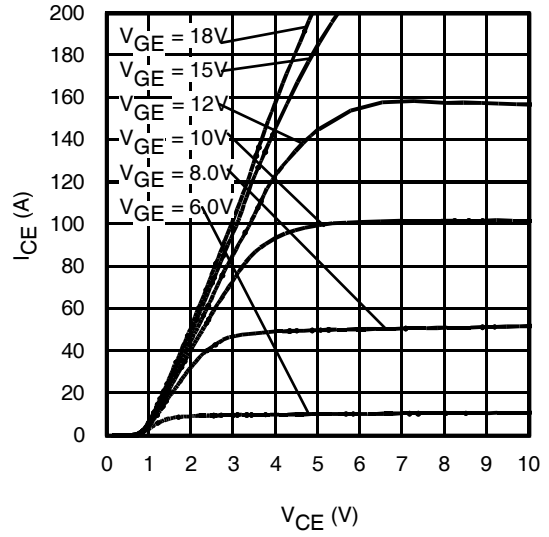


Fig 2. Typical Output Characteristics @ 75°C

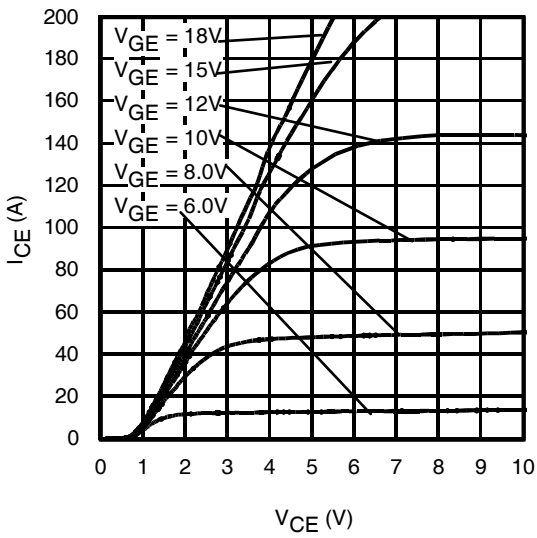


Fig 3. Typical Output Characteristics @ 125°C

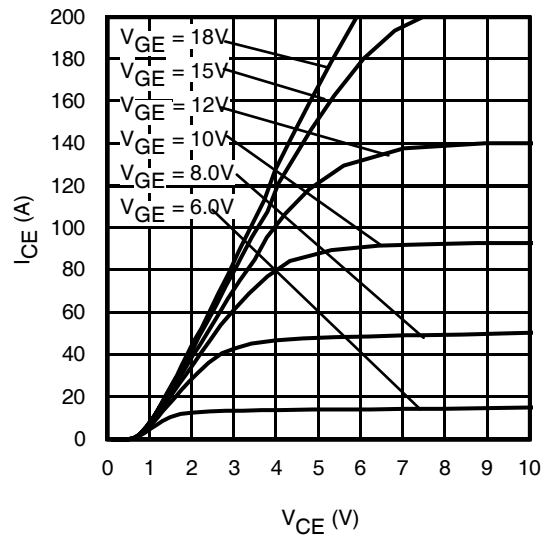


Fig 4. Typical Output Characteristics @ 150°C

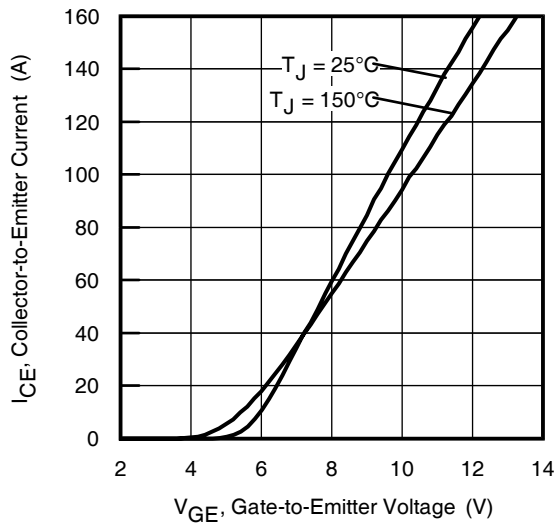


Fig 5. Typical Transfer Characteristics

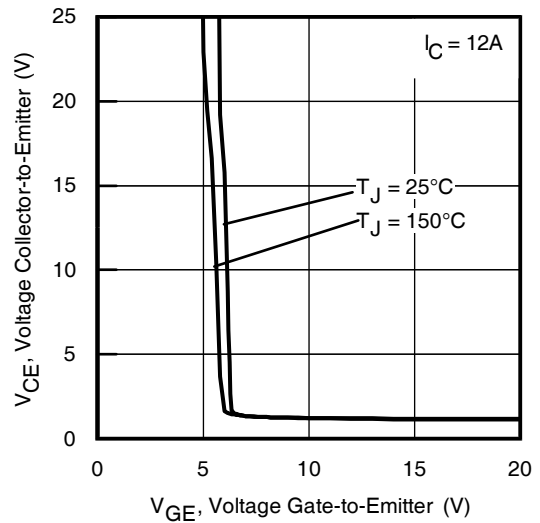


Fig 6.  $V_{CE(ON)}$  vs. Gate Voltage

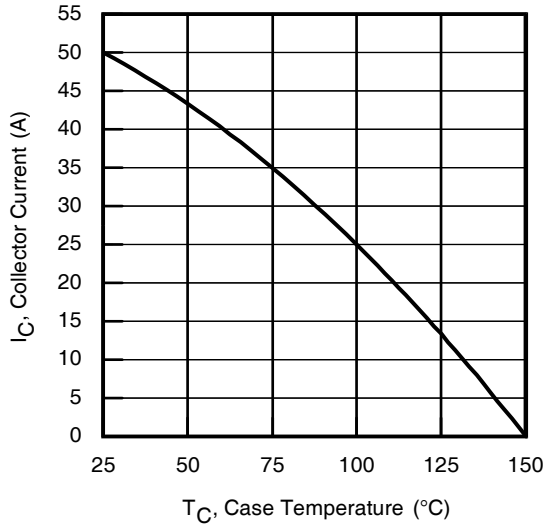


Fig 7. Maximum Collector Current vs. Case Temperature

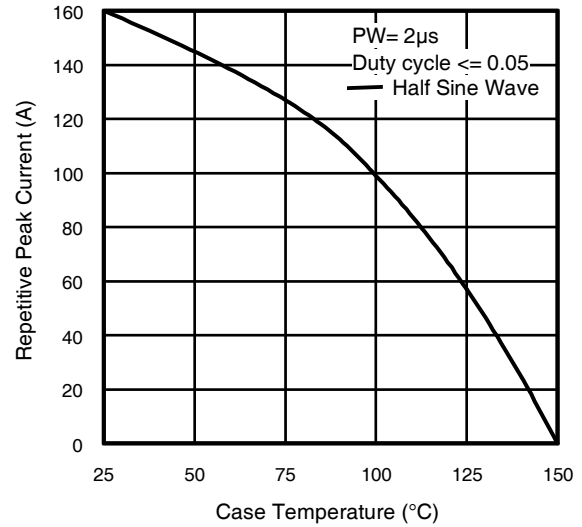


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

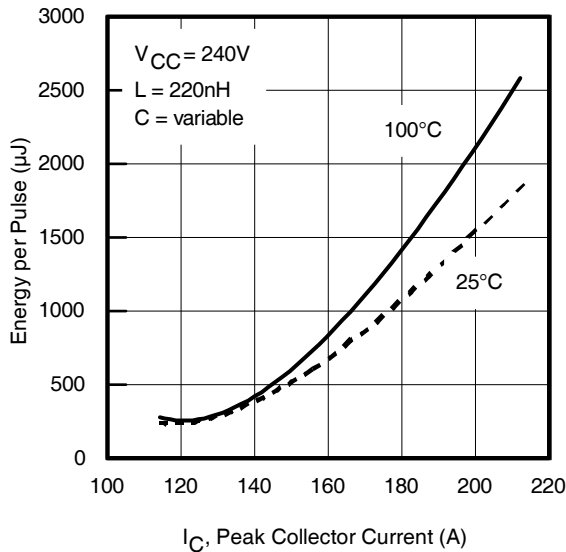


Fig 9. Typical  $E_{PULSE}$  vs. Collector Current

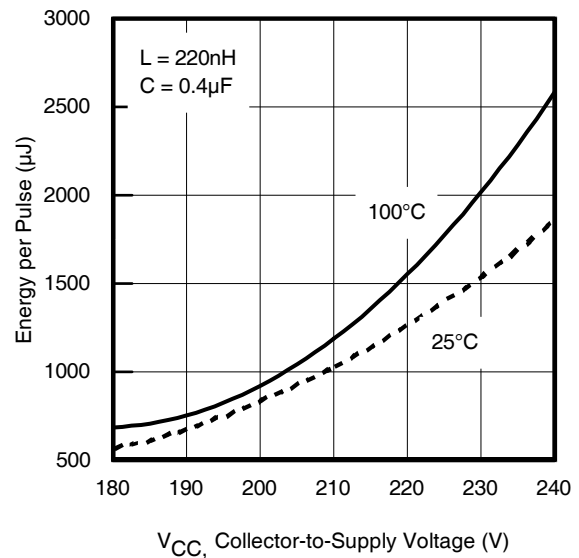


Fig 10. Typical  $E_{PULSE}$  vs. Collector-to-Supply Voltage

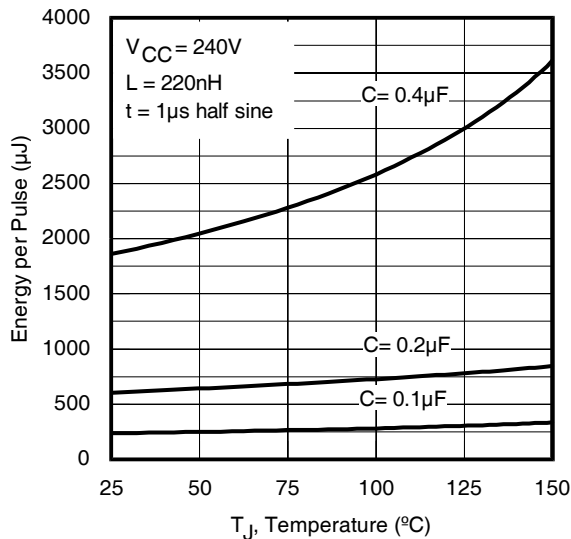


Fig 11.  $E_{PULSE}$  vs. Temperature

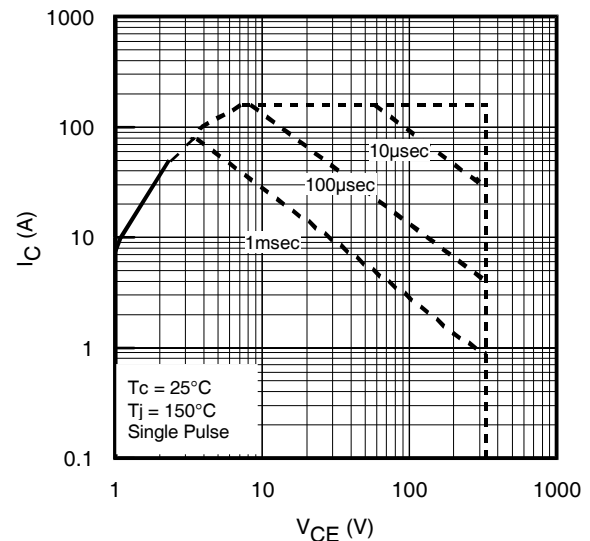


Fig 12. Forward Bias Safe Operating Area

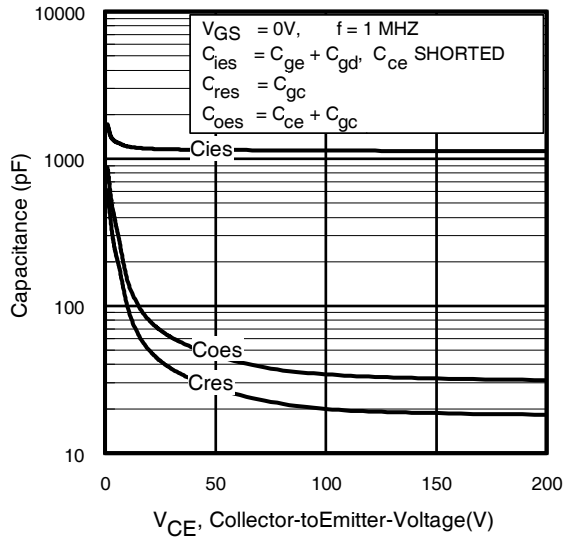


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

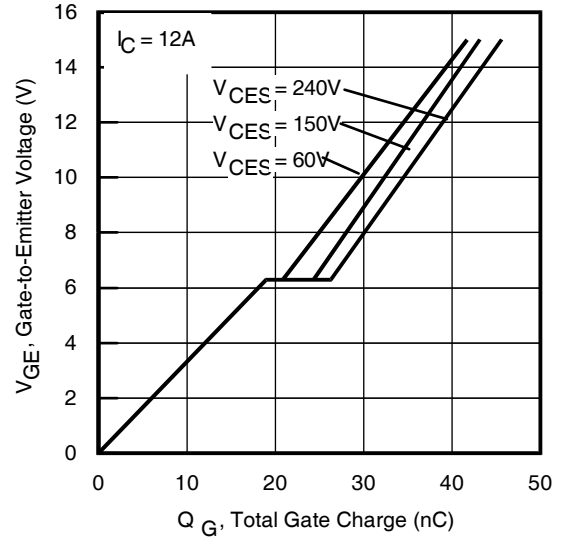


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

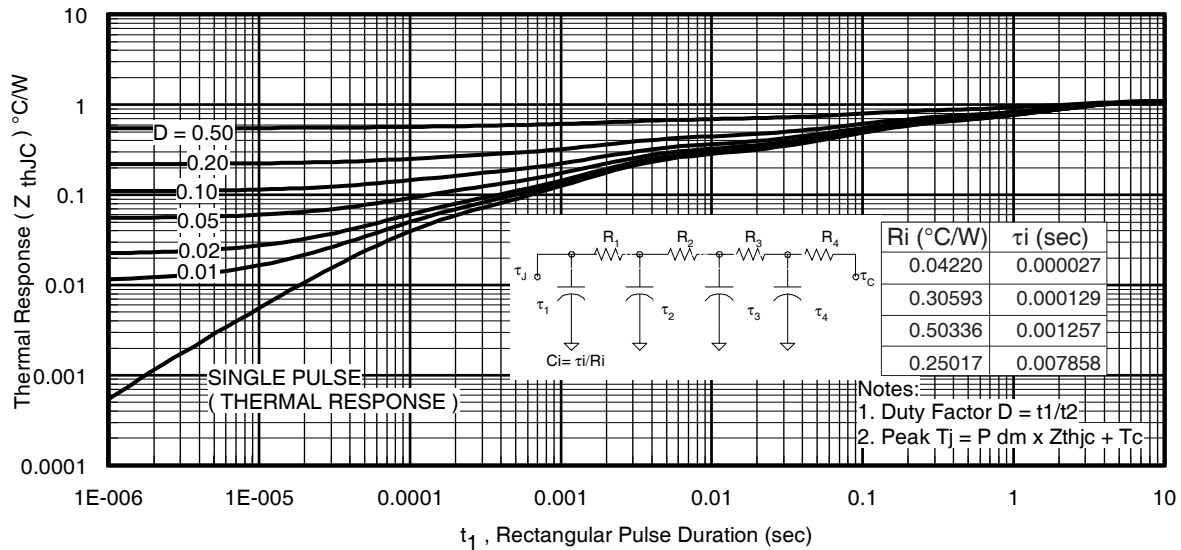
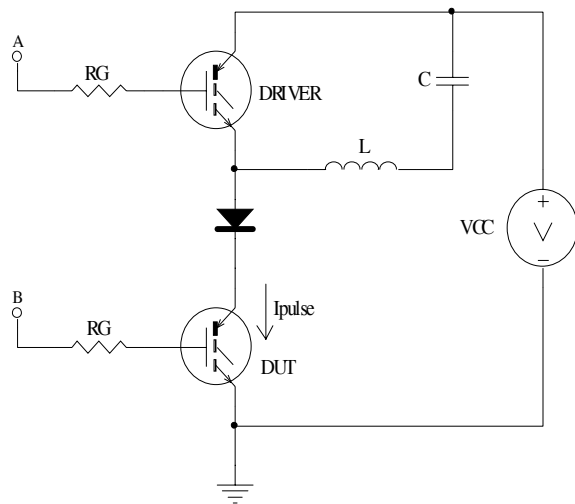
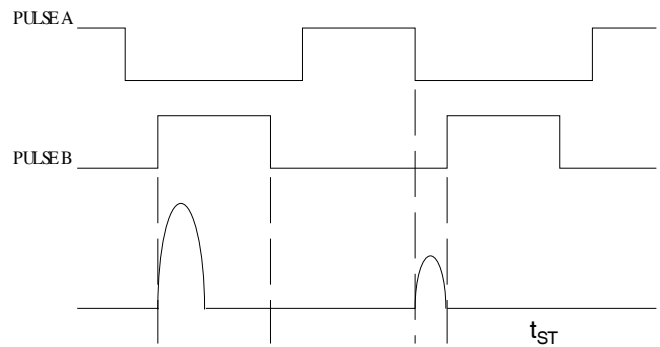


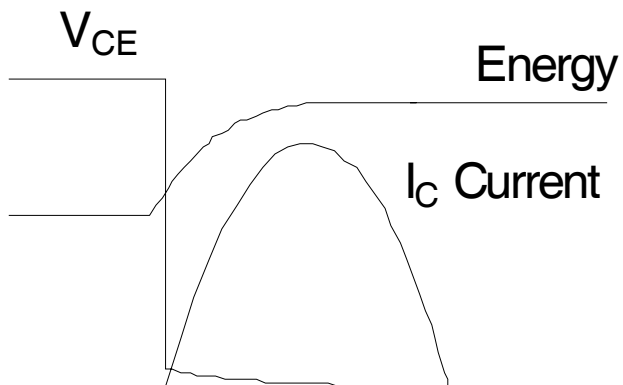
Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case



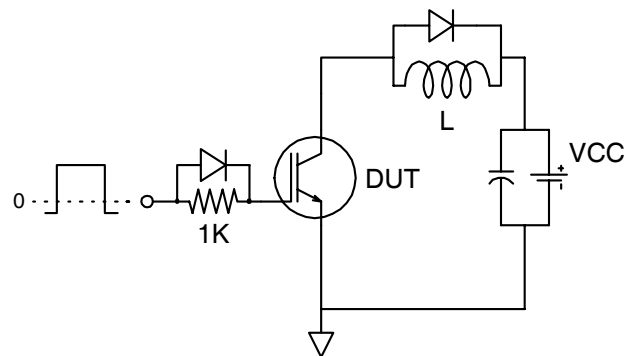
**Fig 16a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit



**Fig 16b.**  $t_{st}$  Test Waveforms



**Fig 16c.**  $E_{PULSE}$  Test Waveforms



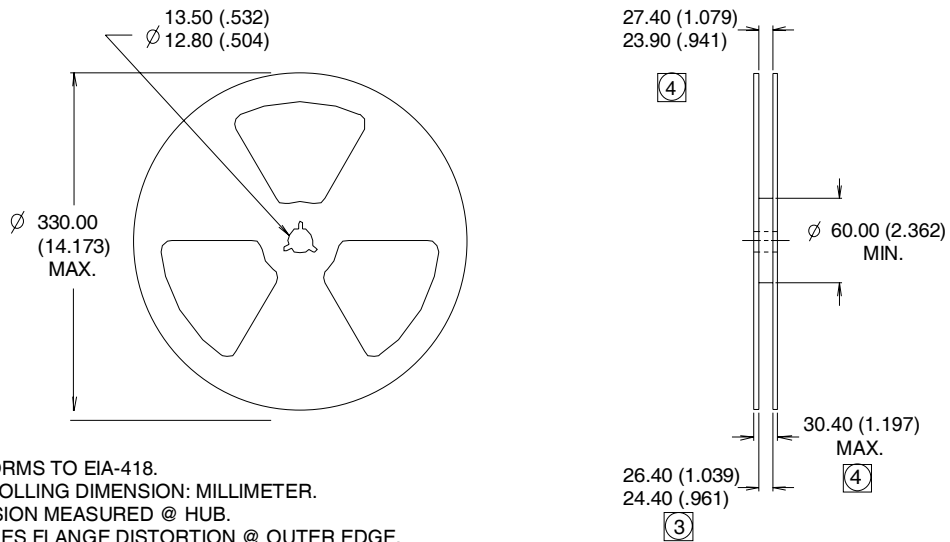
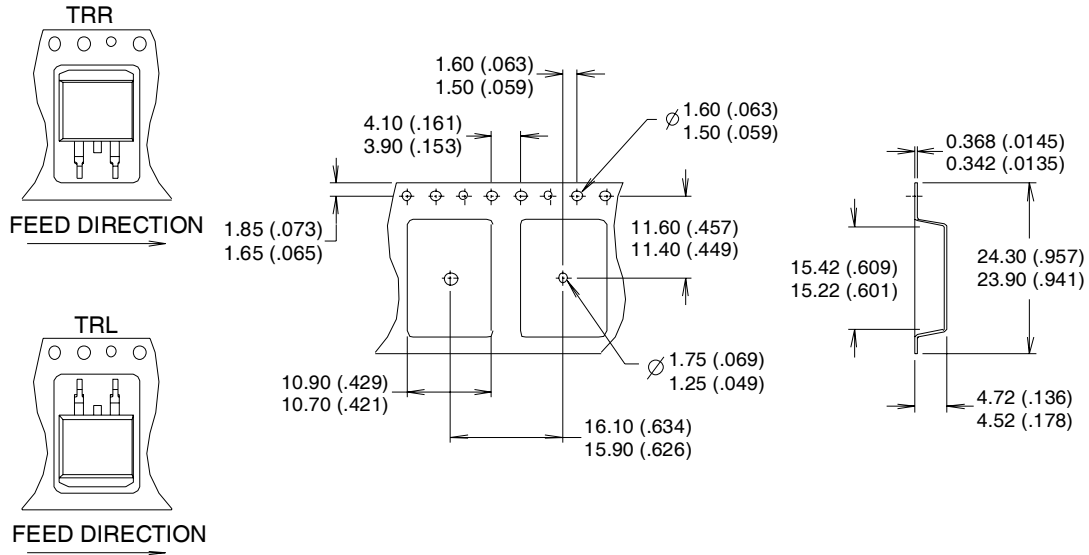
**Fig 17 -** Gate Charge Circuit (turn-off)



# IRG6S320UPbF

## D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed for the Industrial market.  
Qualification Standards can be found on IR's Web site.