ESS Technology, Inc.

ES3204 MPEG Playback Processor and System Controller Product Brief

OVERVIEW

The ES3204 is a single-chip MPEG1 audio/video/system decoder designed for a wide range of digital audio/video playback applications including karaoke players, Video CD players, and PC MPEG playback cards. When combined with memory and audio/video DACs, the ES3204 completes a highly integrated MPEG1 decoder system. The results are an overall system cost that is significantly lower than previously achievable.

The ES3204 is capable of decoding MPEG1 system layer bitstreams at up to 9 Mbits/sec at SIF® resolution with a picture rate of 30 frames/sec. Two channels of MPEG layer 1 or layer 2 audio are simultaneously decoded. For embedded applications, the ES3204's internal RISC processor can be used in place of a microcontroller to provide all system control and user features. On-chip, multi-tap filters provide arbitrary scaling, video standards conversion, and video post-processing.

The ES3204 has additional features for automatic external boot ROM width detection, additional auxiliary control pins, a glueless 24-bit RGB video interface, on-screen display (OSD), and an integrated audio DAC interface to reduce audio glue logic.

Figure 1 shows a block diagram of a typical standalone system with an embedded decoder. The MPEG system bitstream from a Video CD disk is passed to the ES3204 through the TDM (Time Division Multiplexed) serial bus or 16-bit parallel host interface. The ES3204 parses the system layer and demultiplexes the audio and video channels. Audio is decoded and passed through the audio serial bus to an audio DAC and then to the speakers. Video is decoded and output as YUV or RGB digital pixels to an NTSC or PAL video DAC/encoder, then to the screen. System control and housekeeping functions (keypad and remote control) are also provided by the chip.

FEATURES

- Single-chip MPEG1 audio/video/system decoder
- No external microcontroller required
- On-chip arbitrary video scaling
- Video CD, CDi, karaoke, and CD-XA compatible
- STC interpretation and A/V clock PLL control
- Includes CD block decoder functions
- Connects directly to CD-ROM and audio/video DACs
- Drivers for OM1, MCI, video CD, and CDi
- Video Interlacing hardware
- Bitstream error suppression/recovery
- Low power consumption
- Pin compatible with the IIT® MPPex®
- On-screen display (OSD)

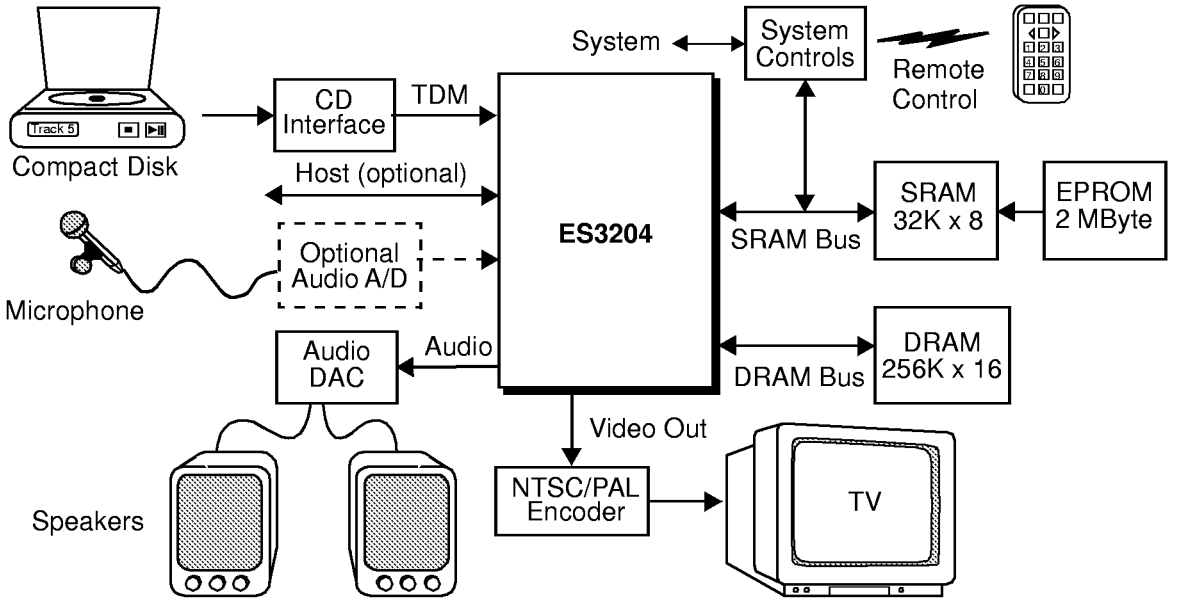

Figure 1 ES3204 Standalone System

PINOUT

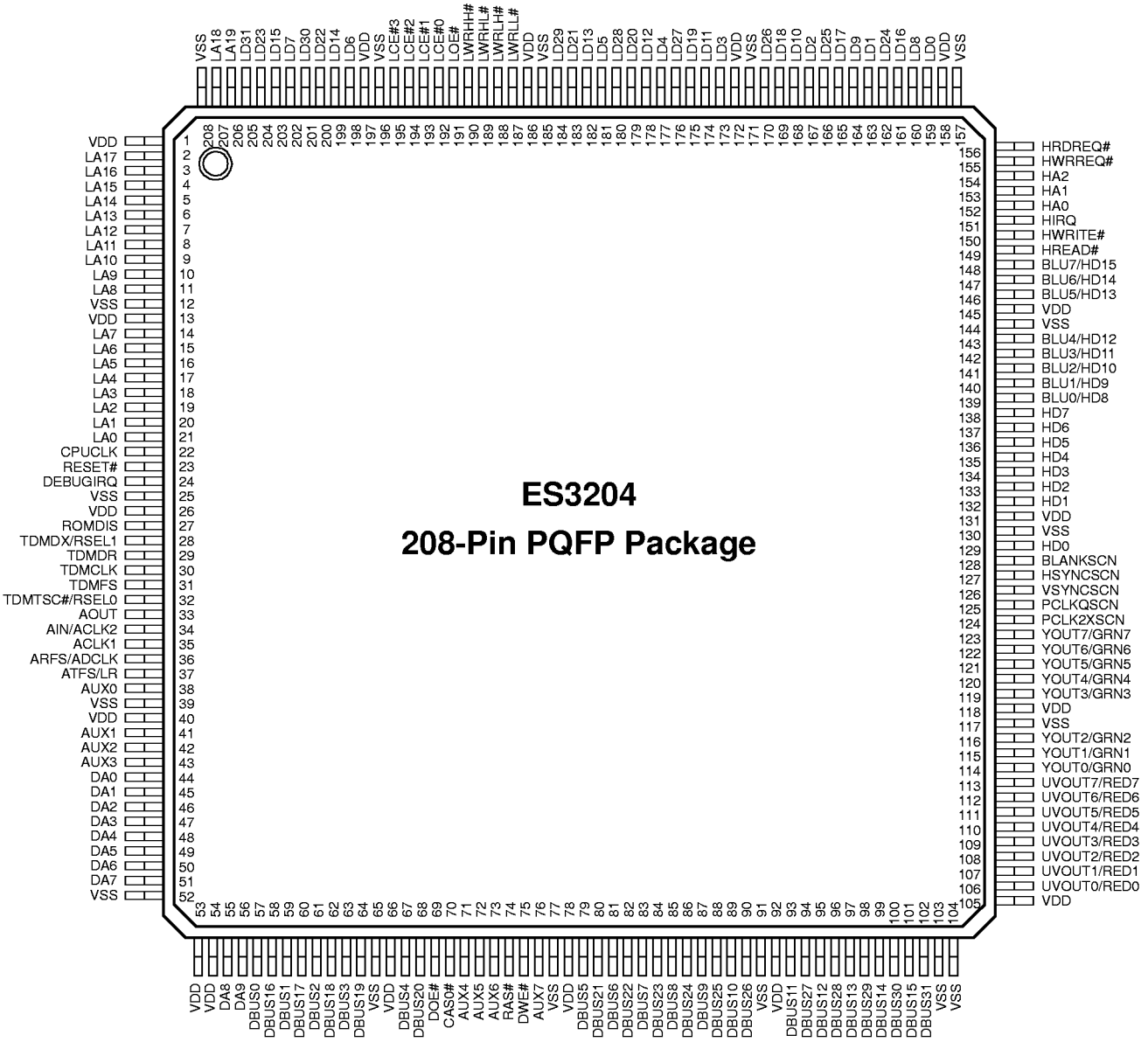

Figure 2 The ES3204 Pinout

PIN DESCRIPTIONS

Name	I/O	Definition
LOE#	O	RISC port output enable
LCE#[3:0]	O	RISC port chip enable. RISC boots from internal ROM or LCE# = 0x03, depending on the value of ROMDIS
LWRLL#	O	RISC port write enable byte 0
LWRLH#	O	RISC port write enable byte 1
LWRHL#	O	RISC port write enable byte 2
LWRHH#	O	RISC port write enable byte 3
LD[31:0]	I/O	RISC port data bus
LA[19:0]	O	RISC port address bus

Name	I/O	Definition
RESET#	I	System reset (active low)
CPUCLK	I	RISC and system clock input
DEBUGIRQ	I	System debug interrupt
ROMDIS	I	Disable the internal boot ROM and boot from external ROM located at LCE# = 0x03
AUX[1:0]	I/O	Auxiliary control lines
AUX[7:2]	I/O	These are open collectors output signals
HIRQ	O	Host interrupt request; indicates an interrupt from the VC to the host
HWRREQ#	O	Host DMA channel write request
HRDREQ#	O	Host DMA channel read request
HD[15:0]	I/O	Host data bus; compressed data is passed to and from the VC across this bus. It is also used to pass commands and parameters from the host to the VC
HA[2:0]	I	Host address bus. This bus is used by the host to address one of eight registers in the host interface
HREAD#	I	Host read; enables data from the host interface onto the HDATA[15:0] bus
HWRITE#	I	Host write; latches data from the HDATA[15:0] bus into the host interface registers
VSYNCSCN	I/O	Vertical sync for screen video port, programmable for rising or falling edge
HSYNCSCN	I/O	Horizontal sync for screen video port, programmable for rising or falling edge
BLANKSCN	O	Blanking for screen video port
PCLK2XSCN	I	Pixel clock; two times the actual pixel clock for Screen Video port
PCLKQSCN	I	Pixel Clock qualifier in for screen video port
YOUT[7:0]/ GRN[7:0]	O	Y luminance data bus for screen video port Green image data when 24-bit RGB mode selected
UVOUT[7:0]/ RED[7:0]	O	UY chrominance data bus for screen video port Red image data when 24-bit RGB mode selected
BLU[7:0]	O	Blue image data when 24-bit RGB mode selected
RAS#	O	Reference DRAM row address strobe
CAS0#	O	Reference DRAM column address strobe bank 0
DA[9:0]	O	Reference DRAM multiplexed address
DWE#	O	Reference DRAM write enable
DOE#	O	Reference DRAM output enable
DBUS[31:0]	I/O	Reference DRAM data bus
ACLK1	I	Audio port serial clock
AIN/ ACLK2	I	Audio port serial data in (AIN) Alternative, internally selectable audio input clock (ACLK2)
AOUT	O	Audio Port Serial Data Out
ARFS/ ADCLK	I/O	Audio port receive frame sync (input) Audio DAC output clock; can be either 1x or 8x data rate (output)
ATFS/ LR	I/O	Audio port transmit frame sync (input) Audio left-right output signal; high for left, low for right (output)
TDMCLK	I	TDM bus serial clock
TDMDR	I	TDM bus serial data receive
TDMDX RSEL1	I/O	TDM bus serial data transmit (output) RSEL1[1:0] RAM bank 3 boot width select. 3 = 8 bits, 2 = 16 bits, 0 = 32 bits wide (input)
TDMFS	I	TDM bus frame sync
TDMTSC#/ RSEL0	I/O	TDM bus tristate control; enables external driver for TDMDX (output) RSEL1[1:0] RAM bank 3 boot width select. 3 = 8 bits, 2 = 16 bits, 0 = 32 bits wide (input)

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Storage temperature range	-65½C to 150½C
Operating temperature range	-65½C to 110½C
Voltage range on any pin	-0.5V to (Vcc + 0.5V)
Power dissipation	2.1 W @ 33MHz

Recommended Operating Conditions

Operating temperature range	0½C to 70½C
Supply voltage Vcc	4.75V to 5.25V

DC Electrical Characteristics

(over recommended operating conditions)

Table 1 DC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit	Comments
Vih	High-level input voltage	2.0	Vcc+0.25	V	All inputs TTL levels except CLK
Vil	Low-level input voltage	-0.3	0.8	V	All inputs TTL levels except CLK
Vch	CLK high-level input	2.0	Vcc+0.25	V	TTL level input
Vcl	CLK low-level input	-0.3	0.8	V	TTL level input
Voh	High-level output voltage	3.0	–	V	IOH = 1mA
Vol	Low-level output voltage	–	0.45	V	IOL = 4mA
Ili	Input leakage current	–	±15	µA	
Ilo	Output leakage current	–	±15	µA	
Cin	Input capacitance	–	10	pF	fc = 1 MHz
Co	Input/output capacitance	–	12	pF	fc = 1 MHz
Cclk	CLK capacitance	–	20	pF	fc = 1 MHz

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Document Number: SAM0033