Am27S55

32,768-Bit (4096 x 8) Bipolar Registered PROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- "A" version offers superior performance with 20 ns set-up time and 10 ns clock-to-output delay
- Slim, 24-pin, 300-mil lateral center package occupies approximately $\frac{1}{3}$ the board space required by standard discrete PROM and register
- Consumes approximately $\frac{1}{2}$ the power of separate PROM/register combination for improved system reliability

- User-programmable for Asynchronous Enable, Synchronous Enable, Asynchronous Initialize, or Synchronous Initialize
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (Typ. > 98%)

GENERAL DESCRIPTION

The Am27S55 (4096 words by 8 bits) is a fully decoded Schottky Array TTL Programmable Read-Only Memory (PROM) incorporating D-type master-slave data registers on-chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.
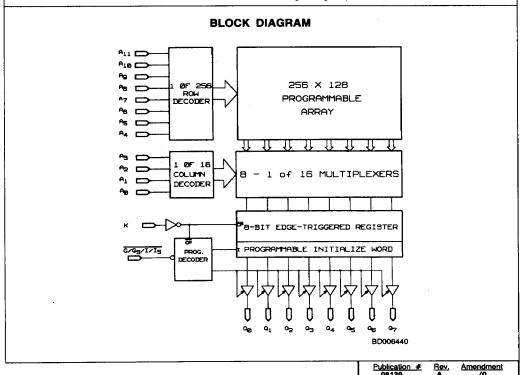
This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control

stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains a single programmable multi-functional input ($\overline{G}/\overline{G_S}/\overline{I}/\overline{I_S}$). The unprogrammed state of this pin operates as an Asynchronous Enable ($\overline{G}$) input. An architecture word permits the programming of the functionality of this pin to Synchronous Enable ($\overline{G_S}$), Asynchronous Initialize ($\overline{I}$), or Synchronous Initialize ($\overline{I_S}$).

If the architecture has been programmed to synchronous enable, upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.
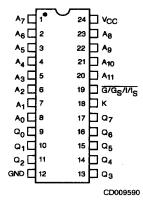
BLOCK DIAGRAM

BD006440

4-248

PRODUCT SELECTOR GUIDE

Part Number	Am27S55A		Am27S55	
Address Setup Time (ns)	20	25	25	30
Clock-to-Output Delay (ns)	10	13	13	16
Operating Range	C	M	C	M

CONNECTION DIAGRAM
Top View

```
        ┌───┬─┐
A₇  □ 1 │•  │ 24 □ V_CC
A₆  □ 2 │   │ 23 □ A₈
A₅  □ 3 │   │ 22 □ A₉
A₄  □ 4 │   │ 21 □ A₁₀
A₃  □ 5 │   │ 20 □ A₁₁
A₂  □ 6 │   │ 19 □ G̅/G̅_S/I̅/I̅_S
A₁  □ 7 │   │ 18 □ K
A₀  □ 8 │   │ 17 □ Q₇
Q₀  □ 9 │   │ 16 □ Q₆
Q₁  □ 10│   │ 15 □ Q₅
Q₂  □ 11│   │ 14 □ Q₄
GND □ 12│   │ 13 □ Q₃
        └───┴─┘
```

CD009590

LOGIC SYMBOL

12
A_0-A_{11}

$\overline{G}/\overline{G}_S/\overline{I}/\overline{I}_S$

K

Q_0-Q_7 8

LS002450

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