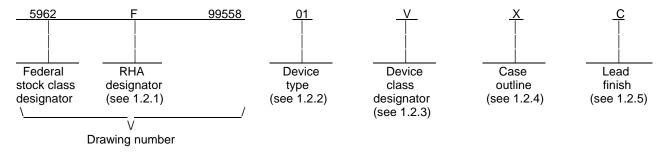
								۱	REVISION	ONS										
LTR						DESCF	RIPTIO	٧					DA	ATE (YF	R-MO-E	DA)	APPROVED			
А	Make	e chang	je to tal	ble IIB.	- ro								00-02-15				R. MONNIN			
В		case ou									CLKH,			01-0	)2-15		R. MONNIN			
С	Make	e chang	ge to the	e ambi	ent ope	erating	temper	ature ra	ange	ro				01-0	3-12		R. MONNIN			
D		new foo e 1 r		to the s	oft star	t sectio	n as sp	ecified	in table	e I and				01-0	)4-25		R. MONNIN			
DEV				ı	T	T										ı				
REV																				
REV SHEET REV	D	D	D	D	D	D														
SHEET	D 15	D 16	D 17	D 18	D 19	D 20														
SHEET REV	15				19	<u> </u>	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET REV SHEET	15			18	19	<u> </u>	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14
SHEET REV SHEET REV STATUS	15			18 REV SHE	19	20 D BY			_		5		7	8	9	10	11	12	13	
SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A	15	16		18 REV SHE PRE RIC	19 / EET PAREC	20 D BY FICER	1		_		5	6 FEN:	7 SE SI	8 UPPL UMBI	9 Y CE JS, O	10	11 COL 43216	12 .UMB	13	
SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A  STA MICRO DR THIS DRAWN FOR U DEPA	ANDAF OCIRC AWIN ING IS A USE BY A	RD CUIT G VAILAR ALL ITS	17	18 REV SHE PRE RIC	19 / EET PAREICK OFF	20 D BY FICER BY PITHAC	nia		_	MIC HA	DE CROC RDE	EFEN:	SE SI COLI http	UPPL UMBI o://ww	Y CE JS, O vw.ds	NTER HIO cc.dla	11 2 COL 43216 a.mil	UMB	13 <b>US</b>	14
SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A  STA MICRO DR THIS DRAWN FOR U DEPA AND AGE DEPARTME	ANDAF OCIRO AWIN ING IS A USE BY ARTMEN ENCIES OF I	RD CUIT G VAILANALL ITS OF THE	17	18 REV SHE PRE RIC	19 / EET PAREICK OFF CKED JESH F	D BY D BY D MON	nia	2	_	MIC HA	DE CROC RDE	CIRC NED WID	SE SI COLI http	UPPL UMBI o://ww	Y CE JS, O vw.ds	NTER HIO cc.dla	11 2 COL 43216 a.mil	UMB	13 <b>US</b>	14
SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A  STA MICRO DR THIS DRAWN FOR U DEPA AND AGE DEPARTME	ANDAF OCIRO AWIN ING IS A USE BY ARTMEN ENCIES O	RD CUIT G VAILANALL ITS OF THE	17	18 REV SHE PRE RIC CHE RA. APF RA	19 / EET PAREICK OFF CKED JESH F	D BY D MON APPRO O0-0	DIA  NIN  DVAL D  01-24	2	_	MIC HA PU SIL	DE CROC RDE LSE	CIRC NED WID N	SE SI COLI http	BUPPLUMBUS://www.	Y CE JS, O vw.ds	NTER HIO cc.dla , RA D, D	11 2 COL 43216 a.mil	ION OUT	US  FPU7	14

#### 1. SCOPE

- 1.1 <u>Scope</u>. This drawing documents three product assurance class levels consisting of high reliability (device classe Q and M), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.
  - 1.2 PIN. The PIN is as shown in the following example:



- 1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
  - 1.2.2 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number	<u>Circuit function</u>
01	HS-1825ARH	Radiation hardened DI dual output pulse width modulator

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

Device class	<u>Device requirements documentation</u>
М	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535
Т	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
Е	CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

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# 1.3 Absolute maximum ratings. 1/2/3/

Supply voltage (V <sub>S</sub> )	36 V dc
Power dissipation (P <sub>D</sub> )	1.6 W
Junction temperature (T <sub>J</sub> )	
Lead temperature (soldering, 10 seconds)	
Thermal resistance, junction-to-case (θ <sub>JC</sub> ):	
Cases E and 2	18°C/W
Case X	8°C/W
Thermal resistance, junction-to-ambient ( $\theta_{JA}$ ):	
Cases E and 2	70°C/W
Case X	90°C/W
4. Percommended operating conditions 2/3/	

### 1.4 Recommended operating conditions. 2/3/

Supply voltage (V <sub>S</sub> )	12 V to 30 V
Ambient operating temperature range (T <sub>A</sub> )	-50°C to +125°C

# 1.5 Radiation features:

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s):

Device classes M, Q, or V	3 x 10 <sup>5</sup> Rads (Si)
Device class T	1 x 10 <sup>5</sup> Rads (Si)
Latch-up	None <u>4</u> /

# 2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

# **SPECIFICATION**

# DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

<sup>4/</sup> Guaranteed by process or design.

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<sup>1/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

<sup>2/</sup> Unless otherwise noted, all voltages are referenced to GND.

<sup>3/</sup> The limits for the parameters specified herein shall apply over the full specified V<sub>CC</sub> range and ambient temperature range of -50°C to +125°C unless otherwise noted.

#### **STANDARDS**

#### DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

#### **HANDBOOKS**

# DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

#### 3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.
  - 3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V or MIL-PRF-38535, appendix A and herein for device class M.
  - 3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.
  - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.
  - 3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.
  - 3.2.4 Irradiation test connections. The irradiation test connections shall be as specified in figure 3.
- 3.3 <u>Electrical performance characteristics and post irradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.
- 3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.
- 3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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Test	Symbol	Test conditions $\underline{1}/$ $-50^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Reference section					l			
Output voltage	V <sub>REF</sub>			01	1	5.05	5.15	V
, ,	VKEF				2,3	5.025	5.25	
		M,D,P,L,F	R.F		1	5.025	5.25	_
Line regulation	VLINE	12 < V <sub>C</sub> < 20 V	,	01	1	-15	15	mV
	* LINE	12 (10 (20 )			2,3	-20	20	
		M,D,P,L,F	R,F		1	-20	20	
Load regulation	V <sub>LOAD</sub>	1 mA < I <sub>OUT</sub> < 10 mA		01	1	-25	25	mV
	20/12				2,3	-50	50	
		M,D,P,L,I	R,F		1	-50	50	
Total output	V <sub>OM</sub>	V <sub>C</sub> = 12 V, 20 V,		01	1	5.00	5.20	V
variation		I <sub>L</sub> = 1 mA, 10 mA			2,3	5.00	5.30	
		M,D,P,L,F	R,F		1	5.00	5.30	
Short circuit current	I <sub>SC</sub>	V <sub>REF</sub> = 0 V	,	01	1	30		mA
	100	TKEI			2,3	20		1
		M,D,P,L,I	R,F		1	20		
Oscillator section  Initial accuracy	Te.	1		01	4	350	425	kHz
miliar accuracy	FO				5,6	300	425	- "
		M,D,P,L,I	R F		4	300	425	1
Voltage stability	dF <sub>O</sub> /D <sub>V</sub>	12 V < V <sub>C</sub> < 20 V	1,1	01	4	-2	2	%
, <b>g</b>	ur θ/bγ	12 V < VC < 20 V			5,6	-7	7	
		M,D,P,L,I	R.F		4	-3	3	
Total variation	F <sub>OM</sub>	V <sub>C</sub> = 12 V, 20 V		01	4	350	425	kHz
	· OIVI	V = 12 v, 20 v			5,6	300	425	-
		M,D,P,L,I	R F		4	300	425	
Clock out high	Volum	101,0,1 ,0,1	1,1	01	1	4.0	720	V
voltage	VCLKH				2,3	3.75		1
voltage		M,D,P,L,I	? F		1	3.75		1
Clock out low	VCLKL	w,z,r,z,r	·,·	01	1,2,3	0.70	0.2	V
voltage	VCLKL	M,D,P,L,I	R.F		1		0.2	
See footnotes at end of	table.	,- ,. , <del>-</del> ,.	·	1	<u> </u>			<u> </u>
	STANDARI		SIZE <b>A</b>			5	5962-9	9558
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Test	Symbol	$\begin{tabular}{lll} Symbol & Test conditions $\underline{1}/$ \\ & -50^{\circ}C \leq T_{A} \leq +125^{\circ}C \\ & unless otherwise specified \\ \end{tabular}$		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Error amplification sec	tion						L	
nput offset voltage	1/	T., 20V	2.7. 2.2.7	01	1,2,3	-10	10	m۷
ilput onoot roilage	Vos	$V_{CM} = 3.0 V,$	, $V_O = 3.0 \text{ V}$ M,D,P,L,R,F		1,2,3	-10	10	4
nput bias current	1	V <sub>CM</sub> = 3.0 V,		01	1,2,3	-10	10	μА
ilput blue carry	I <sub>IB</sub>	VCM = 3.0 v,	, V <sub>O</sub> = 3.0 V M,D,P,L,R,F	_	1,2,0	-1	1	
nput offset current	1	301/		01	1,2,3	-1	2	μΑ
ilput olioot oui	los	$V_{CM} = 3.0 V,$						_ µ.
Open loop gain	<del></del>	ļ	M,D,P,L,R,F	01	1 4,5,6	-2 60	2	dB
уреп юор уаш	Avol	1 V < V <sub>O</sub> < 4		U			<u> </u>	_ u_
Common mode	CMRR		M,D,P,L,R,F	01	4	60 65	<del> </del>	dB
	CIVIKN	1.5 V < V <sub>CM</sub>	< 4.0 V	U I	-		<u> </u>	_ uL
rejection ratio			M,D,P,L,R,F	_	5,6 4	45 65	<del> </del>	4
Power supply	PSRR	101/11/01		01	4,5,6	80	-	dE
	FOR	12 V < V <sub>C</sub> < 2			4,5,6	80	<u> </u>	_
rejection ratio  Output sink	1.		M,D,P,L,R,F	01	1,2,3	80		m/
•	losk	VE/A OUT = 1					<u> </u>	_ '''
current  Output source	<u> </u>	1.,	M,D,P,L,R,F	01	1,2,3	-0.5	-	m/
•	losc	VE/A OUT = 4					<u> </u>	_ '''
current  Output high voltage	<u> </u>	1	M,D,P,L,R,F	01	1,2,3	-0.5 4.0		V
Julput mgn voltage	V <sub>OH1</sub>	I <sub>E/A</sub> OUT = -0					<u> </u>	
Output low voltage	<u> </u>	1	M,D,P,L,R,F	01	1,2,3	4.0	1.0	V
Jutput IOW Voltage	V <sub>OL1</sub>	I <sub>E/A</sub> OUT = 1		U		<u> </u>		_
Pulse width modulator	(PWM) comr		M,D,P,L,R,F		1		1.0	
Ramp bias current	I <sub>RAMP</sub>	V <sub>RAMP</sub> = 0 V	/	01	1,2,3		-8	μΑ
			M,D,P,L,R,F	1	1	 I	-8	1
Duty cycle range	DC <sub>RNG</sub>			01	4,5,6	40		%
	<u> </u>		M,D,P,L,R,F	1	4	40		1
E/A out zero DC	V <sub>TH</sub>	Ramp voltage	e = 0 V	01	1,2,3	0.89		V
threshold voltage			M,D,P,L,R,F		1	0.89		
ee footnotes at end of	table.							

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MICROCIRCUIT DRAWING
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Test	Symbol	Test conditions $-50^{\circ}C \le T_{A} \le +12$ unless otherwise sp	5°C type	Group A subgroups	Lir	nits	Unit
					Min	Max	
Soft start section 2/	1	1		l		1	<u></u>
Charge current	I <sub>CHG</sub>	Soft start voltage = 2.5 V	01	1	8	20	μА
	0110			2,3	8	25	-
		M,D,P,L,R	l,F	1	8	25	-
Discharge current	IDCHG	Soft start voltage = 2.5 V	01	1,2,3	0.1	0.350	mA
		M,D,P,L,R	R,F	1	0.1	0.350	-
Current limit / Start sequ	ience / Fault	section	,	1			<u></u>
Restart threshold	V <sub>RS</sub>		01	1,2,3		0.5	V
		M,D,P,L,R	l,F	1		0.5	†
ILIM bias current	I <sub>BLIM</sub>	0 < V <sub>ILIM</sub> < 2 V	01	1,2,3		15	μΑ
		M,D,P,L,R	2,F	1		15	†
Current limit threshold	VLIMIT		01	1	0.95	1.10	V
				2,3	0.90	1.10	
		M,D,P,L,R	,F	1	0.90	1.10	
Over current	Vover		01	1,2,3	1.14	1.26	V
threshold		M,D,P,L,R	,F	1	1.14	1.26	1
Output section			•	•			
Output low	V <sub>SATL1</sub>	I <sub>OUT</sub> = 20 mA	01	1		0.8	V
saturation 1				2,3		1.0	-
		M,D,P,L,R	,F	1		0.8	
Output low	V <sub>SATL2</sub>	I <sub>OUT</sub> = 200 mA	01	1,2,3		2.2	V
saturation 2		M,D,P,L,R	l,F	1		2.2	1
Output high	V <sub>SATH1</sub>	I <sub>OUT</sub> = 20 mA	01	1,2,3	10		V
saturation 1		M,D,P,L,R	l,F	1	10		1
Output high	V <sub>SATH2</sub>	I <sub>OUT</sub> = 200 mA	01	1,2,3	9		V
saturation 2		M,D,P,L,R	l,F	1	9		1
Under voltage lockout (UVLO) output low	Vols	I <sub>O</sub> = 20 mA	01	1,2,3		1.2	V
saturation voltage		M,D,P,L,R	,F	1		1.2	1
See footnotes at end of to	able.						
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Test	Symbol			Device type	Group A subgroups	Lir	nits	Unit
						Min	Max	
Under voltage section		I			<u> </u>		I	1
Start threshold	VSTART			01	1,2,3	8.4	9.6	V
voltage	0174101		M,D,P,L,R,F		1	8.4	9.6	1
Stop threshold	VSTOP			01	1,2,3		9.6	V
voltage			M,D,P,L,R,F		1		9.6	1
Under voltage lockout	VHYS			01	1,2,3	0.3	1.2	V
(UVLO) hysteresis			M,D,P,L,R,F		1	0.3	1.2	1
Supply current section	1	1					•	· •
Startup current	I <sub>SU</sub>	V <sub>CC</sub> = 8.0 V		01	1,2,3		300	μΑ
			M,D,P,L,R,F		1		300	1
Supply current	Icc	Inverting inpu LIM / SD volt	ut, RAMP, and current age = 0 V,	01	1,2,3		36	mA
			g input voltage = 1.0 V					
			M,D,P,L,R,F		1		36	1

- 1/ Devices supplied to this drawing meet all levels M, D, P, L, R, and F for device classes M, Q, and V and for device class T, will meet levels M, D, P, L, and R of irradiation. However, this device is only tested at the "F" level for device classes M, Q, and V and at the "R" level for device class T (see 1.5 herein). Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T<sub>A</sub> = +25°C.
- 2/ Grounding of the SOFT START pin does not inhibit the outputs.
- 3.6 <u>Certificate of compliance</u>. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change for device class M.</u> For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.
- 3.9 <u>Verification and review for device class M.</u> For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 3.10 <u>Microcircuit group assignment for device class M.</u> Device class M devices covered by this drawing shall be in microcircuit group number 90 (see MIL-PRF-38535, appendix A).

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Device type	01		
Case outlines	E and X 2		
Terminal number	Termina	l symbol	
1	INV	NC	
2	NON-INV	INV	
3	E/A OUT	NON-INV	
4	CLOCK	E/A OUT	
5	R <sub>T</sub>	CLOCK/LEB	
6	СТ	NC	
7	RAMP	R <sub>T</sub>	
8	SOFT START	СТ	
	(SEE NOTE 2)		
9	ILIM/SD	RAMP	
10	GND	SOFT START	
		(SEE NOTE 2)	
11	OUTPUT A	NC	
12	POWER GND	ILIM/SD	
13	Vc	GND	
14	OUTPUT B	OUTPUT A	
15	Vs	POWER GND	
16	V <sub>REF</sub> 5.1 V	NC	
17		Vc	
18		OUTPUT B	
19		VS	
20		V <sub>REF</sub> 5.1 V	

# NOTES:

- NC = No connection
   Grounding of the SOFT START pin does not inhibit the outputs.

FIGURE 1. Terminal connections.

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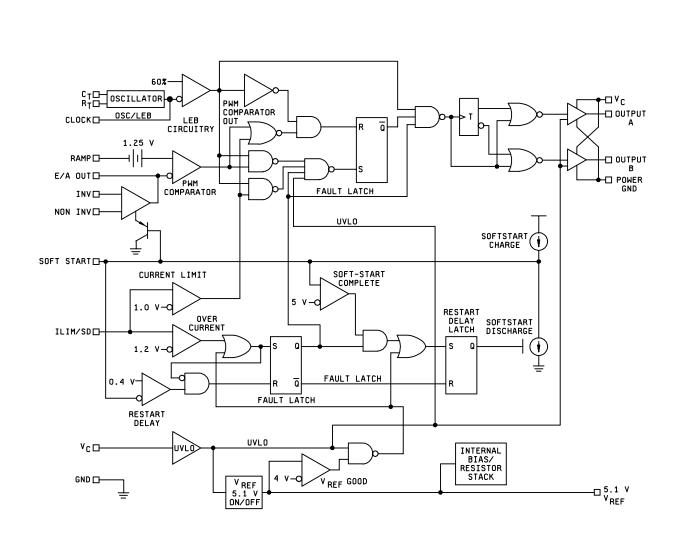


FIGURE 2. Logic diagram.

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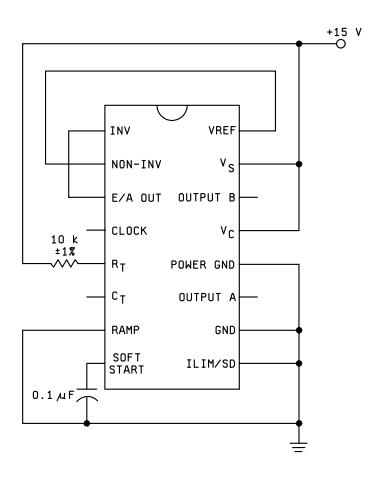


Figure 3. Irradiation connections.

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#### 4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection.</u> For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein.

For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan, including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

# 4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
  - (2)  $T_A = +125^{\circ}C$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

### 4.2.2 Additional criteria for device classes Q, T and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's Quality Management (QM) plan.

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### TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,4	1,4	1,4	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,4,5,6 <u>1</u> /	1,2,3,4,5,6 <u>1</u> /	1,2,3,4, <u>2</u> / <u>3</u> / 5,6	
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6	
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6 <u>3</u> /	
Group D end-point electrical parameters (see 4.4)	1,4	1,4	1,4	
Group E end-point electrical parameters (see 4.4)	1,4	1,4	1,4	

- 1/ PDA applies to subgroups 1 and 4.
- 2/ PDA applies to subgroups 1, 4, and  $\Delta$ 's.
- Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in delta parameters (+25°) and group C delta parameters.

Parameters 1/	Symbol	Delta limits
Supply current	Icc	±2.0 mA
Input bias current	l <sub>IB</sub>	±50 nA

- 1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.
- 4.3 <u>Qualification inspection for device classes Q, T and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).
- 4.3.1 <u>Electrostatic discharge sensitivity (ESDS) qualification inspection</u>. ESDS testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

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- 4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535, or as specified in the QM plan, including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.
  - 4.4.1 Group A inspection.
    - a. Tests shall be as specified in table IIA herein.
    - b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.
  - 4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.
  - 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:
    - a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
    - b.  $T_A = +125^{\circ}C$ , minimum.
    - c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - 4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.
- 4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in table IIA herein. For device class T, the RHA requirements shall be in accordance with the Class T Radiation Requirements of MIL-PRF-38535. The end-point electrical parameters for class T devices shall be as specified in Table I, Group A subgroups, or as modified in the QM plan.
- 4.4.4.1 <u>Total dose irradiation testing</u>. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535 (see 1.5 herein).
- 4.4.4.1.1 <u>Accelerated aging testing</u>. Accelerated aging testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.
  - 4.5 Methods of inspection. Methods of inspection shall be specified as follows:
- 4.5.1 <u>Voltage and current</u>. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

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#### 5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

#### 6. NOTES

- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.
  - 6.1.2 Substitutability. Device class Q devices will replace device class M devices.
- 6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.
- 6.3 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.
- 6.4 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.
- 6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.
  - 6.6 Sources of supply.
- 6.6.1 <u>Sources of supply for device classes Q, T and V</u>. Sources of supply for device classes Q, T and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.
- 6.6.2 <u>Approved sources of supply for device class M.</u> Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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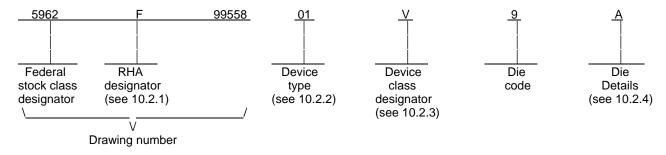
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#### 10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-1825ARH	Radiation hardened DI dual output
		pulse width modulator

10.2.3 Device class designator.

Device class Device requirements documentation Q or V Certification and qualification to the die requirements of MIL-PRF-38535

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10.2.4. <u>Die Details</u>. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die physical dimensions.

Die type Figure number

01 A-1

10.2.4.2. Die bonding pad locations and electrical functions.

Die type Figure number

01 A-1

10.2.4.3. Interface materials.

Die type Figure number

01 A-1

10.2.4.4. Assembly related information.

Die type Figure number

01 A-1

- 10.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.
- 10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.
- 20. APPLICABLE DOCUMENTS.
- 20.1 <u>Government specifications, standards, and handbooks</u>. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

# **SPECIFICATION**

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

**STANDARDS** 

**DEPARTMENT OF DEFENSE** 

MIL-STD-883 - Test Method Standard Microcircuits.

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#### **HANDBOOK**

#### **DEPARTMENT OF DEFENSE**

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of the specification, standard, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2. <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

#### 30. REQUIREMENTS

- 30.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.
- 30.2 <u>Design, construction and physical dimensions</u>. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.
  - 30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1.
- 30.2.2 <u>Die bonding pad locations and electrical functions</u>. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1.
  - 30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1.
  - 30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1.
- 30.2.5 <u>Radiation exposure circuit</u>. The radiation exposure circuit shall be as defined within paragraph 3.2.4 of the body of this document.
- 30.3 <u>Electrical performance characteristics and post-irradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.
- 30.4 <u>Electrical test requirements</u>. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.
- 30.5 <u>Marking</u>. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.
- 30.6 <u>Certification of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.
- 30.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

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#### 40. QUALITY ASSURANCE PROVISIONS

- 40.1 <u>Sampling and inspection</u>. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturers Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.
- 40.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:
  - a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.
  - b) 100% wafer probe (see paragraph 30.4).
  - c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

#### 40.3 Conformance inspection.

40.3.1 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1 and 4.4.4.1.1.

#### 50. DIE CARRIER

50.1 <u>Die carrier requirements</u>. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

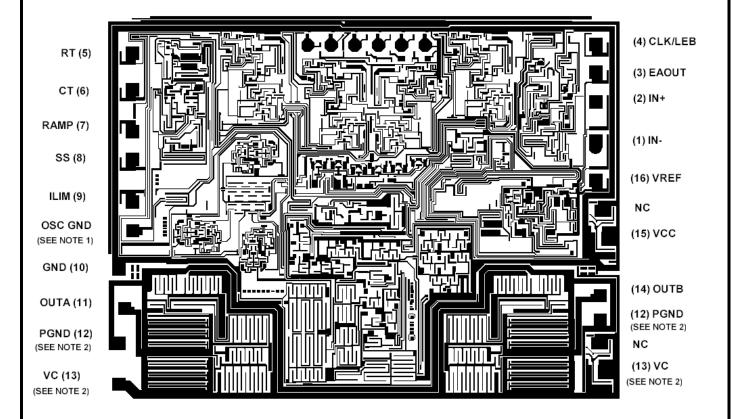
# 60 NOTES

- 60.1 <u>Intended use</u>. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.
- 60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.
- 60.3 <u>Abbreviations, symbols and definitions</u>. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.
- 60.4 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

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NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.

Die size: 4710 microns x 3570 microns. Die thickness:  $19 \text{ mils} \pm 1 \text{ mils}$ .

Interface materials.

Top metallization: Al Si Cu 16.0 kÅ ±2 kÅ

Backside metallization: None

Glassivation. Type: PSG

Thickness: 8.0 kÅ ±1.0 kÅ Type: Si3 N4

Thickness: 4.0 kÅ ±0.5 kÅ

Substrate: DI (dielectric isolation)

Assembly related information. Substrate potential: Unbiased

Special assembly instructions: Note 1. The oscillator ground (OSC GND) pad must be connected to ground.

Note 2. PGND and V<sub>C</sub> each require 2 bond pad connections.

FIGURE A-1. Die bonding pad locations and electrical functions.

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# STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-04-25

Approved sources of supply for SMD 5962-99558 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962F9955801QEC	34371	HS1-1825ARH-8
5962F9955801QXC	34371	HS9-1825ARH-8
5962F9955801Q2C	34371	HS4-1825ARH-8
5962R9955801TXC	34371	HS9-1825ARH-T
5962F9955801VEC	34371	HS1-1825ARH-Q
5962F9955801VXC	34371	HS9-1825ARH-Q
5962F9955801V2C	34371	HS4-1825ARH-Q
5962F9955801V9A	34371	HS0-1825ARH-Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- <u>2</u>/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

34371

Intersil Corporation P.O. Box 883 Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.