STV0684

Digital Camera Processor

PRODUCT PREVIEW

Features

- **Supports the VC6700 CMOS sensor (UXGA, 1600 x 1200 pixels) from STMicroelectronics**
- **High quality video processor**
  - RAM based firmware
  - Pixel defect correction
  - NORA (Noise Reduction Algorithm
  - Anti-vignetting algorithm
  - Advanced statistics processor
  - Two general purpose scalers
  - Dual video interface for concurrent viewfinder and movie capture
- **ST20 32-bit core**
  - Instruction, data cache and embedded memory for fast code execution
  - Embedded ROM bootloader for code storage in cost effective NAND flash memory
  - Code executed in SDRAM, no code-size limitation
- **AVI (Audio Video Interleave) clips directly recorded into the mass storage media**
  - Long clip length
  - Low power consumption
- **Flexible TFT, D-TFD digital interface for preview (while recording) and review**
  - Direct support for Casio, Epson and AU optronics displays
  - Flexible digital interface designed to support future digital panels
- **PAL and NTSC encoder with on-chip digital to analog converter**
  - TV display of pictures and movie clips
- **On-chip 16-bit Sigma-Delta analog to digital converter for audio record**
- **Audio digital to analog converter for audio playback**
- **Versatile mass storage interface**
  - Support Compact-flash, Nand-on-board, Smartmedia, Secure Digital and Multi-Media
- **USB 2.0 full speed device**
  - USB audio and video class compliant
  - USB mass storage class compliant, Bulk only transfer protocol
- **JPEG and MJPEG CODEC**

Description

The STV0684 processor is targeted for use in CMOS digital still cameras. ST supplies complete camera reference designs which include sensor, co-processor, firmware and software drivers. The STV0684 uses a small BGA package (12 mm x 12 mm) ideal for the design of very small digital cameras. The STV0684 incorporates ST's unique and highly performing video processor algorithms including newly improved and patented algorithms (e.g. NORA and Anti-vignetting).

The CMOS sensors from STMicroelectronics use pinned photodiodes manufactured in a high performance process resulting in improved low light performance, reducing the gap with CCD sensors.

Applications

- Digital still cameras
- Solid state video camera recorders
- Embedded cameras

Ordering Information

Part Number	Temperature	Package
STV0684	[0; +70] °C	BGA196

Technical Specifications

Resolution	UXGA - VC6700V048
Sample rate	up to 48 M sample/s (MSPS)
Power supply	3.3V and 1.8V
Power requirements	mA typical
Package	BGA196, 12x12 mm

System Overview

Figure 1: STV0684 system overview

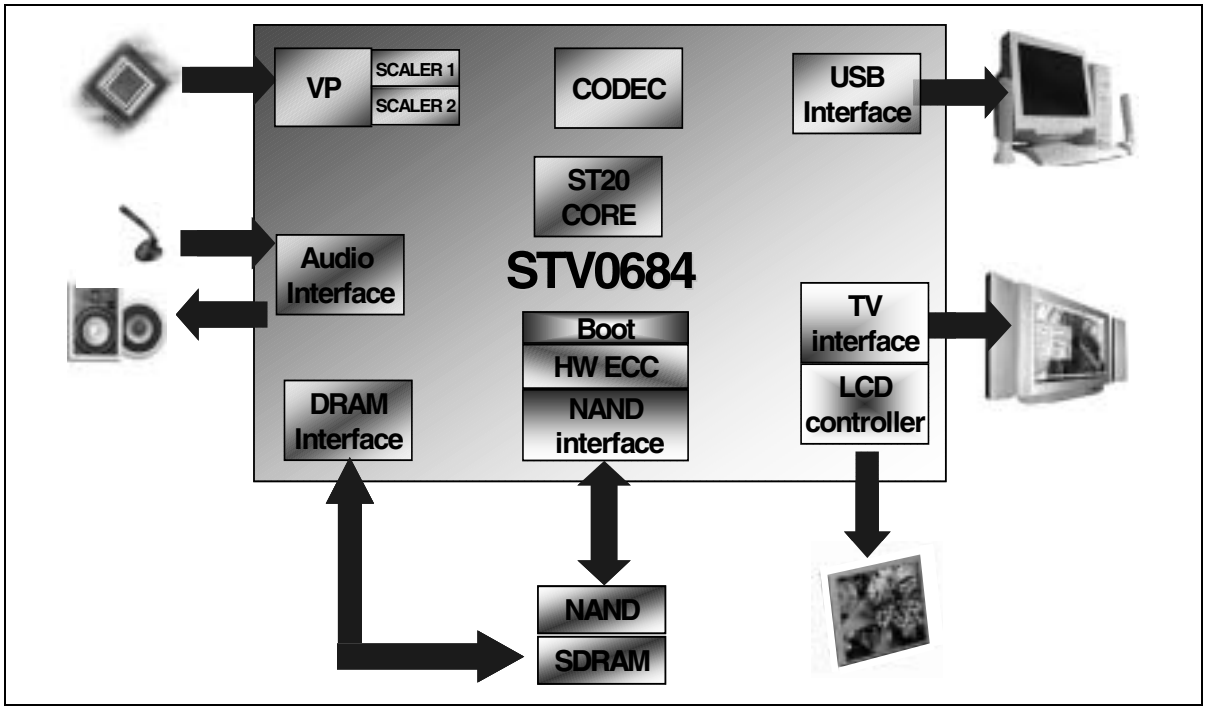

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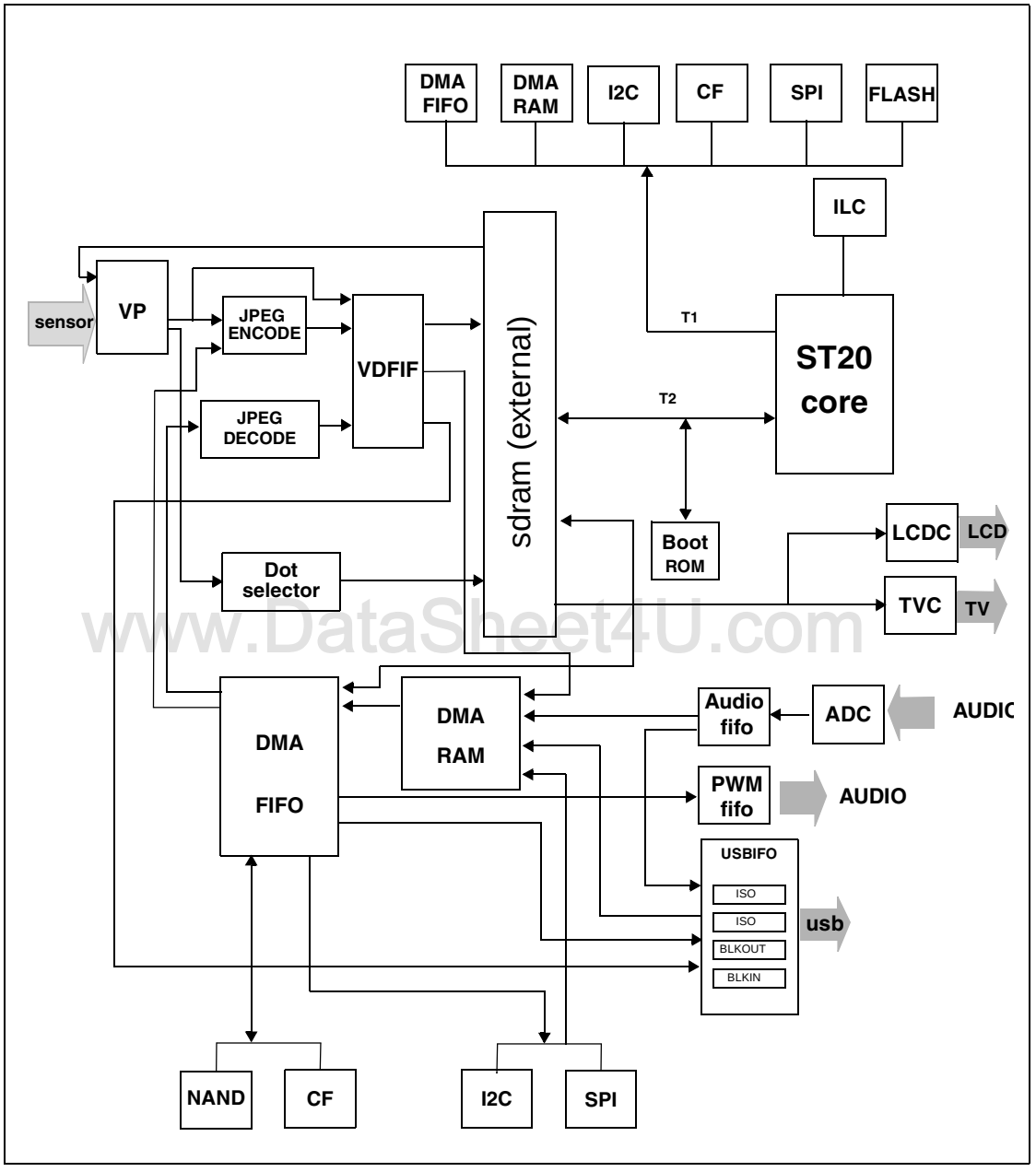
Figure 2: STV0684 functional block diagram



2 Signal Description

Figure 3: Signals identified by functional group

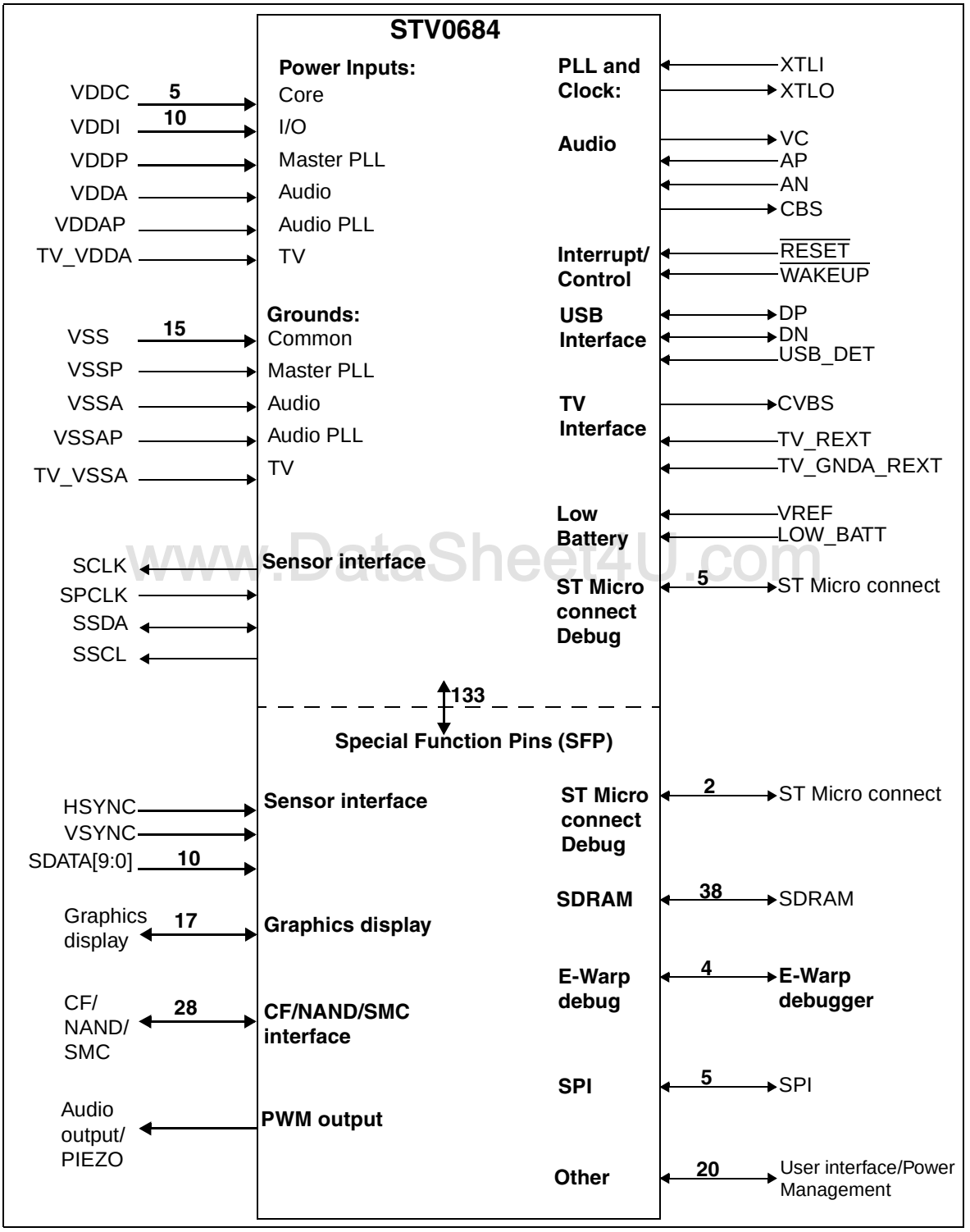


Table 1: STV0684 signal description[1]

Pin name	Location	Type	SFP number	Description
Power supplies: total 38 pins				
VDDI1	L12	S		VDD IO Supply 3.3V
VDDI2	G13	S		VDD IO Supply 3.3V
VDDI3	F10	S		VDD IO Supply 3.3V
VDDI4	F7	S		VDD IO Supply 3.3V
VDDI5	F4	S		VDD IO Supply 3.3V
VDDI6	K3	S		VDD IO Supply 3.3V
VDDI7	N3	S		VDD IO Supply 3.3V
VDDI8	P5	S		VDD IO Supply 3.3V
VDDI9	N6	S		VDD IO Supply 3.3V
VDDI10	K8	S		VDD IO Supply 3.3V
VDDC1	G8	S		VDD CORE supply 1.8V
VDDC2	C7	S		VDD CORE supply 1.8V
VDDC3	F2	S		VDD CORE supply 1.8V
VDDC4	M5	S		VDD CORE supply 1.8V
VDDC5	M11	S		VDD CORE supply 1.8V
VSS	L13	S		GROUND
VSS	H8	S		GROUND
VSS	F14	S		GROUND
VSS	E13			GROUND
VSS	B7	S		GROUND
VSS	A7	S		GROUND
VSS	F6	S		GROUND
VSS	G6	S		GROUND
VSS	K4	S		GROUND
VSS	P2	S		GROUND
VSS	P4	S		GROUND
VSS	M6	S		GROUND
VSS	M7	S		GROUND
VSS	P8	S		GROUND
VSS	N11	S		GROUND
VDDP	D8	S		PLL core supply 3.3V
VSSP	E8	S		PLL core GND
TV_VDDA	A12	S		TV core supply 3.3V

Table 1: STV0684 signal description[1]

Pin name	Location	Type	SFP number	Description
TV_VSSA	B12	S		TV core GND
VDDA	C10	S		Audio analog power supply 3.3V
VSSA	B11	S		Audio analog ground
VDDAP	B14	S		Audio PLL supply 1.8V
VSSAP	C13	S		Audio PLL ground
Sensor interface: total 16 pins of which 12 are SFPs				
SDATA0	N8	I	SFP80	Sensor interface Bit0
SDATA1	M9	I	SFP81	Sensor interface Bit1
SDATA2	J8	I	SFP82	Sensor interface Bit2
SDATA3	L9	I	SFP83	Sensor interface Bit3
SDATA4	P9	I	SFP84	Sensor interface Bit4
SDATA5	N9	I	SPF85	Sensor interface Bit5
SDATA6	K9	I	SFP86	Sensor interface Bit6
SDATA7	P10	I	SFP87	Sensor interface Bit7
SDATA8	L10	I	SFP88	Sensor interface Bit8
SDATA9	N10	I	SFP89	Sensor interface Bit9
HSYNC	M10	I	SFP90	Horizontal synchronization
VSYNC	P11	I	SFP91	Vertical Synchronization
SCLK	N12	O		Clock supplied to the sensor
SPCLK	P14	I		Data qualifying clock from the sensor
SSDA	P12	I/O		I^2C Data line
SSCL	P13	I/O		I^2C clock line
SDRAM interface: total 38 pins all of which are SFPs				
DQ0	L14	I/O	SFP101	SDRAM
DQ1	N13	I/O	SFP92	SDRAM
DQ2	J9	I/O	SFP102	SDRAM
DQ3	N14	I/O	SFP93	SDRAM
DQ4	J10	I/O	SFP103	SDRAM
DQ5	M12	I/O	SFP94	SDRAM
DQ6	K13	I/O	SFP104	SDRAM
DQ7	L11	I/O	SFP95	SDRAM
DQ8	K10	I/O	SFP96	SDRAM
DQ9	J11	I/O	SFP105	SDRAM
DQ10	M13	I/O	SFP97	SDRAM

Table 1: STV0684 signal description[1]

Pin name	Location	Type	SFP number	Description
DQ11	J12	I/O	SFP106	SDRAM
DQ12	M14	I/O	SFP98	SDRAM
DQ13	J13	I/O	SFP107	SDRAM
DQ14	K11	I/O	SFP99	SDRAM
DQ15	K14	I/O	SFP108	SDRAM
DQML	K12	I/O	SFP100	SDRAM
A0	H10	I/O	SFP109	SDRAM
A1	J14	I/O	SFP110	SDRAM
A2	H11	I/O	SFP111	SDRAM
A3	H12	I/O	SFP112	SDRAM
A4	H9	I/O	SFP113	SDRAM
A5	H14	I/O	SFP114	SDRAM
A6	H13	I/O	SFP115	SDRAM
A7	G10	I/O	SFP116	SDRAM
A8	G14	I/O	SFP117	SDRAM
A9	G11	I/O	SFP118	SDRAM
A10	G12	I/O	SFP119	SDRAM
A11	G9	I/O	SFP120	SDRAM
A12	F13	I/O	SFP121	SDRAM
BA0	E14	I/O	SFP122	SDRAM
BA1	F12	I/O	SFP123	SDRAM
CLK	F11	I/O	SFP124	SDRAM
CKE	D14	I/O	SFP125	SDRAM
DQMH	E12	I/O	SFP126	SDRAM
RAS	D13	I/O	SFP127	SDRAM
CAS	E11	I/O	SFP128	SDRAM
WE	D12	I/O	SFP129	SDRAM

Table 1: STV0684 signal description[1]

Pin name	Location	Type	SFP number	Description
Graphics LCD interface: total 18 pins of which all are SFPs				
L_LP	L5	I/O	SFP63	LCD interface
L_RES	M4	I/O	SFP64	LCD interface
L_XINH	N4	I/O	SFP65	LCD interface
L_XSCL	P3	I/O	SFP66	LCD interface
L_FRYP	N5	I/O	SFP67	LCD interface
L_FRYS	L6	I/O	SFP68	LCD interface
L_DY / PNL_CLK	K6	I/O	SFP69	LCD interface
L_YSCL / HSYNC	J6	I/O	SFP70	LCD interface
L_YSCLD / VSYNC	P6	I/O	SFP71	LCD interface
L_DOUT0	H7	I/O	SFP72	LCD interface
L_DOUT1	P7	I/O	SFP73	LCD interface
L_DOUT2	K7	I/O	SFP74	LCD interface
L_DOUT3	J7	I/O	SFP75	LCD interface
L_DOUT4	L7	I/O	SFP76	LCD interface
L_DOUT5	N7	I/O	SFP77	LCD interface
L_FRX / Data6	M8	I/O	SFP78	LCD interface
L_GCP / Data7	L8	I/O	SFP79	LCD interface
BACKLIGHT	B6	I/O	SFP13	LCD interface / GPIO
TV interface: total 3 pins				
CVBS	C12	ANA		CVBS out
TV_REXT	B13	ANA		TV Reference voltage
TV_GNDA_REXT	A13	ANA		TV Reference voltage
SPI (used for MMC, SD): total 5 pins all of which are SFPs				
SPI_MISO	B10	I/O	SFP1	Master In Slave Out
SPI_MOSI	F9	I/O	SFP2	Master Out Slave In
SPI_SLK	D9	I/O	SFP3	SPI clock
SPI_SS	B9	I/O	SFP4	SPI slave/host selection
SPI CS	E9	I/O	SFP5	SPI Chip select

Table 1: STV0684 signal description[1]

Pin name	Location	Type	SFP number	Description
Audio interface: total 6 pins of which 2 are sfps				
CBS	C11	ANA		Audio Vbias
AP	A11	ANA		Audio ADC Differential input
AN	D10	ANA		Audio ADC differential input
VC	C14	ANA		Audio PLL filter
PWM OUT	E10	I/O	SFP0	DAC: Pulse Width Modulator output
$\overline{\text{ENABLE}}$	C6	I/O	SFP17	ENABLE external audio amplifier
NAND (Smartmedia) & Compact-flash interface: total 29 pins all of which are SFPs				
IO0	E4	I/O	SFP35	SMC D0 - CF D00
IO1	E3	I/O	SFP36	SMC D1 - CF D01
IO2	D1	I/O	SFP37	SMC D2 - CF D02
IO3	E2	I/O	SFP38	SMC D3 - CF D03
IO4	E1	I/O	SFP39	SMC D4 - CF D04
IO5	F5	I/O	SFP40	SMC D5 - CF DO5
IO6	F3	I/O	SFP41	SMC D6 - CF DO6
IO7	G3	I/O	SFP42	SMC D7 - CF DO7
$\overline{\text{NAND CS}}$	F1	I/O	SFP43	Nand Chip select
$\overline{\text{WE}}$	G7	I/O	SFP44	SMC $\overline{\text{WE}}$ - CF $\overline{\text{WE}}$
ALE $\overline{\text{OE}}$	G2	I/O	SFP45	SMC ALE - CF $\overline{\text{OE}}$
CLE RDY	J1	I/O	SFP46	SMC CLE - CF READY
RB $\overline{\text{WAIT}}$	J4	I/O	SFP47	SMC R/-B - CF $\overline{\text{WAIT}}$
$\overline{\text{RE}}$ $\overline{\text{REG}}$	J2	I/O	SFP48	SMC $\overline{\text{RE}}$ - CF $\overline{\text{REG}}$
$\overline{\text{CS}}$ $\overline{\text{CARD EN}}$	J5	I/O	SFP49	SMC $\overline{\text{CS}}$ - CF $\overline{\text{CE1}}$
WRIT_PROT $\overline{\text{CARD DET1}}$	K1	I/O	SFP50	SMC $\overline{\text{WP}}$ - CF WP
CARD_DET $\overline{\text{CARD DET2}}$	K5	I/O	SFP51	SMC CD - CF CD1
CFA0	K2	I/O	SFP52	CF A00
CFA1	L1	I/O	SFP53	CF A01
CFA2	L2	I/O	SFP54	CF A02
CFA3	L3	I/O	SFP55	CF A03
CFA4	M1	I/O	SFP56	CF AO4
CFA5	M2	I/O	SFP57	CF A05
CFA6	N1	I/O	SFP58	CF A06
CFA7	N2	I/O	SFP59	CF A07

Table 1: STV0684 signal description[1]

Pin name	Location	Type	SFP number	Description
CFA8	M3	I/O	SFP60	CF A08
CFA9	P1	I/O	SFP61	CF AO9
CFA10	L4	I/O	SFP62	CF A10
User Interface - (Application specific SFP): total 16 pins all of which are SFPs				
$\overline{\text{MODE UP}}$	F8	I/O	SFP6	see firmware manual
$\overline{\text{MODE DOWN}}$	A10	I/O	SFP7	see firmware manual
$\overline{\text{SELECT}}$	C9	I/O	SFP8	see firmware manual
$\overline{\text{CANCEL}}$	A9	I/O	SFP9	see firmware manual
$\overline{\text{SHUTTER}}$	D7	I/O	SFP12	see firmware manual
$\overline{\text{LED0}}$	A5	I/O	SFP18	see firmware manual
$\overline{\text{LED1}}$	B5	I/O	SFP19	see firmware manual
FLASH RDY	B8	I/O	SFP10	see firmware manual
FLASH TRIGGER	E5	I/O	SFP20	see firmware manual
POWER OFF	E7	I/O	SFP11	see firmware manual
POWER DOWN	A6	I/O	SFP14	see firmware manual
SNAP	B4	I/O	SFP24	Sensor interface
SHUTTER_CNTL1	D5	I/O	SFP21	mechanical shutter interface
SHUTTER_CNTL2	A4	I/O	SFP22	mechanical shutter interface
SHUTTER_CNTL3	C5	I/O	SFP23	mechanical shutter interface
SUSPEND	E6	I/O	SFP15	Sensor suspend pin
General Purpose Input/Output: total 11 pins all of which are SFPs				
GPIO0	B3	I/O	SFP28	General purpose IO
GPIO1	A2	I/O	SFP29	General purpose IO
GPIO2	C3	I/O	SFP30	General purpose IO / JTAG TRIG EWARP
GPIO3	B2	I/O	SFP31	General purpose IO / JTAG TDI EWARP
GPIO4	A1	I/O	SFP32	General purpose IO / JTAG TDO EWARP
GPIO5	B1	I/O	SFP33	General purpose IO / JTAG TMS EWARP
GPIO6	C2	I/O	SFP34	General purpose IO / JTAG TCK EWARP
GPIO7	D3	I/O	SFP130	General purpose IO
GPIO8	C4	I/O	SFP25	General purpose IO
GPIO9	A3	I/O	SFP26	General purpose IO
GPIO10	D4	I/O	SFP27	General purpose IO

Table 1: STV0684 signal description[1]

Pin name	Location	Type	SFP number	Description
USB interface: total 4 pins of which 1 is a SFP				
DP	G4	I/O		USB DATAP
DN	G5	I/O		USB DATAN
DETECT	G1	I/O		High when USB VCC present
USB TX_EN	D6	I/O	SFP16	
Battery level detector: total 2 pins				
LOW_BATT	A14	ANA		Battery level input
VREF	D11	ANA		Reference for the battery voltage
CLOCK, Reset, system signals: total 4 pins				
Xtal in	C8	ANA		27 Mhz Crystal input
Xtal out	A8	ANA		27 MHz Crystal Output
$\overline{\text{RESET}}$	C1	I		RESET INPUT
$\overline{\text{WAKE\_UP}}$	D2	I/O		
Debug and test interface: total 7 pins of which 2 are SFPs				
UP_TRIGI	H5	I/O	SFP131	ST20 microconnect debug interface
UP_TRIGO	H4	I/O	SFP132	ST20 microconnect debug interface
UP_TDI	H1	I		ST20 microconnect debug interface
UP_TDO	H2	O		ST20 microconnect debug interface
UP_TMS	J3	I		ST20 microconnect debug interface
UP_TCK	H6	I		ST20 microconnect debug interface
UP_RST	H3	I		ST20 microconnect debug interface

1. This is preliminary information that may be subject to change

3 Functional Description

3.1 Video processor (VP)

The VP is the result of STMicroelectronics extensive know-how and hard work around the colour science for CMOS sensor. The VP block fulfills many functions related to colour reconstruction from a bayer filter, colour matrixing and sharpening, real-time and programmable defect pixel correction, AGC, AWB, Anti flicker and Gamma correction, scaling from the sensor to the required video and LCD panel resolution. This new video processor benefits from STMicroelectronics latest algorithms development such as the patented Noise Reduction Algorithm and anti-vignetting that ensures the highest quality standard.

The VP combines hardware and firmware. The main block controller is powered by a 8051 E WARP microcontroller, with RAM based firmware for the highest level of flexibility.

Feature list

System features

- RAM based firmware
- Dual video interface for simultaneous ViewFinder and movie capture
- Bayer or YCbCr input from supported memory
- 48Mpixel/s capable processing pipe
- Flashgun and shutter support
- RGB/YUV 4:2:2 output formats

Image reconstruction functions

- x2, x2.5 Horizontal downscaling
- Colour Channel Gains and Offsets
- Anti-vignetting
- Defect correction
- NoRA - Active Noise Reduction
- Demosaic (bayer->rgb conv)
- YUV matrix (rgb -> YUV)
- Image crop
- General purpose RGB downscaler
- RGB matrix
- Peaking
- Gamma correction

Statistics processor

- 4 Accumulators - programmable on the fly
- Programmable zones

Image control functions (Tasks handled by the EWARP processor)

- Sensor detection, initialisation and configuration
- VP mode management: stills, streaming etc.
- Automatic Exposure Control, Automatic White balance
- Flicker correction
- Dampening/Promotion Tasks
- Scaler Management
- Dark Calibration
- Flashgun control
- Shutter control

3.2 ST20-C103 core

The ST20 core is the heart of the STV0684 system-on-chip. The processor can execute its code from either the 64KB of private SRAM or directly from the external SDRAM. Instruction/Data cache ensure a fast code execution.

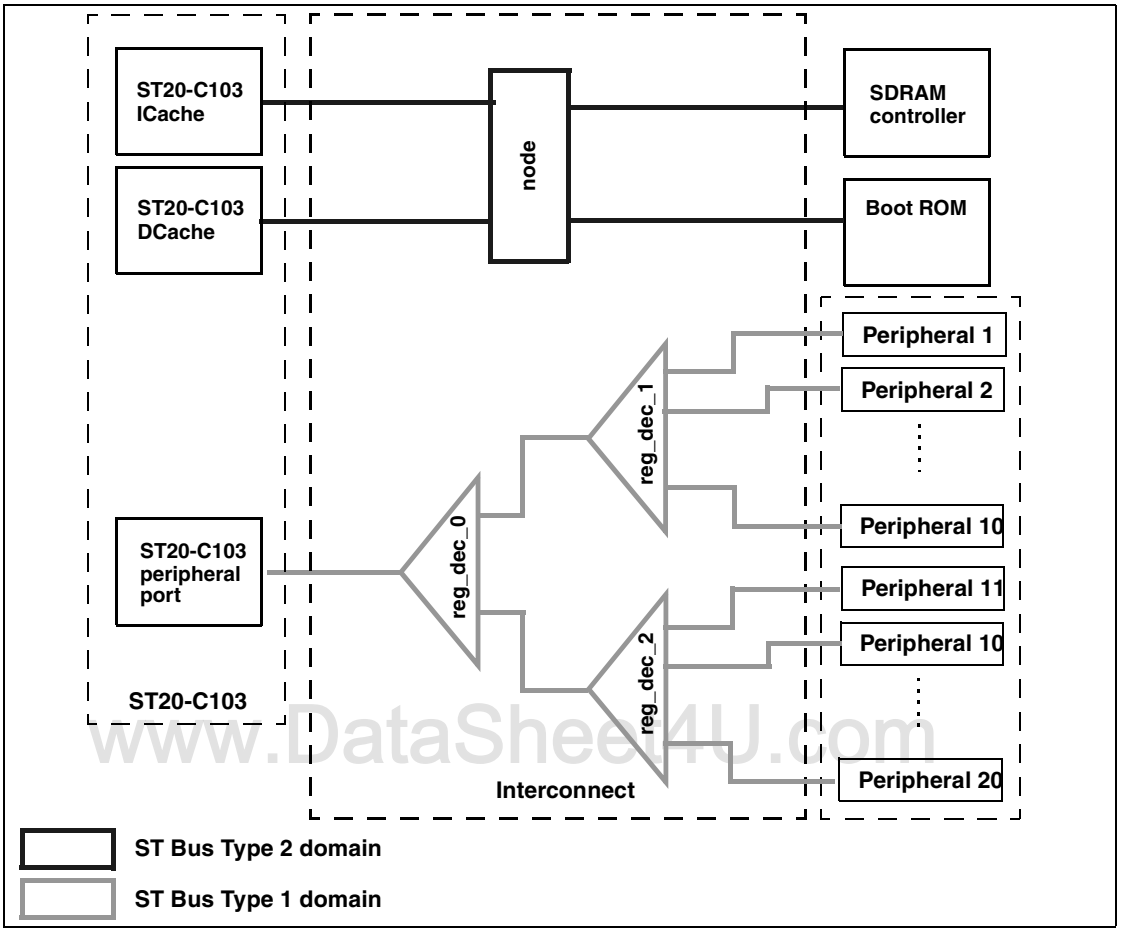
A boot loader residing in a ROM of the device provides capability to boot the system by copying the application firmware image from Non Volatile Memory (SPI Flash or Standard NAND Flash) to the program SRAM or SDRAM memory. This mechanism ensures the lowest system cost by storing the application firmware on a cheap mass storage memory and thus avoiding the extra cost of a NOR type memory. The boot loader also provides the useful possibility to upgrade the Application Firmware and therefore program cameras on the factory line.

The ST20-C103 core includes the following:

- ST20C1 processor running at 48 MHz frequency
- diagnostic control unit DCU3 (4 compare, 4 capture, trace) for debug and code development
- PWM4 timer, INTC2 interrupt controller (16 inputs)
- 64K local RAM (SRAM)
- 4K D-cache & 4K I-cache instruction and data caches memory arbiter

Core architecture and block diagram

Figure 4: ST20DC3 architecture and block diagram



3.3 SFP module

The SFP module is based on reconfigurable device pins combined with some local logic to maximize in-system flexibility of the device in any given application

An SFP can be configured either to be driven as a GPIO or by the local logic block within the STV0684 (detailed in *Figure 3*). The functionality and configuration of each SFP is determined and managed under control of the ST20. Control registers local to each module are mapped into the processors address space, this leaves the processor to support more demanding, computational intensive tasks.

3.4 USB interface

The USB interface fulfills the three following functions:

- The first function is to download from the camera to the PC all the various objects stored on the mass storage media. The STV0684 uses mass storage class, Bulk Only Transfer to ensure seamless connection with most of the Operating System on the market, including PC and Mac platforms.
- The second function is to stream concurrent audio and video through isochronous endpoints. Once again, the STV0684 follow established and newly developed standards to ensure the lowest burden of driver development. The STV0684 is USB Audio class and USB video class Compliant.
- The third function allows the download of the system program code, necessary to run the application, to either serial Flash or NAND flash soldered on the main camera PCB. This function is extremely convenient when programming the cameras on the manufacturing lines and is not open to final users.

Features

- USB 2.0 Compliant (Full speed device)
- Full speed (12 Mbps) signalling bit rate
- USB Audio Class Compliant
- USB Video Class Compliant
- USB Mass Storage Compliant, Bulk only Transfer protocol
- Simultaneously accessible endpoints:
  - ➢ Isochronous endpoint (IN) for video
  - ➢ Isochronous endpoint (IN) for audio
  - ➢ Bulk endpoint (IN) for download
  - ➢ Bulk endpoint (OUT) for download
  - ➢ Interrupt endpoint (IN)
  - ➢ Control pipe

3.5 Memory interface

Description

The memory control Block provides dedicated support for embedded SRAM, external SDRAM, NAND, Smartmedia and Compact Flash (via SFP pins).

Embedded SRAM

- Full-speed random read/write access from the ST20 to embedded SRAM
- Full-speed embedded SRAM address generation for real-time data writes from the compression engine, the Video Processor block, SPI, the audio block and the USB module
- Full-speed embedded SRAM address generation for data reads to the DMA out FIFO

Selection of the source/destination modules is managed by firmware.

External SDRAM

- ST20 memory mapped accesses to external SDRAM
- Full-speed embedded SDRAM address generation for real-time data writes from VDFIF (for VC and VP modules) or DMA out FIFO
- Full-speed external SDRAM address generation/control to DMA out FIFO, TV FIFO, LCD FIFO or VP FIFO's
- Operation with PC100 (or better e.g. PC133) and JEDEC Standard No. 21-C compliant devices and supports 64MB, 128MB, 256MB and 512MB parts with a 16-bit bus width

Mass storage media support

- Compact-flash support
- SmartMedia Card support
- NAND flash memory with a 512B+16 page organization, ECC done by hardware, 32Mbit to 1Gbit devices
- Support for Multi-Media card and Secure Digital with the SPI interface

3.6 Audio interface

The STV0684 includes every step of the processing chain required to record, compress, decompress and playback audio. The STV0684 features a high quality 16 bit sigma delta analog to digital converter including automatic level control and noise gating, as well as volume control. It also features an ADPCM CODEC to maximize the length of audio and AVI clips on a given mass storage media. Finally, the product features a digital to analog converter (PWM followed by RC filters) to directly address a speaker or buzzer for audio playback.

3.6.1 Audio record

The audio record block consists two main blocks the analogue front end and a 16bit delta-sigma ADC. The front end includes the functions of automatic level control and noise gate, and volume control, the ADC uses sampling frequencies of 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz and 48kHz, with either differential or single ended inputs. The sampled output can be 8 or 16 bit. The output of the ACD is then available to the ADPCM module giving an audio compression ratio of 4 to 1.

3.6.2 Audio playback

Audio playback is achieved by an internal Pulse Width Modulator with a sample rates of 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz or 44.1kHz, connected to either an external amplifier chip and loudspeaker/ head phone socket, or to a simple piezo buzzer.

3.7 TV interface

The TV block is composed of a digital encoder that supports PAL and NTSC and a video digital to analog converter (DAC). This interface supports still and video encoding for display on a TV set.

Features

- Supports PAL/NTSC analog TV standards
- Interlaced input data, YCrCb 4:2:2 format
- 16bits x 16words FIFO for buffering incoming display data
- Interrupt generation

3.8 LCD controller - Display interface

The STV0684 LCD controller has been specifically designed to ensure the two following important characteristics:

- Support of low cost panels with a direct interface to digital LCD panels removing the need for an external timing controller IC
- Flexibility with a high-level of programmability on all the signals shapes, polarities and frequencies

The display interface fully supports LCD panel dot selection modes such as Delta, Delta Transverse, Delta Longitudinal and Mosaic and many more by incorporating a dot selector which converts 3dot/pixel input RGB frame data, to 1dot/pixel RGB data.

Basic functionality of the system includes still picture review, viewfinder mode as well as viewfinder mode while recording a video clip.

Features

- Support Thin Film Transistor (TFT) color displays
- 64 or 256 grey level, 256k(18bit)or 16.7Million(24bit) color TFT support
- 6 bit or 8 bit display interfaces
- 16-deep, 16bit deep FIFO for buffering incoming display data
- Resolution programmable up to 1024x1024 pixels
- Programmable timing for different display panels
- Support CASIO, EPSON, and AU optronics panels
- Horizontal, Vertical Sync and Pixel clock signals
- Supports little-endian data formats
- Interrupt generation

3.9 JPEG CODEC

Description

The STV0684 features a compression and a decompression engine that is used for both Still pictures and video clips. The hardware CODEC ensures a fast reaction time of the system to encode and decode data. This is particularly important to minimize the shutter to shutter time and the ability to rapidly display images on a local display or the TV set.

Compression engine The compression engine uses Baseline Sequential JPEG techniques to compress a digital 656 video stream (at up to 12MPixels/s), down to bandwidth that can be transmitted over the USB interface or to a mass storage media, typically 500-900Kbytes/s. It outputs a JPEG data stream with the headers required by standard decoders.

Decompression engine The JPEG decoder block reads the compressed data from the DMA fifo, parses the header and writes back decompressed data back to DMA fifo. This data is organized in 8x8 blocks of the different color components. This data can be converted to raster scan format to be read by the display controller for display on a LCD or TV.

3.10 Other interfaces

3.10.1 SPI

The SPI interface is a generic serial interface that can be used to perform the following functions:

- Support for Multi-media and Secure Digital Cards
- Support for serial flash where code can be located

The SPI supports:

- Full duplex, three-wire synchronous transfers
- Single, master/slave operation selectable either through firmware or hardware
- Programmable clock polarity and phase
- End of transfer interrupt flag
- Write collision flag
- Busy flag indication

3.10.2 I2C

The STV0684 features a hardware I2C master interface and supports the following features:

- I2C protocol
- Standard I2C mode (100 Khz)/Fast I2C mode (400 Khz)
- Single master mode
- Transmitter/Receiver performance
- 7/10 bit addressing
- DMA mode data transfer
- Clock stretching

3.10.3 Comparator for low battery detection

The comparator circuit was designed to compare the battery voltage (after an external resistor divider) with an external reference voltage and generate a low_batt (high when battery voltage is lower than the present threshold) signal for the CPU core.

4 Electrical Characteristics

4.1 Absolute maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDC}	Supply voltage (core)	2.5	V
V_{DDI}	Supply voltage (IO)	4.0	V
V_{DDP}	Supply voltage (PLL)	4.0	V
V_{DDA}	Supply voltage (Audio)	4.0	V
V_{DDAP}	Supply voltage (Audio_PLL)	2.5	V
V_{TV_VDDA}	Supply voltage (TV)	2.5	V
	Current on any signal pin	2	mA
T_{STO}	Storage temperature	-50 to 150	°C
T_{OP}	Operating temperature	0 to 70	°C
T_{LEAD}	Lead temperature (soldering, 10 s)	+260	°C

Caution:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Operating conditions

Table 3: Operating conditions

Symbol	Parameter	Typ.	Unit
V_{DDC}	Supply voltage (core)	1.8	V
V_{DDI}	Supply voltage (IO)	3.3	V
V_{DDP}	Supply voltage (PLL)	3.3	V
V_{DDA}	Supply voltage (Audio)	3.3	V
V_{DDAP}	Supply voltage (Audio_PLL)	1.8	V
V_{TV_VDDA}	Supply voltage (TV)	3.3	V
T_A	Ambient temperature	25	°C

4.3 Thermal data

Table 4: Thermal data

Symbol	Parameter	Value	Unit
Rth(j-a)	Junction-ambient thermal resistance - LFBGA196 (*Note 1*)	50	°C/W

Note: 1 Typical, measured with the component mounted on an evaluation PC board in free air.

4.4 DC electrical characteristics

Over operating conditions unless otherwise specified. Values from *Table 5* and *Table 6* are estimates.

Table 5: DC electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{Il}	Input low voltage (XTAL_IN)	0		0.631	V
V_{Ih}	Input high voltage (XTAL_IN)	1.123		V_{DDC}	V
V_{hys}	Hysteresis (XTAL_IN)		0.492		V
V_{IL}	Input low voltage (SFP pin)[1]	0		0.8	V
V_{IH}	Input high voltage (SFP pin)[1]	2		V_{DDI}	V
V_{HYS}	Schmitt trigger hysteresis (SFP pin)[1]	0.4			V
V_{T+}	Schmitt input low to high threshold voltage (SFP pin)[1]		2.15		V
V_{T-}	Schmitt input high to low threshold voltage (SFP pin)[1]		1.05		V
V_T	Threshold point (SFP pin)[1]		1.65		V
V_{OL}	Output low voltage(SFP pin)			0.4	V
V_{OH}	Output high voltage(SFP pin)	2.4			V
I_{IL}	Input leakage current Input pins I/O pins	1			µA
V_{ILU}	USB differential pad D+/D- input low			0.8	V
V_{IHU}	USB differential pad D+/D- input high (driven)	2.0			V
V_{IHUZ}	USB differential pad D+/D- input high (floating)	2.7		3.6	V
V_{TDI}	USB differential pad D+/D- input sensitivity [2]	0.2			V
V_{CM}	USB differential pad D+/D- common mode voltage [3]	0.8		2.5	V
V_{OLU}	USB differential pad D+/D- output low voltage	0.0		0.3	V
V_{OHU}	USB differential pad D+/D- output high voltage	2.8		3.6	V
V_{CRS}	USB differential pad D+/D- output signal cross over voltage	1.3		2.0	V
Z_{drv}	Driver output resistance	28		44	Ω

1. These figures apply to SFP, SPCLK, SSCL, and SSDA, they do not apply to the XTAL_IN pad
2. $V_{DI} = |(D+)- (D-)|$
3. V_{cm} includes V_{DI} range

Table 6: Power supply specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDC}	Supply voltage (core)	1.65	1.8	1.95	V
V_{DDI}	Supply voltage (IO)	3.0	3.3	3.6	V
V_{DDP}	Supply voltage (PLL)	3.0	3.3	3.6	V
V_{DDA}	Supply voltage (Audio)	3.0	3.3	3.6	V
V_{DDAP}	Supply voltage (Audio_PLL)	1.65	1.8	1.95	V
V_{TV_VDDA}	Supply voltage (TV)	3.0	3.3	3.6	V
$I_{Suspend}$	Core Suspend current		0.2		mA
	IO Suspend current		1.166		mA
	PLL Suspend current			1	µA
	Audio Suspend current			1	µA
	Audio_PLL Suspend current			1	µA
	TV Suspend current			1	µA
$I_{Low\ power}$	Core Low power Current		54.3		mA
	IO Low power Current		6.3		mA
	PLL Low power Current		3.8		mA
	Audio Low power Current		5.9		µA
	Audio_PLL Low power Current		12		µA
	TV Low power Current			1	µA
$I_{Highpower}$	Core High power Current		130		mA
	IO High power Current		17.8		mA
	PLL High power Current		7.74		mA
	Audio High power Current		5.3		mA
	Audio_PLL High power Current		0.23		mA
	TV High power Current		11.63		mA

4.5 AC electrical characteristics

4.5.1 SFP AC parameters

Each SFP is a TTL schmitt trigger bidirectional pad Buffer, 3v3 capable with 2mA drive capability and Slew-rate Control. The 3.3V IOs comply to the EIA/JEDEC standard JESD8-B.

4.5.2 Audio ADC electrical parameters

Table 7: Audio/ADC electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Fclk	Clock frequency			12		MHz
Dutymclk	Clk duty cycle		40		60	%
Fs	Sample frequency		8		48	kHz
Vbias	Bias reference voltage	Vbias / V_{DDA} = 3V		1.5		V
Rbias	Vbias impedance	Vbias		5		kΩ
RIN	Input impedance	IN+ / IN-		50		kΩ
Cin	Input capacitance	IN+ / IN-		10		pF
Dyn In	Input dynamic range	ADC Out Full scale IN+ / IN- Gain 0dB (AGC off)		1.5		Vpp
SNR*	Signal / Noise ratio	Sinewave @FS - 3dB Gain 0dB		82		dB
Offset	Offset error	After automatic calibration			100	LSB
Harm[1]	Signal to peak harmonics	Sinewave @FS - 3dB Gain 0dB	75			dB
		Sinewave @FS - 3dB Gain 24dB	50			dB

1. Input sine wave 1kHz, Fmclk 11.289 MHz, BW = 10Hz-20 kHz, A-weighting filters, output 16 bits RAW PCM

4.5.3 AC electrical characteristics of USB transceiver

All measurements are fully electrically compliant to Chapter 7 (Electrical requirements) of revision 2 of the USB specification for full-speed devices (V1.1). The transceiver has been tested with external impedance-matching series resistors (27 Ω +/-5%) between the pads and the USB cable.

The operation of the USB transceiver is guaranteed through design and application testing.

Table 8: AC characteristics of USB transceiver

Symbol	Description	Min.	Typ.	Max	Unit
Transmit /Output stage					
tlr	Fall time	4.45	5.82	7.31	ns
tlf	Rise time	4.55	5.77	6.81	ns
tlrfm	Rise and fall time matching	90		111	%
System					
Rpu	USB differential pad Dp, Dn pullup Resistor	1.425		1.575	kΩ
Rpd	USB differential pad Dp, Dn pulldown Resistor	14.25		15.75	kΩ

4.5.4 SDRAM timing description

4.5.4.1 Read/Write timing diagrams for external synchronous DRAM

Figure 5: SDRAM read timing

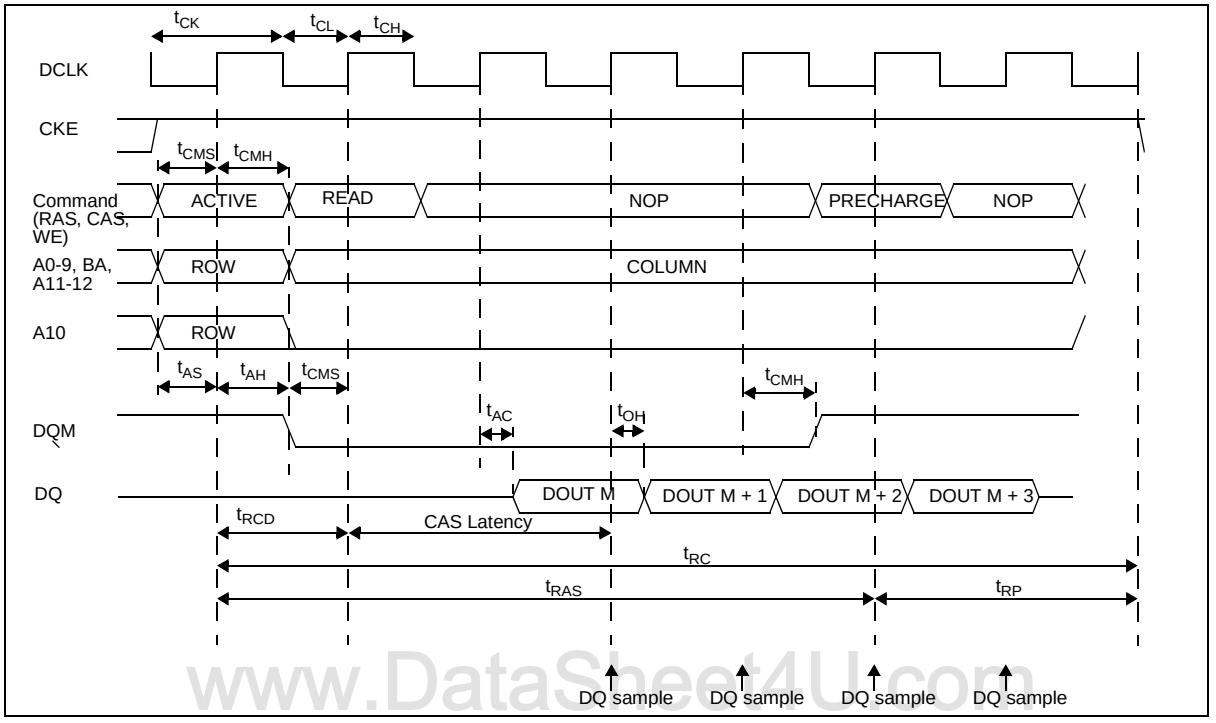


Figure 6: SDRAM write timing

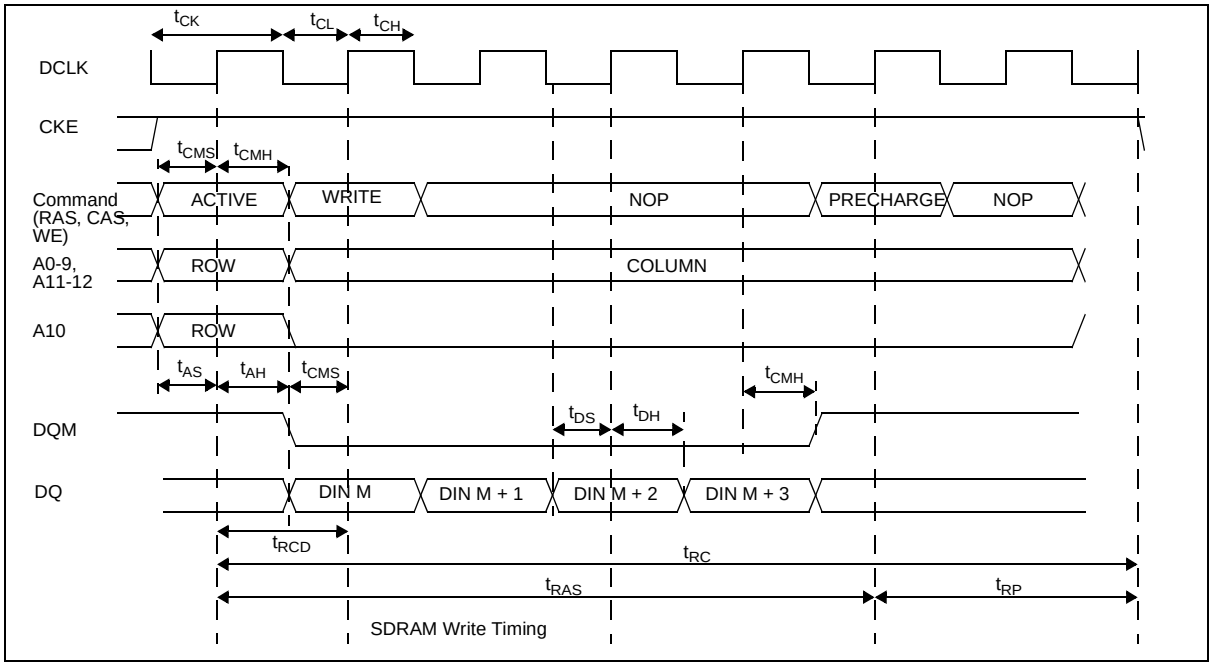


Table 9: SDRAM timing

Symbol	Min	Typ	Max	Units
t_{CK}		41.67		ns
t_{CH}	$t_{CK}/2 - (t_{CK}*0.0345)$	$t_{CK}/2$	$t_{CK}/2 + (t_{CK}*0.0345)$	ns
t_{CL}	$t_{CK}/2 - (t_{CK}*0.0345)$	$t_{CK}/2$	$t_{CK}/2 + (t_{CK}*0.0345)$	ns
t_{AC}			24.8	ns
t_{OH}	0			ns
t_{CMS}	20.3			ns
t_{CMH}	20			ns
t_{AS}	20.7			ns
t_{DS}	20.1			ns
t_{DH}	21.8			ns
t_{RCD}	1			t_{CK}
t_{RAS}	2			t_{CK}
t_{RC}	4			t_{CK}
t_{RP}	2			t_{CK}
t_{RRD}[1]	2			t_{CK}
tah	19.8			ns

1. t_{RRD} = Row active to row active delay

Note: 1 The SDRAM interface is designed to operate with SDRAM devices which are compliant with the Intel SDRAM Specification Revision 1.7 November 1999. Speed grades 66, 100 and 133MHz are compatible.

2 Above timing assumes 20pF load per pad.

4.5.5 I²C timing description

Figure 7: START and STOP conditions

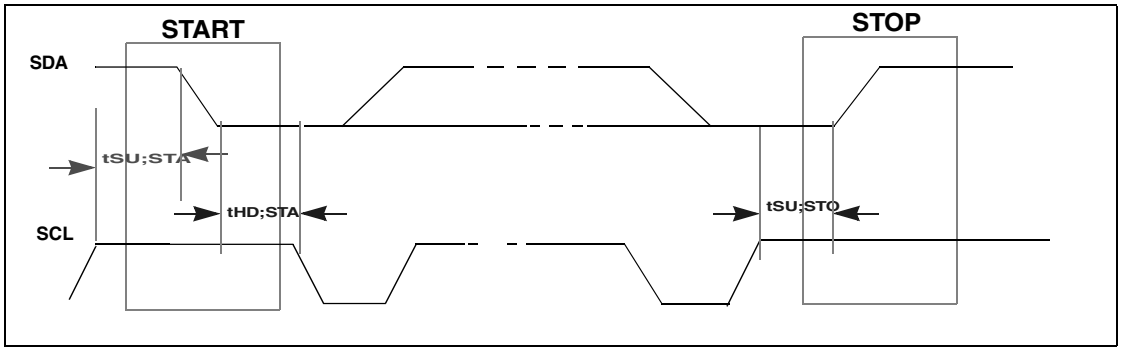


Figure 8: SDA Data valid

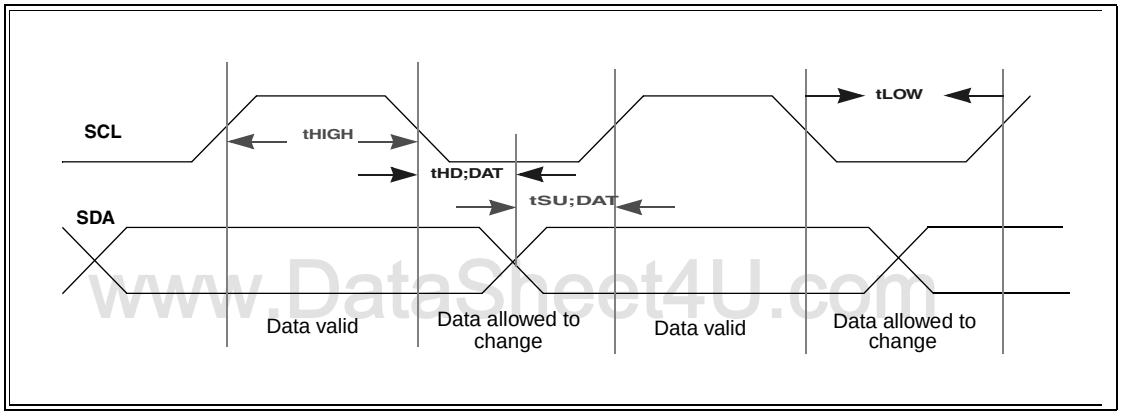
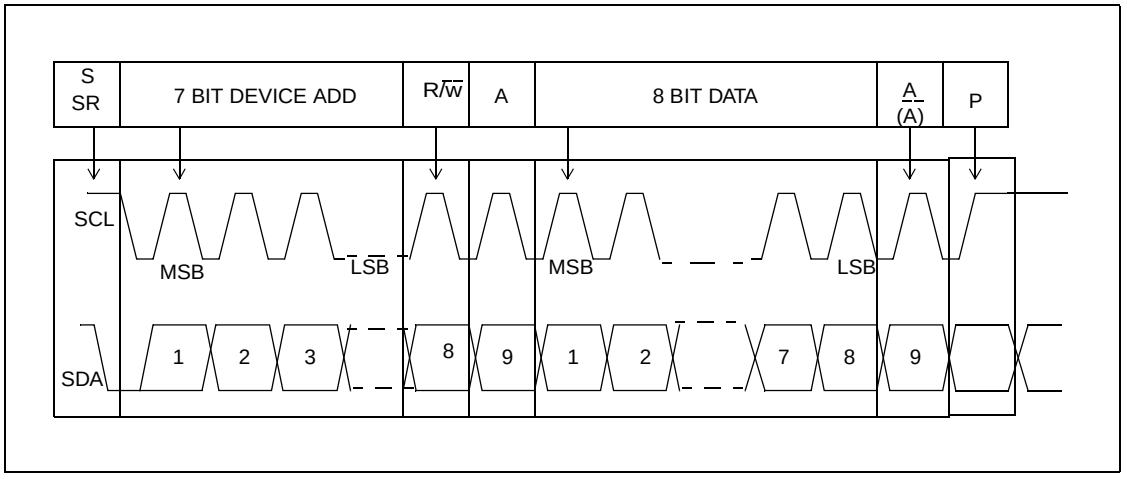


Table 10: I²C timing Spec

Symbol	Parameter	STD mode		FAST mode		Unit
		Min	Max	Min	Max	
f SCL	SCL clock frequency	10	100	10	400	kHz
tLOW	Low period of SCL	4.8	-	1.4	-	µs
tHIGH	High period of SCL	4.8	-	0.9	-	µs
tHD;STA	Hold time for a repeated start	4.8	-	1.4	-	µs
tSU;STA	Setup time for repeated start	4.8	-	0.9	-	µs
tSTU;STO	Setup time for a stop	4.8	-	0.9	-	µs
tHD;DAT	Data hold time	350	-	350	-	ns
tSU;DAT	Data setup time	2.4	-	045	-	µs
tBUF	Bus free time between stop and start	4.8	-	1.4	-	µs

Figure 9: Message format



4.5.6 SPI timing description

It is able to support master and slave mode. The timing given is needed for slave mode and in master mode is able to provide

t_R, t_F = 5ns with output load 30pF

Figure 10: SPI timing diagram

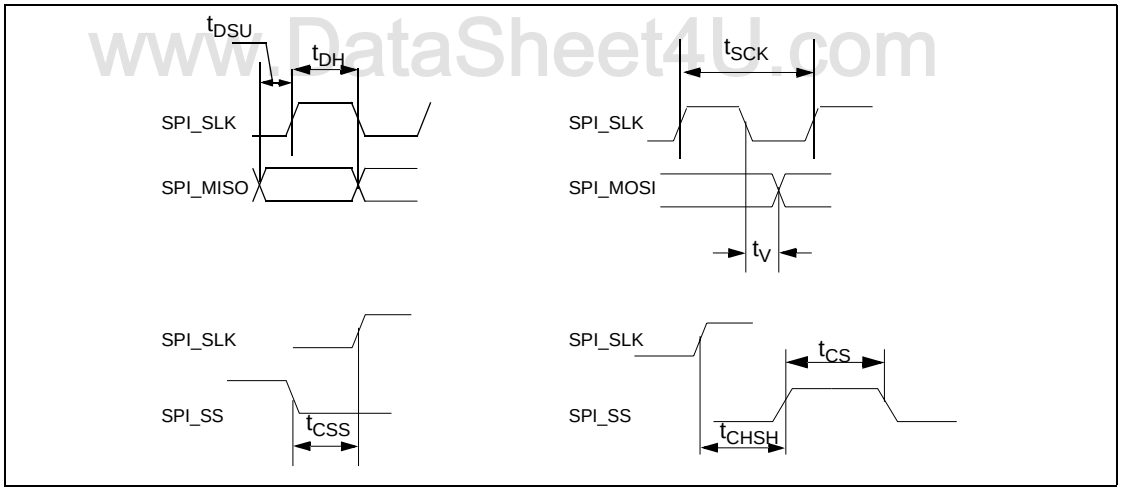


Table 11: SPI timing table

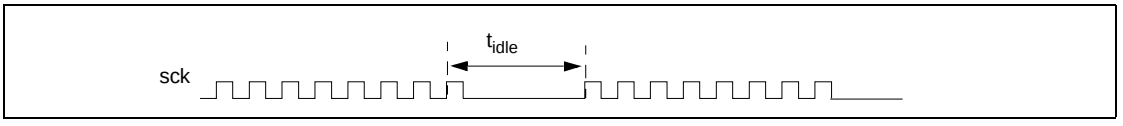
Symbol	Parameter	Min	Max	Units
f_{SCK}	SCK frequency= $1/t_{SCK}$		24 (master) 48 (slave)	MHz
t_{DSU}	Data in Setup time	18(master) 5(slave)		ns
t_{DH}	Data in Hold time	0(master) 5(slave)		ns

Table 11: SPI timing table

Symbol	Parameter	Min	Max	Units
t_{CSS}	$\overline{SS}$ active Setup time, relative to SCK	210(master/ slave)		ns
t_{CHSH}	$\overline{SS}$ active hold time, relative to SCK	50(master/ slave)		ns
t_V	Clock low to output valid		20 (master/slave)	ns
t_{CS}	Minimum $\overline{SS}$ high time	120(slave)		ns
t_{idle}	Idle phase between byte transfer in transmit mode for resynchronisation	120(slave)		ns

In slave mode for resynchronization purpose the need for idle phase between byte transfer is needed for the transmit mode.

Figure 11: Idle phase timing in slave mode



4.5.7 NAND timing description

Figure 12: Command latch cycle for NAND flash interface

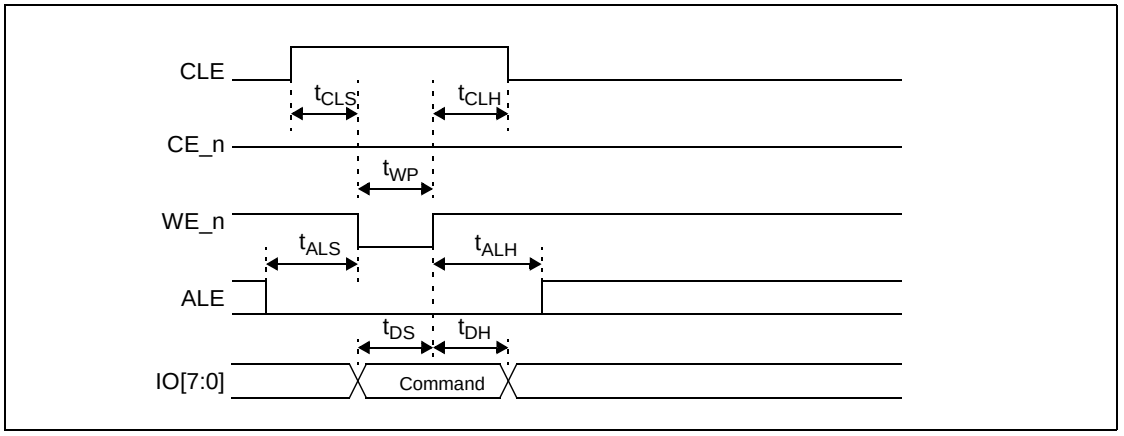


Figure 13: Address latch cycle for NAND flash interface

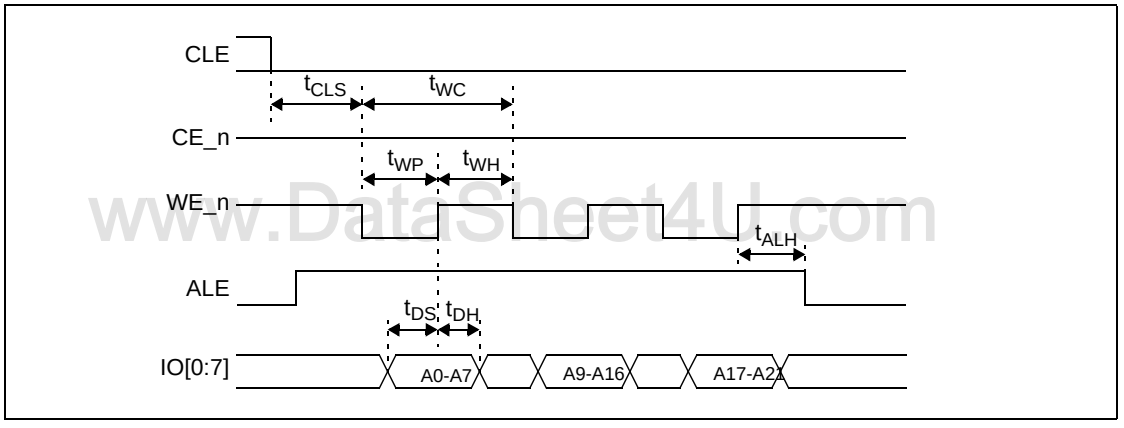


Figure 14: Input data latch cycles for NAND flash interface

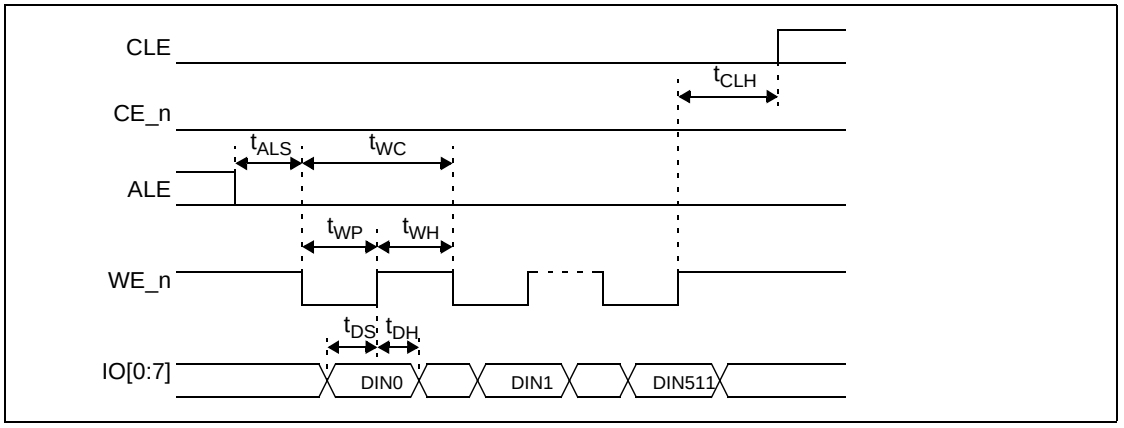


Figure 15: Sequential output cycle after read for NAND flash interface

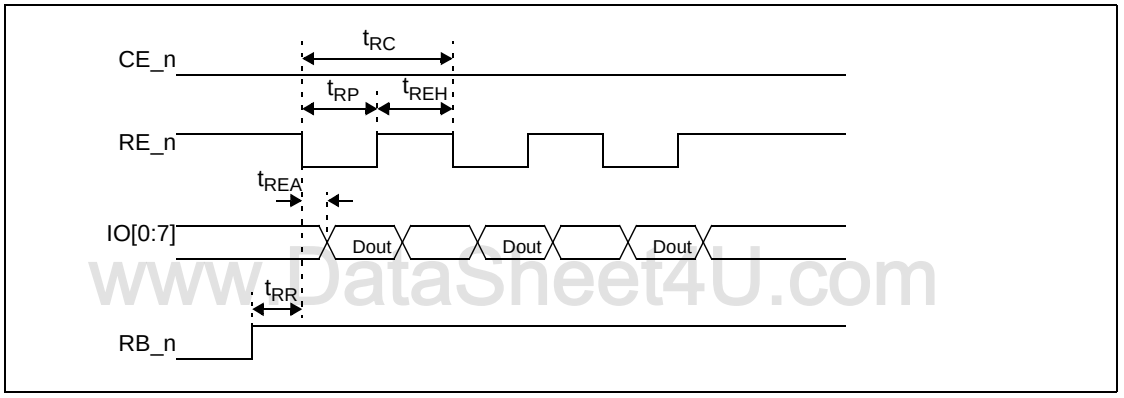


Figure 16: Status read cycle for NAND flash interface

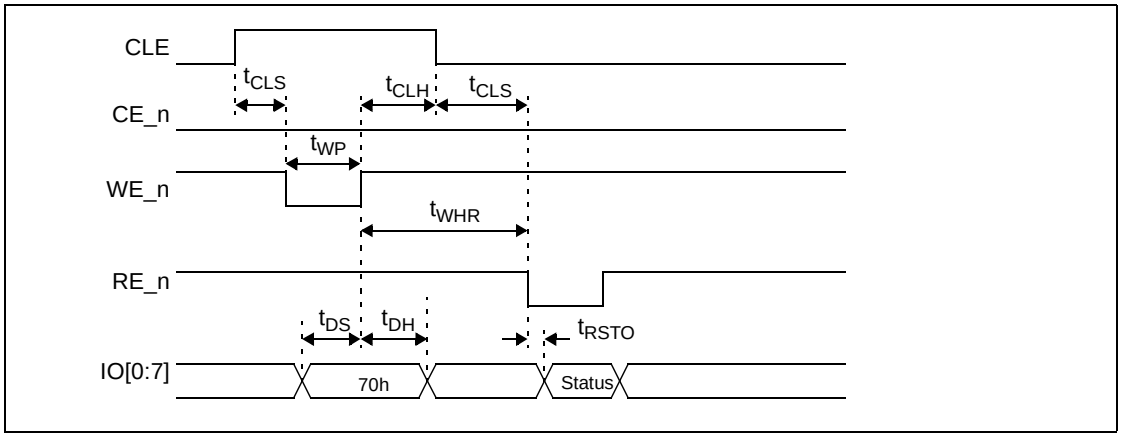


Figure 17: Read operation for NAND flash interface

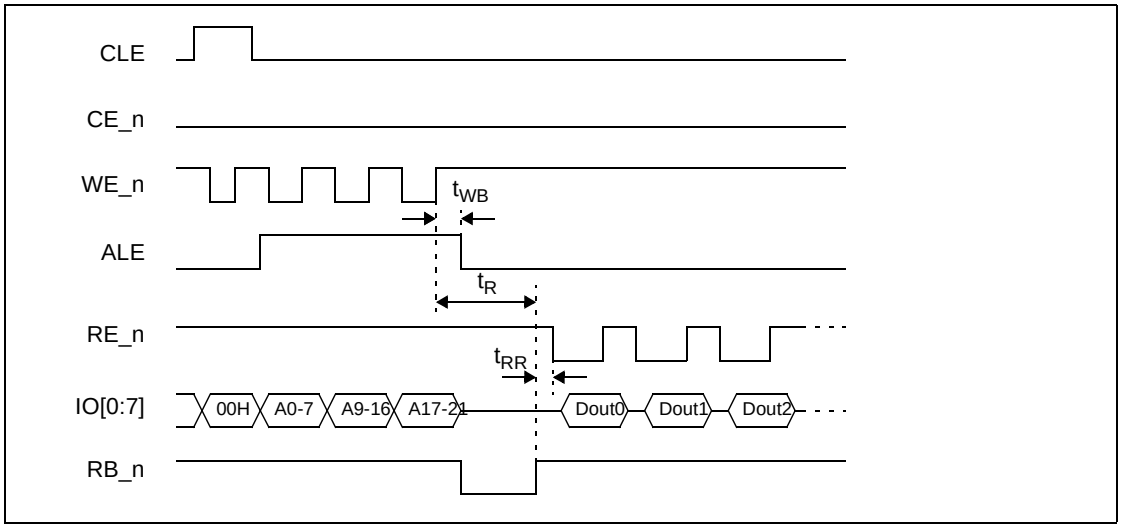
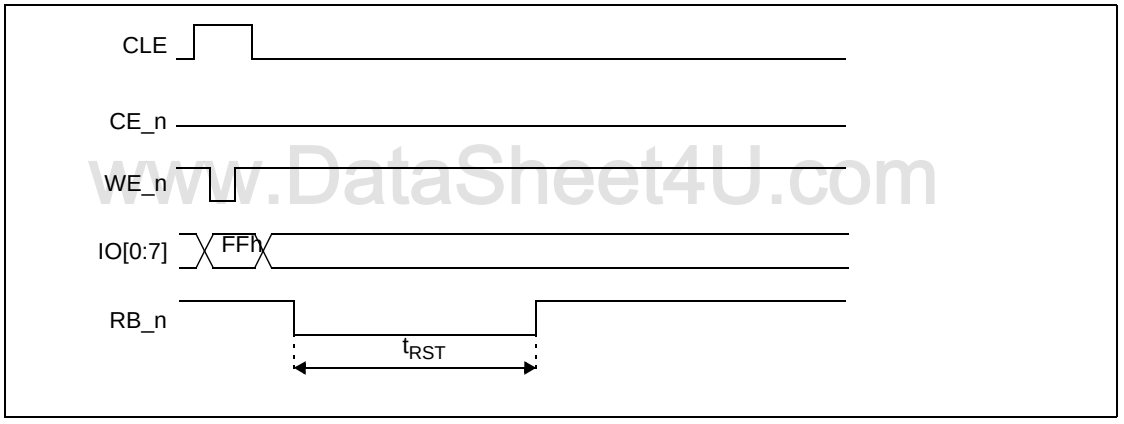


Figure 18: Reset operation for NAND flash interface



4.5.8 AC characteristics for NAND flash operation

Table 12: AC characteristics for NAND flash operation

Symbol	Parameter	Min	Typical	Max	Units
t_{CLS}	CLE Set-up time	61.4	62.4		ns
t_{CLH}	CLE Hold time	83.2			ns
t_{WP}	WE-n Pulse Width	83.2			ns
t_{ALS}	ALE Set-up time	82.6	83.2		ns
t_{ALH}	ALE Hold time	82.4	83.2		ns
t_{DS}	Data Set-up time	82.6	83.2		ns
t_{DH}	Data Hold time	61.8	62.4		ns
t_{WC}	Write Cycle time	145.1	145.6		ns
t_{WH}	WE_n High Hold time	61.9	62.4		ns
t_{RR}	Ready to RE_n Low	81	83		ns
t_{RP}	RE_n Pulse Width	83.2			ns
t_{RC}	Read Cycle time	187.2			ns
t_{REA}	RE_n Access time		35	43.2	ns
t_{REH}	RE_n High Hold time	103.5	104		ns
t_{WHR}	WE_n High to RE_n Low	124.2	124.8		ns
t_{R}	Data Transfer from Cell to Register			25.015	µs
t_{WB}	WE_n High to Busy		41.6	215.3	ns
t_{RST}	Device Resetting (Read)			5.015	µs

Note: 1 All parameters relating to the CE_n signal are omitted as it is not enabled/disabled during execution of any NAND flash operation i.e. it is permanently tied low.

2 All timings are worst case

3 Conforms to both Samsung and Toshiba specifications as outlined in datasheets.

4 The NAND flash timings detailed here are guaranteed by design.

5 The loading factor used for the characterization is equivalent to 40pF.

4.5.9 Compact flash timing

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, direct mapped I/O transfer and memory access. The STV0684 will only support the memory mapped mode.

4.5.9.1 Compact flash pin description

The following table lists the pins of the CF card which are connected to the STV0684.Output refers to pins that are driven by STV0684. Input is those pins that are driven by the CF Card.

Table 13: Pin description

Symbol	Pin Description	Direction	SFP used
CFA0 ~CFA10	Address	Output	52~62
CARD_DET CARD_DET2	Card Detect	Input	50
$\overline{CS}$ $\overline{CARD\ EN}$	Card Enable.	Output	49
IO0~IO7	Data. Only 8 bits of the data bus D[7:0] are used.	Input	35~42
ALE $\overline{OE}$	Output Enable	Output	45
CLE RDY	Ready/Busy	Input	46
$\overline{RE}$ $\overline{REG}$	Register(Attribute) Memory Select	Output	48
RST	Reset		note [1]
RB $\overline{WAIT}$	Wait	Input	47
WE	Write Enable	Output	44

1. The reset may come from the global reset of the system or be driven by a user definable SFP this function is application specific.

4.5.9.2 Compact flash timings

The timings achieved for accessing the attribute and common memory are listed below.There are registers in the CF Controller of the STV0684 in which all these timings can be programmed in terms of number of clocks of 48MHz. All the timings below assume a 48MHz operating clock frequency.

Table 14: CF attribute memory read timing

Symbol	Parameter	Min.	Typ.	Max.	Units
tc(R)	Read Cycle Time	340	-		ns
ta(A)	Address Access Time		-	300	ns
ta(CE)	Card Enable Access Time		-	300	ns
ta(OE)	Output Enable Access Time		-	300	ns
tdis(CE)	Output Disable Time from CE		-	100	ns
tdis(OE)	Output Disable Time from OE		-	100	ns
tsu (A)	Address Setup Time	40	-		ns
ten(CE)	Output Enable Time from CE	5	-		ns
ten(OE)	Output Enable Time from OE	5	-		ns
tv(A)	Data Valid from Address Change	0	-		ns

Figure 19: Attribute memory read timing diagram

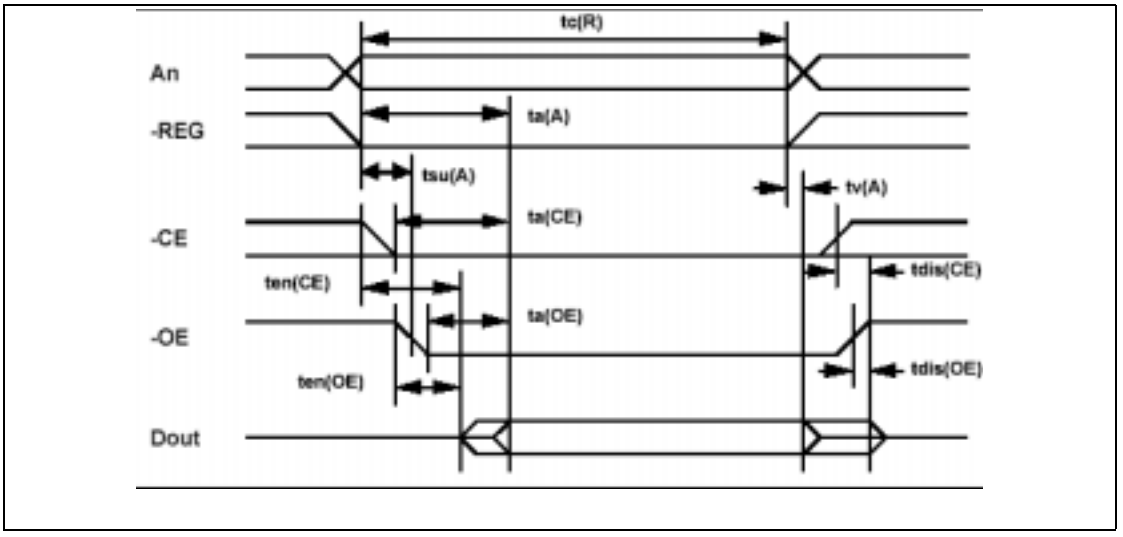


Table 15: Attribute memory write timing

Symbol	Parameter	Min.	Max.	Units
tc(W)	Write Cycle Time	280		ns
tw(WE)	Write Pulse Width	200		ns
tsu(A)	Address Setup Time	40		ns
trec(WE)	Write Recovery Time	40		ns
WE tsu(D-WEH)	Data Setup Time for WE	160		ns
th(D)	Data Hold Time	40		ns

Figure 20: Attribute memory write timing diagram

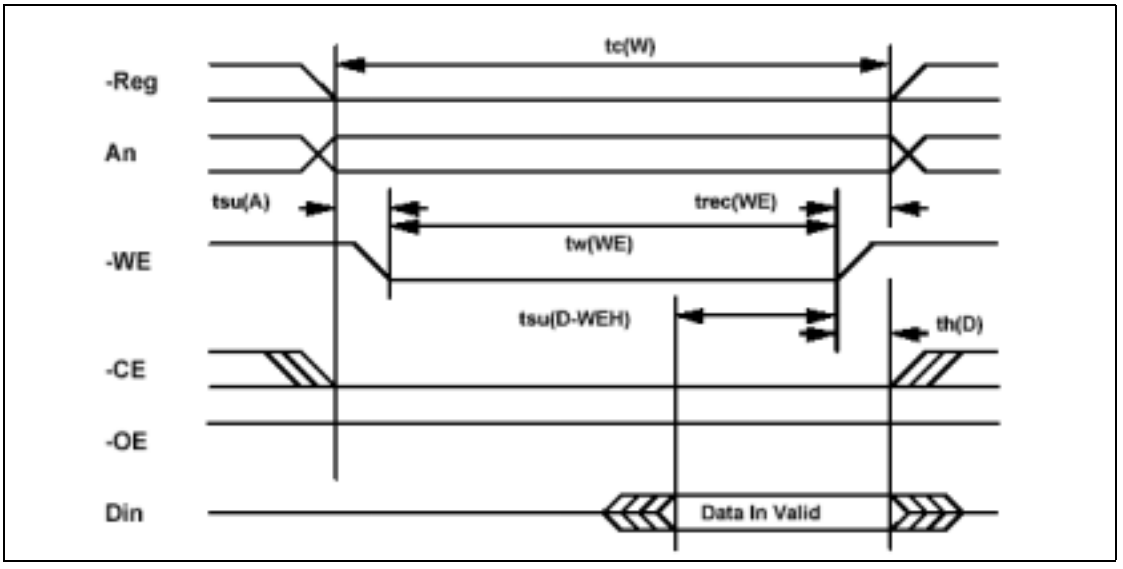


Table 16: Common memory read timing

Symbol	Item	Min.	Max.	Units
ta(OE)	Output Enable Access Time		140	ns
tdis(OE)	Output Disable Time from OE		100	ns
tsu(A)	Address Setup Time	40		ns
th(A)	Address Hold Time	40		ns
tsu(CE)	CE Setup before OE	0		ns
th(CE)	CE Hold following OE	40		ns
tv(WT-OE)	Wait Delay Falling from OE		40	ns
tv(WT)	Data Setup for Wait Release		0	ns
tw(WT)	Wait Width Time		350	ns

Figure 21: Common memory read timing diagram

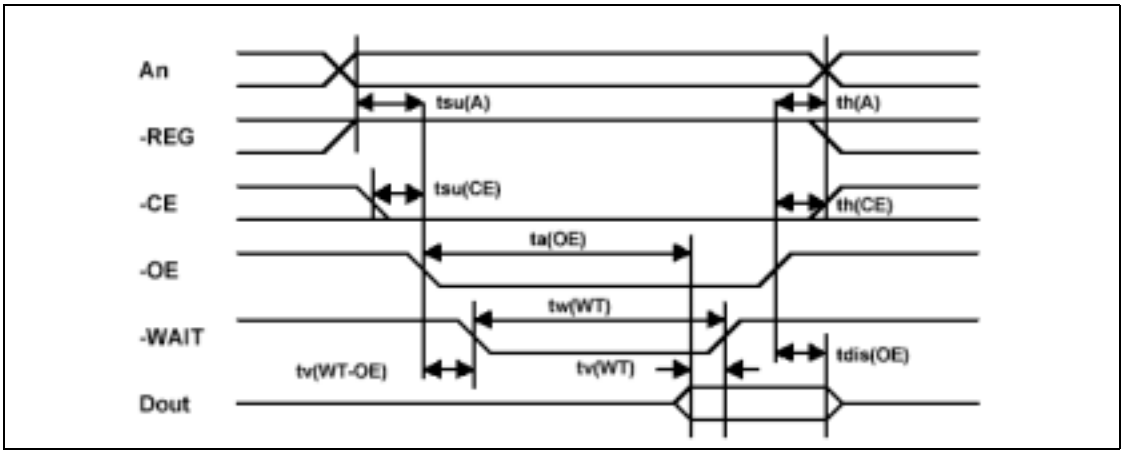


Table 17: Common memory write timing

Symbol	Parameter	Min.	Max.	Units
tsu(D-WEH)	Data Setup before WE	80		ns
th(D)	Data Hold following WE	40		ns
tw(WE)	WE Pulse Width	200		ns
tsu(A)	Address Setup Time	40		ns
tsu(CE)	CE Setup before WE	0		ns
trec(WE)	Write Recovery Time	40		ns
th(A)	Address Hold Time	40		ns
th(CE)	CE Hold following WE	20		ns
tv(WT-WE)	Wait Delay Falling from WE		40	ns
tv(WT)	WE High from Wait Release	0		ns
tw (WT)	Wait Width Time		350	ns

4.5.10 TFT

Table 18: TFT timing

Symbol	Parameter	Min.	Max.	Units
PNL_CLK	Panel clock	1.56	27	MHz
HSYNC[1]	Horizontal Sync	2	1822	PNL_CLK periods
VSYNC[1]	Vertical sync	2	1598	Horizontal sync periods

1. HSYNC & VSYNC are active low (default, but programmable) and the falling edge of both HS & VS are always synchronous.

4.5.11 TV

TV timing description

Table 19: TV timing description

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution			10	Bits
	Recommended load impedance		175		Ω
	Analog output				
	Dynamic current[1]	6.64	8	9.36	mA
	Output voltage[1]			1.6	V DC
	Dynamic performance				
	SNR, BW=10MHz, Fclk=80MHz		50		dB
	THD, BW=10MHz, Fclk=80MHz		50		dB
	Voltage reference				
	V_REXT - TV_GNDA_REXT	-7%	1.4	+7%	V

1. The output current of 8mA = typ: TV_REXT - TV_GNDA_REXT =1.4V, RREF=10000 Ω

TV External components

An external 10000 ohm precision resistor typical 1% placed between the TV_REXT pin and GNDAS_REXT sets the full scale DAC current.

4.5.12 Sensor interface

Figure 22: Timing for sensor input

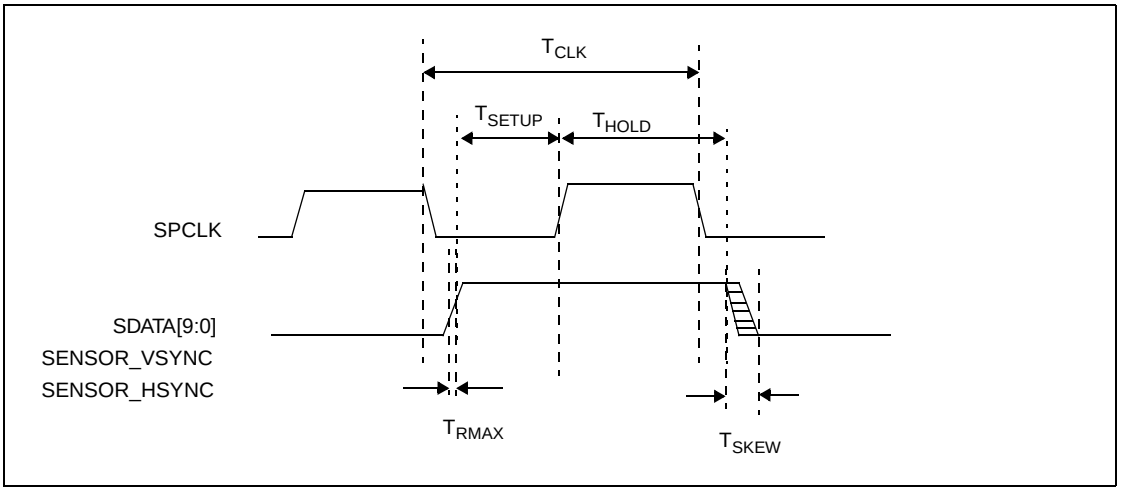


Table 20: Timing for Sensor Input

Symbol	Parameter	Min	Max	Unit
T_{CLK}	SPCLK	20 (50MHz)	1000 (1MHz)	ns
T_{SETUP}	Data valid before clock rising	1.5		ns
T_{HOLD}	Data hold time	$T_{CLK}/2$		
T_{RMAX}	Max transition time (20% to 80%)		1	ns
T_{SKEW}	Data / clock skew		440	ps
	Clock duty cycle	45	55	

4.6 ESD handling characteristics

Table 21: ESD handling characteristics

Test	Criteria	Unit
ESD Machine Model	150	V
ESD Human body	2	kV

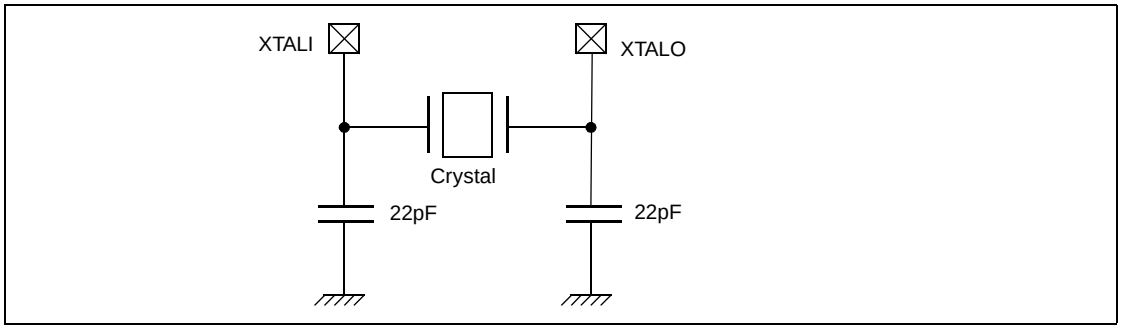
4.7 External circuits

4.7.1 Crystal oscillator

There are 2 crystal oscillator pins XTAL_IN, XTAL_OUT, as shown in Figure 23. The Oscillator cell architecture is a single stage oscillator with an inverter working as an amplifier. The oscillator stage is biased by an internal resistor (>1MΩ). It also requires an external PI network consisting of a crystal and two capacitors.

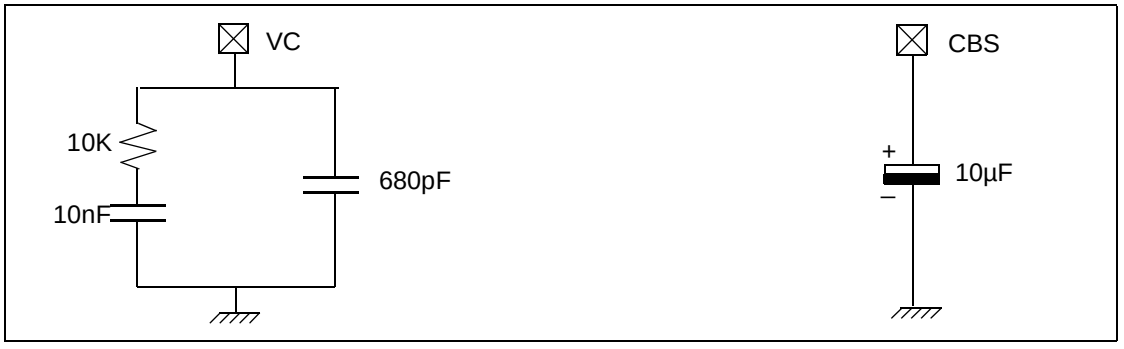
Note: The TV standards requests that the clock accuracy of the oscillator circuit must be 30ppm or less to achieve a 500Hz accuracy for 4.5MHz chroma.

Figure 23: Oscillator support circuit



4.7.2 Audio

Figure 24: Audio PLL filter and CBS



If the record audio section of the STV0684 is not required, AP, CBS, VC and AN can be left unconnected. Power must still be supplied to VDDA and VDDAP.

4.7.3 Recommended power supply decoupling

A 0.1µF bypass capacitor located as close as possible to the chip package connecting between all VDD pins and GND and at least one bulk decoupling capacitor on each of the supply rails VDDA, VDDC, VDDI and VDDP.

5 Package Information

5.1 STV0684 pin assignment

Figure 25: STV0684 pin assignment

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
LOW_BAT	TV_GNDA_REXT	TV_VDDA	AP	SFP7	SFP9	XTALO	VSS_6	SFP14	SFP18	SFP22	SFP26	SFP29	SFP32	A
VDDAP	TV_REXT	TV_VSSA	VSSA	SFP1	SFP4	SFP10	VSS_5	SFP13	SFP19	SFP24	SFP28	SFP31	SFP33	B
VC	VSSAP	CVBS	CBS	VDDA	SFP8	XTALI	VDDC_2	SFP17	SFP23	SFP25	SFP30	SFP34	$\overline{\text{RESET}}$	C
SFP125	SFP127	SFP129	VREF	AN	SFP3	VDDP	SFP12	SFP16	SFP21	SFP27	SFP130	$\overline{\text{WAKEUP}}$	SFP37	D
SFP122	VSS_4	SFP126	SFP128	SFP0	SFP5	VSSP	SFP11	SFP15	SFP20	SFP35	SFP36	SFP38	SFP39	E
VSS_3	SFP121	SFP123	SFP124	VDDI_3	SFP2	SFP6	VDDI_4	VSS_7	SFP40	VDDI_5	SFP41	VDDC_3	SFP43	F
SFP117	VDDI_2	SFP119	SFP118	SFP116	SFP120	VDDC_1	SFP44	VSS_8	DN	DP	SFP42	SFP45	USB_DETECT	G
SFP114	SFP115	SFP112	SFP111	SFP109	SFP113	VSS_2	SFP72	UP_TCK	SFP132	SFP131	UP_RST	UP_TDO	UP_TDI	H
SFP110	SFP107	SFP106	SFP105	SFP103	SFP102	SFP82	SFP75	SFP70	SFP49	SFP47	UP_TMS	SFP48	SFP46	J
SFP108	SFP104	SFP100	SFP99	SFP96	SFP86	VDDI_10	SFP74	SFP69	SFP51	VSS_9	VDDI_6	SFP52	SFP50	K
SFP101	VSS_1	VDDI_1	SFP95	SFP88	SFP83	SFP79	SFP76	SFP68	SFP63	SFP62	SFP55	SFP54	SFP53	L
SFP98	SFP97	SFP94	VDDC_5	SFP90	SFP81	SFP78	SFP13	SFP12	VDDC_4	SFP64	SFP60	SFP57	SFP56	M
SFP93	SFP92	SCLK	VSS_15	SFP89	SFP85	SFP80	SFP77	VDDI_9	SFP67	SFP65	VDDI_7	SFP59	SFP58	N
SPCLK	SSCL	SSDA	SFP91	SFP87	SFP84	VSS_14	SFP73	SFP71	VDDI_8	VSS_11	SFP66	VSS_10	SFP61	P

5.2 STV0684 package mechanical data

Reference	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.210		1.700
A1	0.270		
A2		1.120	
b	0.450	0.500	0.550
D	11.850	12.000	12.150
D1		10.400	
E	11.850	12.000	12.150
E1		10.400	
e	0.720	0.800	0.880
f	0.650	0.800	0.950
ddd			0.120

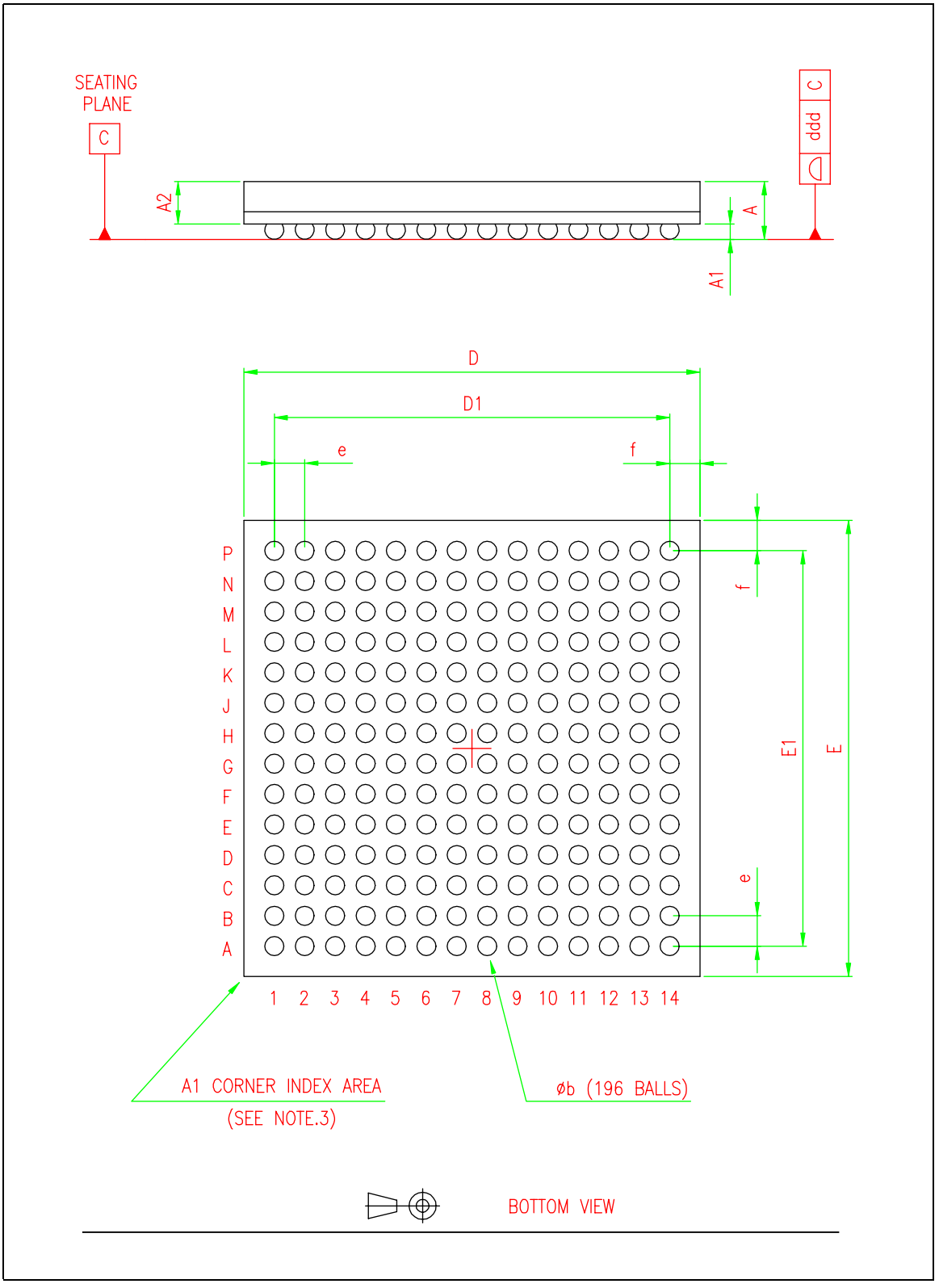
Note: 1 The maximum mounted height is 1.57 mm based on a 0.37 mm ball pad diameter. Solder paste is 0.15 mm thick with 0.37 mm ball pad diameter.

*2 LFBGA stands for **L**ow Profile **F**ine Pitch **B**all **G**rid **A**rray.*
Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component. A = [1.21 to 1.70] mm
FIne pitch: e<1.00 mm pitch.

3 The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings or other features of package body or integral heatslug.
A distinguishing feature can be added on the bottom surface of the package to identify the terminal A1 corner.

Exact shape of each corner is optional.

Figure 26: LFBGA 12x12x1.70 196 (80% scale versus original drawing)



Revision history

Table 22: Revision history

Version	Date	Comments
1	22-Mar-05	First publication for this revision 1.