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SSI 67F686
Automobile Bus Transceiver

December 1991

DESCRIPTION

The SSI 67F686 Automobile Bus Transceiver is an analog bus interface for a medium speed data communications network. It is designed specifically for a Class B J1850 10.4 kBit/s interface utilizing variable pulse width modulation bit encoding. However, many of the system parameters are user configurable, allowing for flexibility in a variety of applications requiring pulse shaping, signal filtering, or transient detection.

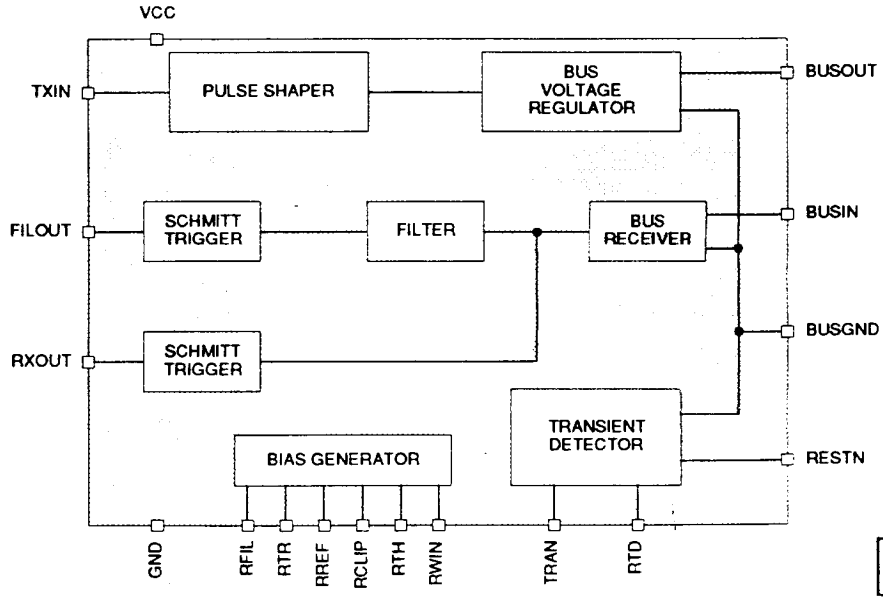
The SSI 67F686 allows a host system to transmit and receive data from a shared data bus. It communicates to the host system via a serial data line and is connected directly to a Class B bus, thus providing a complete link between host application and multiplexed data bus.

The SSI 67F686 provides a waveshaped 7.75V bus waveform in response to a timed logic signal from the host system. It also receives bus waveforms and provides the host system with either a filtered or unfiltered logic signal.

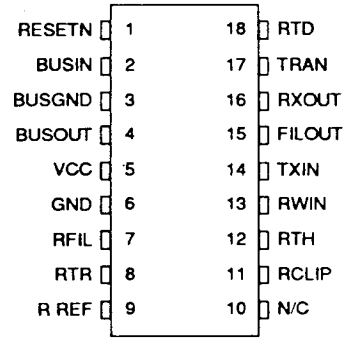
FEATURES

- **Single wire J1850 bus interface**
- **Compatible with VPWM bit encoding at 10.4 kBit/s**
- **CMOS compatible digital interface**
- **Waveshaping**
- **Analog filtering**
- **User configurable**
- **Detection of ground offset**
- **Isolation between local ground and bus ground**
- **ESD protection**
- **Operating temperature range: -40°C to +125 °C**
- **Available in an 18-pin DIP**

BLOCK DIAGRAM



PIN DIAGRAM



18-Pin PDIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

WAVESHAPING

A square wave input (TXIN) from the host system is conditioned for bus compatibility and to minimize EMI. A Pulse Shaper rounds off the edges of the square wave signal. An external resistor connected to RTR allows the system designer to control the rise and fall time of the waveshaped pulse. A Bus Voltage Regulator produces an output waveform (BUSOUT) that maintains a constant slew rate over variable resistive and capacitive loads. In order to achieve a 7.75V level necessary for the bus signal, the output current is regulated to sustain a constant bus voltage. This is preserved even during transient changes in bus impedance, temperature, or collisions where more than one message is transmitting on the bus simultaneously.

USER CONFIGURABLE

Many of the key system parameters are programmable by changing external resistor values. This is convenient for system designers wishing to optimize their designs. The following circuit parameters can be adjusted: waveshaped output rise and fall time, analog filter corner frequency, transient detect threshold, receive bus waveform window, Schmitt trigger threshold and hysteresis.

BUS RECEIVER

The Bus Receiver converts the ground reference of the bus signal from BUSGND to GND. The signal is then clipped at the top and bottom to improve noise immunity. An external resistor RCLIP allows the designer to adjust the window. The SSI 67F686 produces a filtered and an unfiltered output to the host system. The receive signal proceeds to a Schmitt trigger which squares the edges of the pulse and provides a CMOS level signal to an unfiltered output RXOUT. The receive signal also passes through a two pole Bessel low pass filter to remove high frequency interference. The filter's corner frequency can be adjusted with an external resistor at RFIL. It then proceeds to another Schmitt trigger where the edges are squared up and the filtered output is available at FILOUT. External resistors connected to RTH set the threshold and RWIN control the hysteresis of both Schmitt triggers.

TRANSIENT DETECTOR

The Class B bus is intended to work in a relatively noisy environment. Transients on the network bus can corrupt valid data. One source of low frequency noise is ground offset between the nodes. A Transient Detector circuit inside the SSI 67F686 detects the presence of ground offset in order to notify the host system of potentially corrupt data on the bus. The circuit monitors the voltage on the bus ground and compares it with the voltage on the logic ground. If a preset voltage threshold between bus ground and logic ground is exceeded, an output (TRAN) is latched high to indicate the occurrence of a transient. TRAN remains high until RESETN is set low. The threshold at which the Transient Detector latches is controlled by an external resistor connected to RTD. This adjustable voltage threshold ranges from 0V to 3V.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
BUSOUT	O	Bus output
BUSIN	I	Bus input
BUSGND	I	Bus ground return
RREF	I	External resistor to compensate for the temperature coefficient of the other external resistors
RWIN	I	External resistor to set Schmitt trigger window
RTH	I	External resistor to set Schmitt trigger threshold
GND	I	Logic ground
RCLIP	I	External resistor to set receive clipping levels
RTD	I	External resistor to set transient detector threshold
RFIL	I	External resistor to set filter corner frequency
RTR	I	External resistor to set transmitter rise and fall time
RESETN	I	Transient detector reset (active low)
TRAN	O	Transient detector output
RXOUT	O	Received data output
FILOUT	O	Filtered received data output
TXIN	I	Transmit data input
VCC	I	Power supply

ELECTRICAL SPECIFICATIONS

Unless otherwise specified 11 < VCC < 13V and -40°C < T(ambient) < +125 °C and external resistors are set to the nominal values. Currents flowing into the integrated circuit are positive. All voltages are referenced to logic ground unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	MIN	MAX	UNIT
Vcc (Relative to Bus Ground)		13	V
Storage Temperature	-55	+125	°C
Soldering Temperature (10 seconds)		260	°C
Bus Voltage (Relative to Logic Ground)	-4V	Vcc	V
Bus Voltage (Relative to Bus Ground)	-1.6	Vcc	V
BUSGND (Relative to Logic Ground)	-4	4	V
Other Inputs	-0.3	6	V

EXTERNAL RESISTOR EQUATIONS

PARAMETER	MIN VALUE	NOM VALUE	MAX VALUE	NOM RESISTOR
Transmit rise/fall time (10% to 90% of peak pulse voltage with respect to BUSGND) Rtr = Tr (2.17 kΩ/µs)	5 µs	12 µs	25 µs	28.8 kΩ
Transient detector threshold: Rtd = 30 kΩ + Vtd (6 kΩ/V)	0 V	2.0V	3V	44 kΩ
Receive clipping voltage: (clipping occurs Vclip above and below 3.875 V) Rclip = Vclip (9.09 kΩ/V)	.5V	2.2V	3V	20 kΩ
Filter critical frequency: (Filter delay = 1.2/2πFcr) Rfil = Fcr (1.18 kΩ/kHz)	5 kHz	23 kHz	120 kHz	35.7 kΩ
Schmitt trigger threshold: (at BUSIN) Rth = Vth (5.16 kΩ/V)	1.9V	3.875 V	5.8V	20 kΩ
Schmitt trigger window: (at BUSIN) Rwin = Vwin (3.8 kΩ/V)	0V	0.75 V	3V	2.4 kΩ
Reference Resistor: Rref = 22.5 kΩ				22.5 kΩ

OPERATING CONDITIONS

Unless otherwise specified, 11V <VCC<13, -40 °C< T(ambient) < +125 °C, Rbus = 240Ω, Cbus = 15 nF, external resistors are set to the nominal values. Current maximums are currents with the highest absolute value. All voltages are referenced to logic ground unless otherwise spcified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Vcc	With respect to BUSGND	11	12	13	V
Operating Temperature		-40	25	125	°C
Power consumption	Vout = 7.75 V with respect to BUSGND. GND = +2V with respect to BUSGND Vcc = 13V, Rbus = 240Ω		315	380	mW

POWER SUPPLY

Vcc Supply Current	BUSOUT = 7.75V with respect to BUSGND GND = +2V with respect to BUSGND. Vcc = 13V, Rbus = 240Ω		44	49	mA

FUNCTIONAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Logic inputs TXIN and RESETN						
High-level input current	Iih	Vi = 5V		125	150	µA
Low-level input current	Iil	Vi = 0V		-125	-150	µA
High-level input voltage	Vih		3.5			V
Low-level input voltage	Vil				1.5	V

PULSE SHAPING

Transmit Propagation Delay	Tp	V_{ih} or V_{il} of input pulse to 50% point of output. Output pulse is measured with respect to BUSGND	8.0	10	12.0	µs
Pulse Rise Time	Tr	10% to 90% of peak output voltage with respect to BUSGND	10.0	12	14.0	µs
Pulse Fall Time	Tf	90% to 10% of peak output voltage with respect to BUSGND. Cload<Tf/8Rload R_L = 240, C_L = 1nF	10.0	12	14.0	µs
Corner Rounding	T1	0% to 10% of peak output voltage with respect to BUSGND		4		µs
	T2	0% to 90% of peak output voltage with respect to BUSGND		16		µs

BUS OUTPUT

Pulse Amplitude Regulation	Vmax	Relative to bus ground	6.60	7.75	8.90	V
Current Limiter set point	Iout	BUSOUT = High Rbus = 100Ω	27	39	51	mA
BUSGND current	Iout	BUSOUT = High Rbus = 240Ω		300	400	µA

TRANSIENT DETECTOR

Trigger Voltage	Vtd	BUSGND relative to GND RTD = 42 kΩ	1.6	2.0	2.4	±V
RESETN Pulse Width	Trs		4			µs

BUS RECEIVER

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input low	V_{ilB}*	Relative to bus ground (RXOUT = V_{oh})	3.25	3.50	3.75	V
Input high	V_{ihB}*	Relative to bus ground (RXOUT = V_{ol})	3.95	4.25	4.55	V
Input current	Iin	Busin = 7.75V			2.0	µA
Receive Propogation Delay at RXOUT	Tu	V_{ihB} or V_{ilB} at BUSIN to 50% point of RXOUT	1.1	1.6	2.1	µs

* $V_{ilB} = V_{th} + \frac{1}{2}V_{win}$

* $V_{ihB} = V_{th} - \frac{1}{2}V_{win}$

RECEIVE FILTERING

Filter Type		Bessel, Second Order				
Transfer Function	TF	$\frac{3}{\frac{s^2}{(2\pi f_{cr})^2} + \frac{3s}{2\pi f_{cr}} + 3}$				
Corner Frequency	f_{cr}			23		kHz
Receiver Delay	Td	V_{ihB} or V_{ilB} BUSIN to 50% of FILOUT	8.0	10	12.0	µs

CMOS OUTPUTS (RXOUT AND TRAN)

High Level Output Voltage	Voh	Ioh = -280 µA	4.0			V
Low Level Output Voltage	Vol	Iol = 280 µA			1.0	V

APPLICATIONS INFORMATION

The SSI 67F686 is an automotive multiplex bus transceiver conforming to the SAE J1850 (10.4 kBit/s VPWM) standard. Figure 1 shows a typical application circuit. The SSI 67F686 is designed to be used with a microprocessor, or other logic device, which generates the appropriate messages for transmission, handles bus arbitration and processes the received information. The SSI 67F686 is the interface between the 5V logic level signals of the microprocessor and the 7.75V waveshaped signals on the bus. The BUSIN and BUSOUT signals are referenced to BUSGND, while the logic signals (TXIN, RXOUT, FILOUT, TRAN and RESETN) are referenced to GND.

The SSI 67F686 requires a single 12V supply, usually derived from the automobile battery. This voltage should be sufficiently regulated and filtered to keep it below the maximum VCC of 13V. It should be refer-

enced to GND and not BUSGND (if these are different). BUSGND is internally isolated from GND. This gives the designer the flexibility to ground BUSGND at some point external to the circuit board. This could reduce bus susceptibility to noise and also reduce the possibility of bus noise affecting the logic circuits.

The transient detector monitors the voltage difference between BUSGND and GND. When this difference exceeds the preset amount, the TRAN pin goes high and stays high until RESETN is driven low. This, in conjunction with externally grounding the BUSGND pin, can alert the microprocessor to the possibility of data corrupted by noise on the bus.

The configuration resistors shown in Figure 1 are nominal values and should be used for most applications. If other than nominal performance is desired, these resistor values can be changed and will affect the appropriate parameter according to the equation for that parameter. These resistors should all have a tolerance of 1% or better. RREF is an external reference resistor which is used to compensate for the temperature coefficients of the others. For this reason, they should be close together on the circuit board and should all be the same type.

ANALOG FILTER STARTUP

Due to the size of the time constants designed into the SSI 67F686 internal analog filter (on the FILOUT pin), the circuit is sensitive to power supply sequencing. Dropping the part into a "hot socket" or applying a signal at BUSIN prior to connecting Vcc may lock FILOUT into a low state. To eliminate this condition, tie a series combination of a 0.22 µF capacitor and 75 kΩ resistor between Vcc (pin 5) and RFIL (pin 7) as shown in Figure 1. RXOUT and the other outputs are not susceptible to this condition.

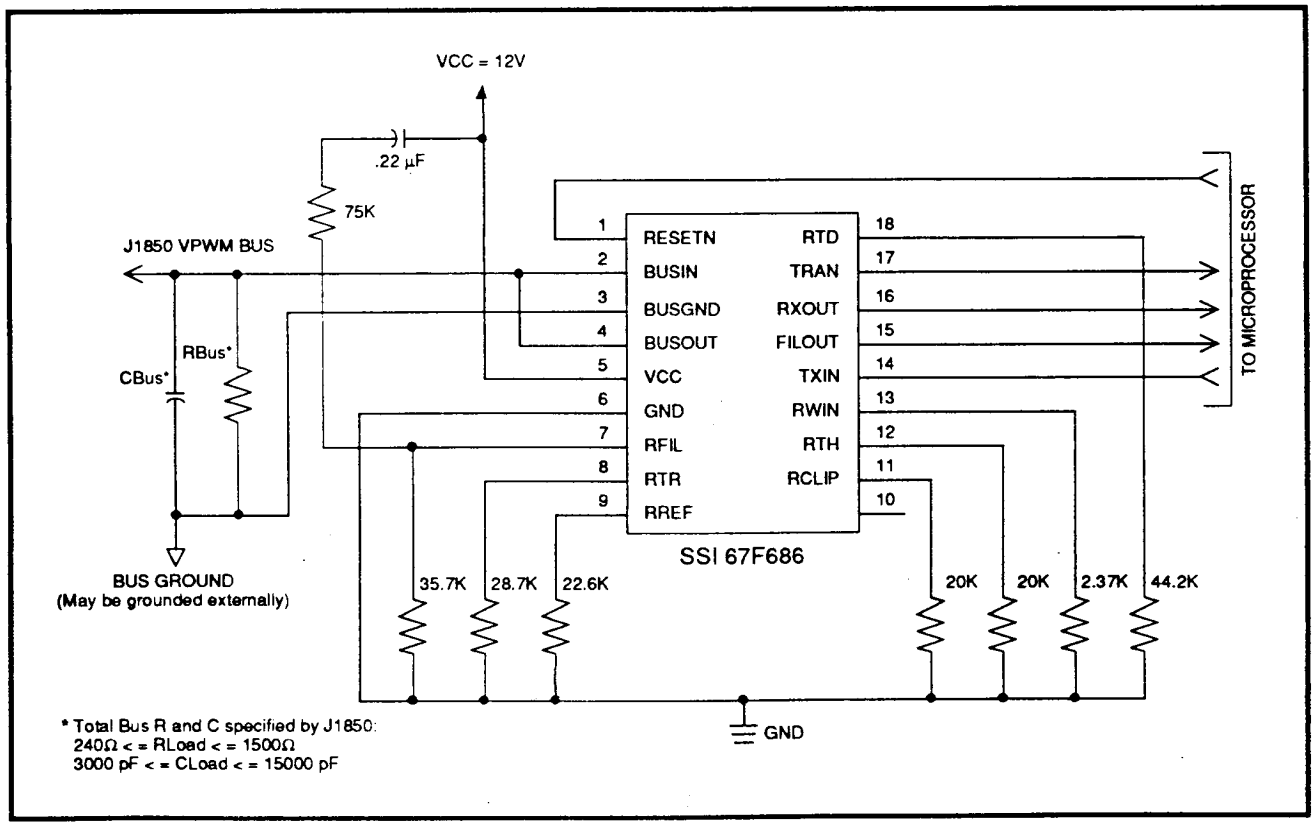


FIGURE 1: Typical Application Circuit

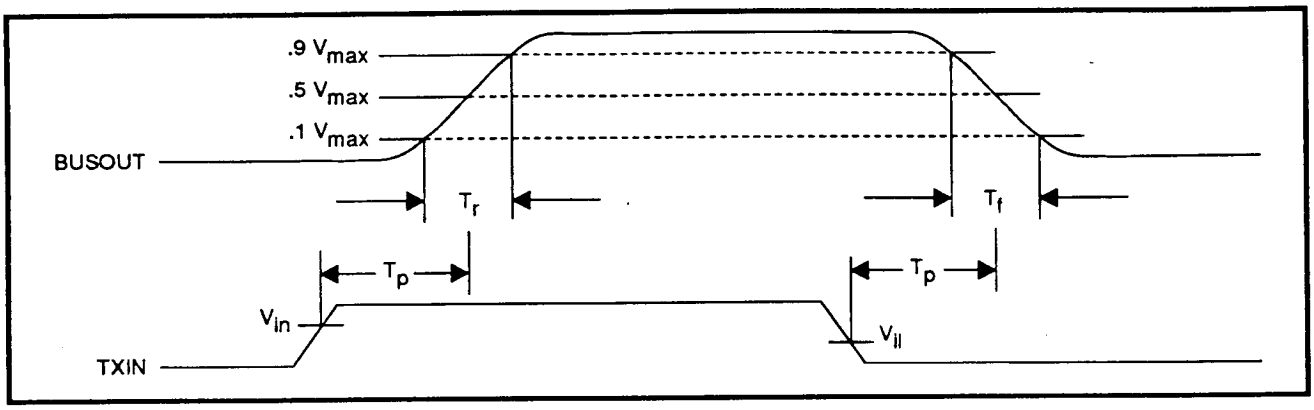


FIGURE 2: BUSOUT Timing

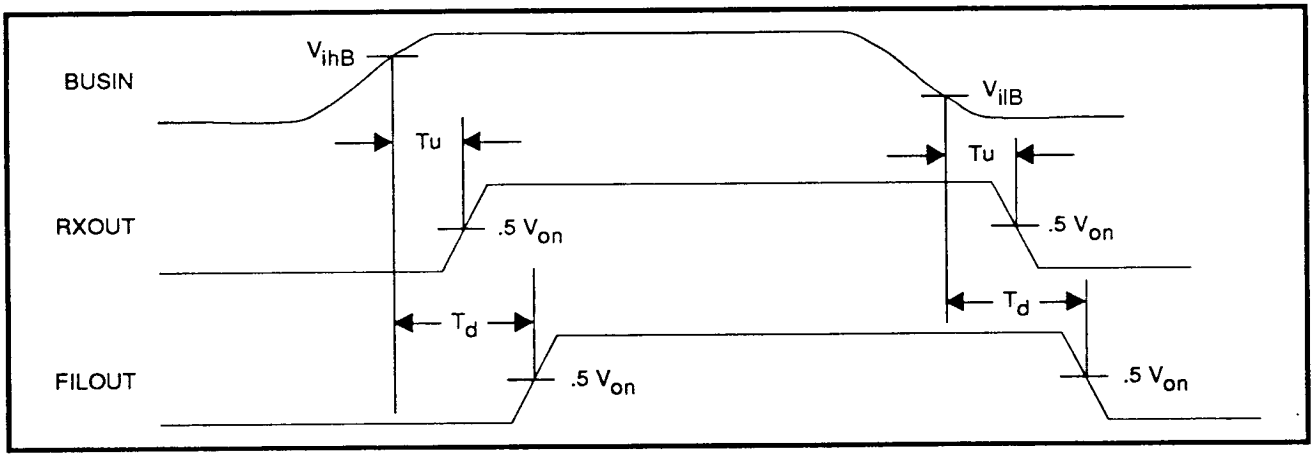


FIGURE 3: BUSIN Timing

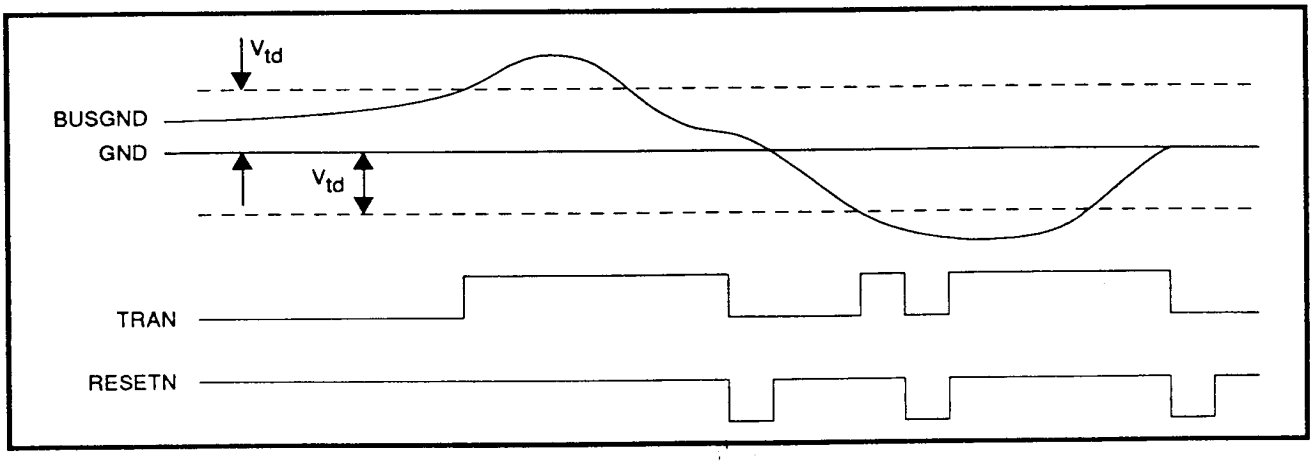
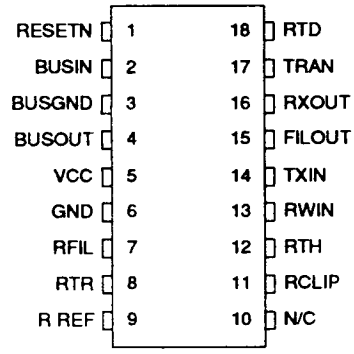


FIGURE 4: Transient Detector Operation

PACKAGE PIN DESIGNATION

(Top View)



18-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 67F686 18-pin Plastic Dual-In-Line	67F686-P	67F686-P

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