

Approval

TFT LCD Approval Specification

MODEL NO.: N141C3 - L01

Customer:	
Approved by:	
Note:	

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
0.0 2.0 2.1	Oct 11,'06 Mar. 12,'07 May. 09,'07 May. 15,'07	All All 14,15,16 30	AII AII 5.5 11	Tentative specification was first issued. Approval specification was first issued. Change EDID code (WWAN frequency change to 107.8 MHz) Outline drawing update (mylar location changed).



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1 GENERAL DESCRIPTION

1.1 OVERVIEW

N141C3 - L01 is a 14.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins

LVDS interface. This module supports 1440 x (3 RGB) x 900 WXGA+ mode and can display 262,144 colors.

The optimum viewing angle is at 6 o'clock direction. The inverter module for backlight is not built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA+ (1440 x 900 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- RoHS compliance

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	303.48(H) X 189.675(V) (14.1 inch Diagonal)	mm	(4)
Bezel Opening Area	306.76 (H) x 193.0 (V)	mm	(1)
Driver Element	a-si TFT active matrix	-	_
Pixel Number	1440 x R.G.B. x 900	pixel	
Pixel Pitch	0.21075 (H) x 0.21075 (V)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Colors	262,144	color	_
Transmissive Mode	Normally white	-	_
Surface Treatment	Anti-glare and Hard Coat, Haze 26, (3H min.)	-	

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Horizontal(H)	319	319.5	320	mm	7
Module SizeVertical(V)	205	205.5	206	mm	(1)
Depth(D)		5.2	5.5	mm	()
Weight		425	430	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

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2 ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

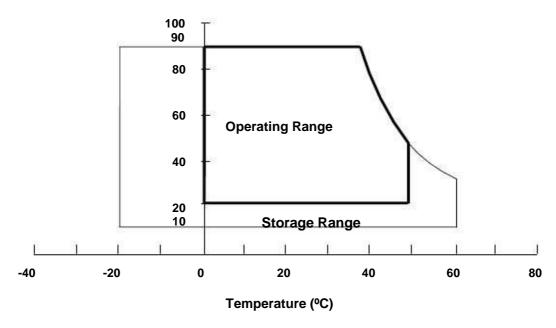
Itam	Cymphol	Va	Linit	Note	
Item	Symbol	Min.	Max.	Unit	Note
Storage TemperatureTsT		-20	+60	°C	(1)
Operating Ambient TemperatureTop		0	+50	°C	(1), (2)
Shock (Non-Operating)SNOP		-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)VNOP			1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta ≤ 40 °C).

- (b) Wet-bulb temperature should be 39 $^{\circ}$ C Max. (Ta > 40 $^{\circ}$ C).
- (c) No condensation.

Note (2) The temperature of panel display surface area should be 0 $^{\circ}$ C Min. and 60 $^{\circ}$ C Max..

Relative Humidity (%RH)

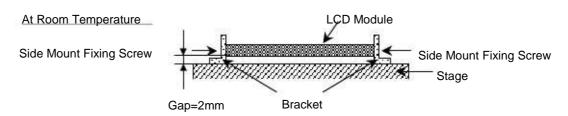


Note (3) 1 time for \pm X, \pm Y, \pm Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10 \sim 200 Hz, 30 min / Cycle, 1 cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:





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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

lán m	Cumphal	Value		I Imia	Note
Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	Vcc	-0.3	+4.0	V	(4)
Logic Input Voltage	Vin	-0.3	Vcc+0.3	V	(1)

2.2.2 BACKLIGHT UNIT

lt a ma	Company of	Val	ue	I Imia	Nista
Item	Symbol	Min.	Max.	Unit	Note
Lamp Voltage	VL	-	2.5K	VRMS	(1), (2)
Lamp Current	lL IL	2.0	6.5	mA _{RMS}	(4) (0)
Lamp Frequency	FL	45	80	KHz	(1), (2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).



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3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

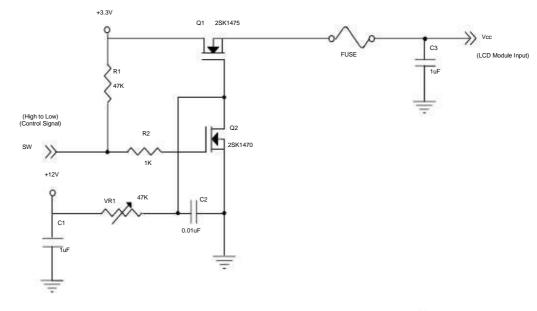
Davamatar	Curahal		Value	1.1	Nete	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Power Supply Voltage	Vcc	3.0	3.3	3.6	V	1
Permissive Ripple Voltage	VRP	i - ii	50	-	mV	-
Rush Current	Irush	-	-	1.5	А	(2)
Initial Stage Current White	lis		380	1.0	A	(2)
Power Supply Current Black	lcc	-	465	510	mA mA	(3)a (3)b (5),
LVDS Differential Input High Threshold	VTH(LVDS)	-	-	+100	mV	VcM=1.2\ (5)
LVDS Differential Input Low Threshold	VTL(LVDS)	-100	-	-	mV	Vcм=1.2\ (5)
LVDS Common Mode Voltage	Vсм	1.125	-	1.375	V	(5)
LVDS Differential Input Voltage	VID	100	-	600	mV	(4)
Terminating Resistor	R⊤		100		Ohm	(4)
Power per EBL WG	PEBL	-	3.69	-	W	

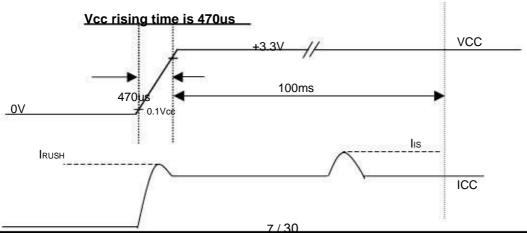
Note (1) The ambient temperature is $Ta = 25 \pm 2$ °C.

Note (2) IRUSH: the maximum current when VCC is rising

lis: the maximum current of the first 100ms after power-on

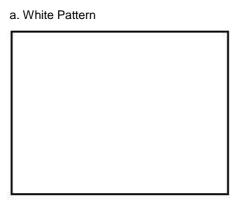
Measurement Conditions: Shown as the following figure. Test pattern: black.





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Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, $Ta = 25 \pm 2 \,^{\circ}\text{C}$, $f_v = 60 \,^{\circ}\text{Hz}$, whereas a power dissipation check pattern below is displayed.



b. Black Pattern

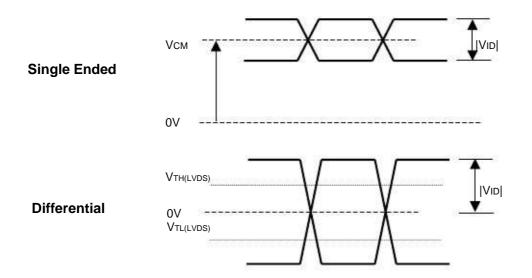


Active Area Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

- (a) Vcc = 3.3 V, $Ta = 25 \pm 2 \, {}^{\circ}\text{C}$, $f_{V} = 60 \, \text{Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.
- (d) The inverter used is provided from Sumida (www.sumida.com.tw). Please contact Sumida for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.



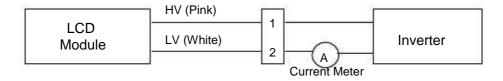
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3.2 BACKLIGHT UNIT

 $Ta = 25 \pm 2 \, {}^{\circ}C$

Davana atau	Cumphial		Value	Llais	NI-4-	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Lamp Input Voltage	VL	612	680	748	VRMS	IL = 6.0 mA
Lamp Current	l l	2.0	6.0	6.5	mA _{RMS}	(1)
		-	<u> </u>	1370 (25 °C)	VRMS	(2)
Lamp Turn On Voltage	Vs	-		1520 (0 _o C)	VRMS	(2)
Operating Frequency	FL	45 15.000	_	80	KHz Hrs	(3)
Lamp Life Time	LBL		4.08	_	W	(4), I _L = 6.0 mA
Power Consumption	PL		,			(4), 12 = 0.0 1117

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



- Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.
- Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.
- Note (4) $PL = IL \times VL$
- Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition $Ta = 25 \pm 2 \text{ } \circ \text{C} \text{ and } \text{IL} = 6 \text{ mArms until one of the following events occurs:}$
 - (a) When the brightness becomes or lower than 50% of its original value.
 - (b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)
- Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter



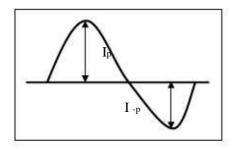


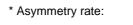
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which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- a. The asymmetry rate of the inverter waveform should be 10% below.
- b. The distortion rate of the waveform should be within $\sqrt{2 \pm 10\%}$.
- c. The ideal sine wave form shall be symmetric in positive and negative polarities.





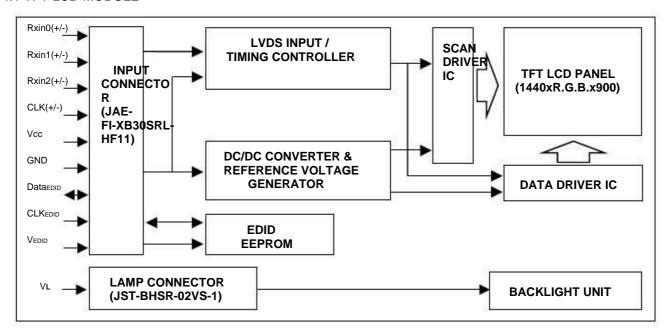
* Distortion rate



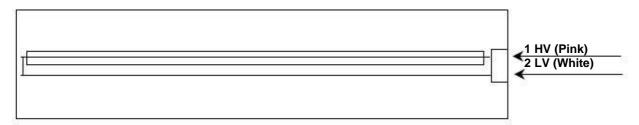
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4 BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



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5 INPUT TERMINAL PIN ASSIGNMENT

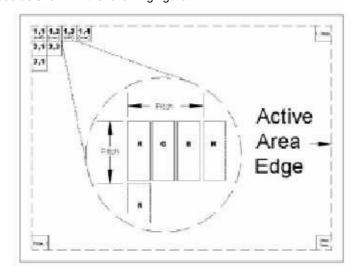
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	VEDID	DDC 3.3V Power		
5	NC NC	Non-Connection	- 100	
_6	CLKEDID	DDC Clock	19	
7	DATAEDID	DDC Data		
8	RXO0-	LVDS Differential Data Input (Odd)		-
9	RXO0+	LVDS Differential Data Input (Odd)	Negative	
10	Vss	Ground	Negative Positive	
11	RXO1-	LVDS Differential Data Input (Odd)	Positive	
12	RXO1+	LVDS Differential Data Input (Odd)		
13	Vss	Ground	Negative	
14	RXO2-	LVDS Differential Data Input (Odd)	Positive	
15	RXO2+	LVDS Differential Data Input (Odd)		
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RxE0-	LVDS Differential Data Input (Even)	Negative	
21	RxE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground	-	
23	RxE1-	LVDS Differential Data Input (Even)	-	
24	RxE1+	LVDS Differential Data Input (Even)	Negative	
25	Vss	Ground	Positive	
26	RxE2-	LVDS Differential Data Input (Even)		
27	RxE2+	LVDS Differential Data Input (Even)	Negative	
28	Vss	Ground	Positive	
29	RXEC-	LVDS Clock Data Input (Even)	1 OSILIVE	
30	RXEC+	LVDS Clock Data Input (Even)	-	
		EVBO Glock Bata Input (EVeri)	Negative	
			Positive	
			Negative	
			Positive	

Note (1) Connector Part No.: JAE-FI-XB30SRL-HF11 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

Note (3) The first pixel is odd as shown in the following figure.





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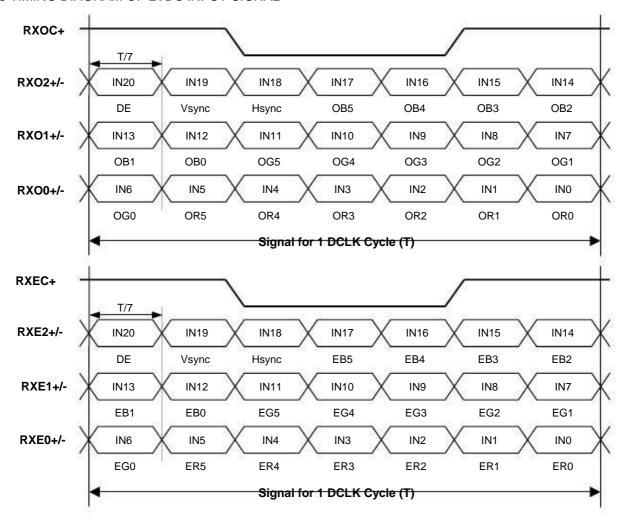
5.2 BACKLIGHT UNIT

ij	Pin	Symbol	Description	Color
	1	HV	High Voltage	Pink
ì	2	LV	Ground	White

Note (1) Connector Part No.: JST- BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL





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5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

				Г	ata S	Signal						1.00				
ColorRedGreenE	Blue															
R	5 R4 R3 R2	2 R1 I	R0 G	G4	G3 G	2 G1	G0 E	5 B4	B3 E	2 B1	B0	-				
Black0000000000		7			1	_	10		-			1	-			
Red11111100000	0000000															
Green000000111																
Basic Blue00000000000000	111111															
Colors Cyan00000011111	11111111															
Magenta1111110	000001111	11														
Yellow111111111	111000000)														
White1111111111	111111111															
Red(0)/Dark0000	000000000	0000	0													
Red(1)000001000	000000000)														
Gray Red(2)00001000000	00000000															
Scale::::::::::::::::::::::::::::::::::::																
Of:::::::																
RedRed(61)11110100000																
Red(62)11111000																
Red(63)11111100																
Green(0)/Dark 00			000													
Green(1)0000000																
Gray Green(2)000000000	010000000)														
Scale::::::::::::::::::::::::::::::::::::																
Of::::::::																
Green Green(61)0000001																
Green(62)000000																
Green(63)000000																
Blue(0)/Dark0000			0													
Blue(1)00000000		1														
Gray Blue(2)00000000000	00000010	_		_								15 13		_		15
Scale:::: Of::::::::																
Blue Blue(61)0000000000	00111101															
Blue(62)00000000		10														
Blue(63)0000000																
Piue(03)0000000		''														
73	E 4 1	y			1	17	P - 00	نــــا	00		D	19	 £2)	

Note (1) 0: Low Level Voltage, 1: High Level Voltage



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5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the

VESA Plug & Display and FPDI standards.

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	0000000
1	1	Header	FF	1111111
2	2	Header	FF	1111111
3	3	Header	FF	1111111
4	4	Header	FF	1111111
5	5	Header	FF	1111111
6	6	Header	FF -	1111111
7	7	Header	00	0000000
8	8	EISA ID manufacturer name ("CMO")	0D	0000110
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	1010111
10	OA	ID product code (N141C3-L01)	30	0011000
11	0B	ID product code (hex LSB first; N141C3-L01)	14	0001010
12	0C	ID S/N (fixed "0")	00	0000000
13	0D	ID S/N (fixed "0")	00	0000000
14	0E	ID S/N (fixed "0")	00	0000000
15	OF_	ID S/N (fixed "0")		0000000
16	10	Week of manufacture (fixed week code)	0B	0000101
17	11	Year of manufacture (fixed year code)	11	0001000
18	12	EDID structure version # ("1")	01	0000000
19	13	EDID revision # ("3")	- 03	0000001
20	14	Video I/P definition ("digital")	80	1000000
21	15	Active area horizontal 30.348cm	1E	0001111
22	16	Active area vertical 18.9675cm	13	0001001
23	17	Display Gamma (Gamma = "2.2")	78	0111100
24	18	Feature support ("Active off, RGB Color")	0A	0000101
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	09	0000100
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	05	0000010
27	1B	Rx=0.590	97	1001011
28	1C	Ry=0.340	57	0101011
29	1D	Gx=0.319	51	0101000
30	1E	Gy=0.541	8A	1000101
31	1F	Bx=0.152	27	0010011
32	20	By=0.125	<u>20</u>	0010000
33	21	Wx=0.313	50	0101000
34	22	Wy=0.329	54	0101010
35	23	Established timings 1	00	0000000
36	24	Established timings 2		0000000
37	25	Manufacturer's reserved timings	00	0000000
38	26	Standard timing ID # 1	01	0000000
39	27	Standard timing ID # 1	01	0000000
40	28	Standard timing ID # 2	01	0000000
41	29	Standard timing ID # 2	01	0000000
42	2A	Standard timing ID # 2 Standard timing ID # 3	01	0000000
43	2B	Standard timing ID # 3	01	0000000



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44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	0000000
48	30	Standard timing ID # 6	01	0000000
49	31	Standard timing ID # 6	01	0000000
50	32	Standard timing ID # 7	01	0000000
51	33	Standard timing ID # 7	01	0000000
52	34	Standard timing ID # 8	01	0000000
53	35	Standard timing ID # 8	01	0000000
55	- 55	Detailed timing ib # 0 Detailed timing description # 1 Pixel clock ("107.8MHz",	- 01	0000000
		According to VESA CVT Rev1.1)		
		# 1 Pixel clock (hex LSB first)		
		# 1 H active ("1440")		
		# 1 H blank ("418")	1C	00011100
<u>54</u>	36	# 1 H active : H blank ("1440 : 418")		
55	37	#1 V active ("900")	2A	00101010
56	38	# 1 V blank ("67")	A0	10100000
57	39	# 1 V active : V blank ("900 :67")	A2	10100010
58	3A_		51	01010001
59	3B	# 1 H sync offset ("126")	84	10000100
60	3C	# 1 H sync pulse width ("84") # 1 V sync offset : V sync pulse width (" 8 : 15")	43	01000011
61	3D	# 1 V sync offset : V sync pulse width (" 8 : 15")	30	00110000
62	3E	# 1 H sync offset : H sync pulse width : V sync offset : V sync	7E	01111110
63	3F	width ("126: 84 : 8 : 15")	54	01010100
64	40	# 1 H image size ("303 mm")	8F	10001111
-		# 1 V image size ("190 mm")		
		# 1 H image size : V image size ("303 : 190")	_	
		# 1 H boarder ("0")		
		# 1 V boarder ("0")	1	
05		# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol	00	00000000
65	41 42	Negatives		-
66		Detailed timing description # 2	2F	00101111
67	43	# 2 Flag	BE	10111110
68	44	# 2 Reserved	10	00010000
69	45	# 2 FE (hex) defines ASCII string (Model Name "N141C3-L01",		00000000
70	46	ASCII)	00	00000000
		# 2 Flag		
		# 2 1st character of name ("N")		
		# 2 2nd character of name ("1")	18	00011000
71	47	# 2 3rd character of name ("4")	_	
72	48	# 2 4th character of name ("1")	00	00000000
73	49	# 2 5th character of name ("C")	00	00000000
74	4A	# 2 6th character of name ("3")	00	00000000
		# 2 7th character of name ("-")	_	
		# 2 8th character of name ("L")		1111111
75	4B	# 2 9th character of name ("0")	FE	1111111
76	4C	# 2 9th character of name ("1")	00	0000000
77 77	4D	# 2 New line character indicates end of ASCII string	00	00000000
78	4E	# 2 Padding with "Blank" character	4E	01001110
79	4F	# 2 Padding with "Blank" character	31	00110001
80	50		34	00110100
81	51		31	00110001
82	52	Si di	43	01000011
83	53		33	00110011
ია 84	54		2D	00101101
85	55		4C	01001100
		2	30	00110000
86 87	56 57		31	00110001
			OA	00001010
88 89	58 59		20	00100000
oa	59		20	00100000



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90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMO", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string ("C")	43	01000011
96	60	# 3 2nd character of string ("M")	4D	01001101
97	61	# 3 3rd character of string ("O")	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved		00000000
13		# 4 FE (hex) defines ASCII string (Model Name"N141C3-L01",		
		ASCII)		
- 1		# 4 Flag		
-	-	# 4 1st character of name ("N")	-	-
		# 4 2nd character of name ("1")		
		# 4 3rd character of name ("4")		
		# 4 4th character of name ("1")		
		# 4 5th character of name ("C")	FE	1111111
111	6F	# 4 6th character of name ("3")		
112	70	# 4 7th character of name ("-")	00	00000000
113	71	# 4 8th character of name ("L")	4E	01001110
114	72	# 4 9th character of name ("0")	31	00110001
115	73	# 4 9th character of name ("1")	34	00110100
116	74	# 4 New line character indicates end of ASCII string	31	00110001
117	75	# 4 Padding with "Blank" character	43	01000011
118	76	# 4 Padding with "Blank" character	33	00110011
119	77	Extension flag	2D	00101101
120	78	Checksum	4C	01001100
121	79	Onconoun	30	00110000
122	7A		31	00110001
123	7B		0A	00001010
124	7C		20	00100000
125	7D	(f)	20	00100000
126	7E	0 01	00	0000000
127	7F		9C	10011100
			- 30	10011100

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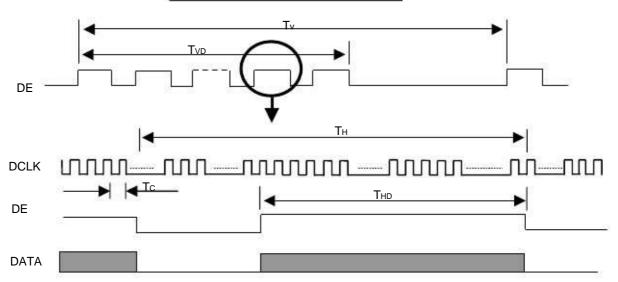
6 INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

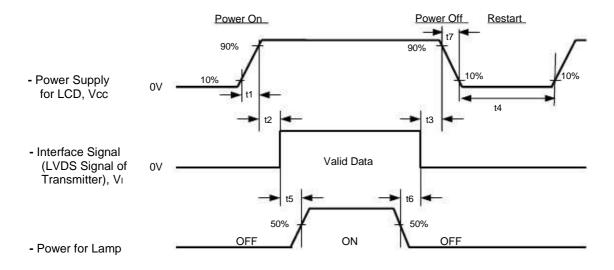
The specifications of input signal timing are as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	25	44.5	60	MHz	(2)
	Vertical Total Time	TV	910	926	1500	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	-
DE	Horizontal Total Time	TH	760	800	880	Tc	_
	Horizontal Active Display Period	THD	720	720	720	Tc	(2)
	Horizontal Active Blanking Period	THB		80		Tc	(2)
	· ·		TH-THD		TH-THD		(2)

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE





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Timing Specifications:

0.5< t1 ≤ 10 msec

0 < t2 ≤ 50 msec

0 < t3 ≦ 50 msec

t4 ≥ 500 msec

t5 ≧ 200 msec

t6 ≥ 200 msec

- Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.
- Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.
- Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.
- Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 5 □ t7 □ 300 ms.



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7 OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	SymbolValueUnit		
Ambient Temperature	T-025.2		0
Ambient Humidity Supply Voltage	TaC25±2 Ha%RH50±10		
Input Signal	Vcc3.3V		
Inverter Current	According to typical value	e in "3. ELECTRICAL CHAF	RACTERISTICS"
Inverter Driving Frequency	IL6.0mA		9
Inverter	FL61KHz	Sumida H05-4915	

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

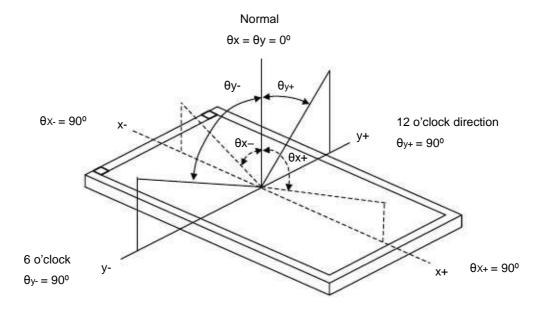
7.2 OPTICAL SPECIFICATIONS

lter	n		mbol	Condition	Min.	Тур.	Max.	Unit	Note		
Contrast Ratio Response Time Average Luminance of White White Variation			CR Tr F VE		250 - - - 185	400 5 11 220	10 16 -	ms ms cd/m ₂	(2), (6) (3) (4), (6)		
			5pts		-	- 1.4	1.4	-	(6)		
	Red		Rx Ry	θx=0°, θy =0° Viewing Normal Angle	ring Normal 0.590 Angle 0.340		-				
Color	Green	-	Gx Gy Bx	Gy	Gy		TYP	0.319 0.541 0.152	TYP		
Chromaticity	Blue	1	By Wx Wy	0.31	-0.03	0.125 0.313 0.329	+0.03	-	(4) (6)		
	White		vvy			45 45			(1), (6)		
Minusina Anada	Horizontal	-	9x+ 9x- 9y+	CD>40	40 40	20 45	eng, ange	Dan			
Viewing Angle	Vertical		9 _Y -	CR≥10	40	40		Deg.			



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Note (1) Definition of Viewing Angle (θx , θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

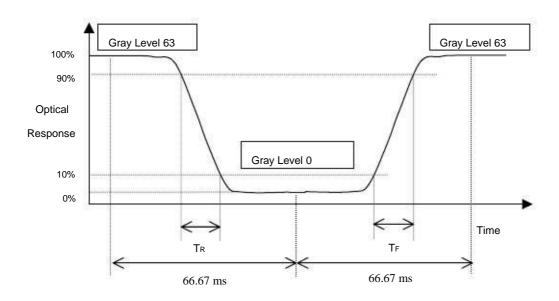
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

Note (3) Definition of Response Time (TR, TF):





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Note (4) Definition of Average Luminance of White (LAVE):

Measure the luminance of gray level 63 at 5 points

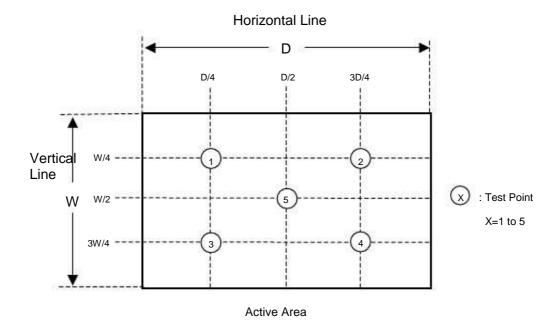
$$LAVE = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

L (x) is corresponding to the luminance of the point X at Figure in Note (5)

Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

 $\delta W = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]$

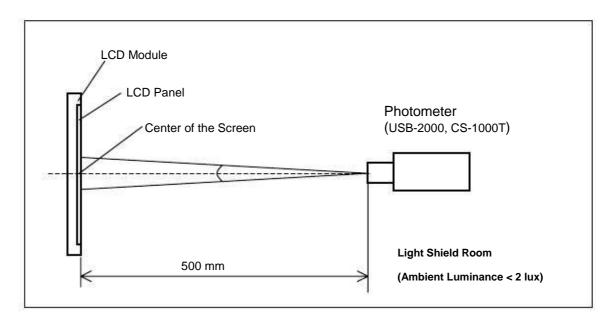




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Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



CHIMEI OPTOELECTRONICS CORP.

Issued Date: May 15, 2007 Model No.: N141C3 - L01

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8 PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 SAFETY PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

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9 PACKAGING9.1 CARTON

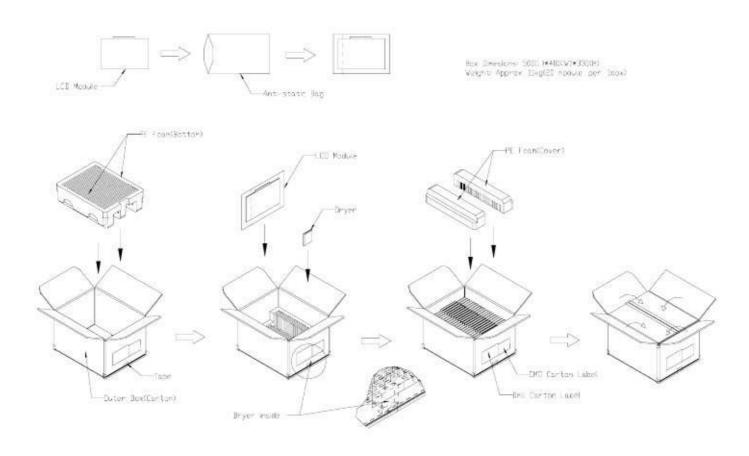


Figure. 9-1 Packing method

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9.2 PALLET FOR SEA FREIGHT

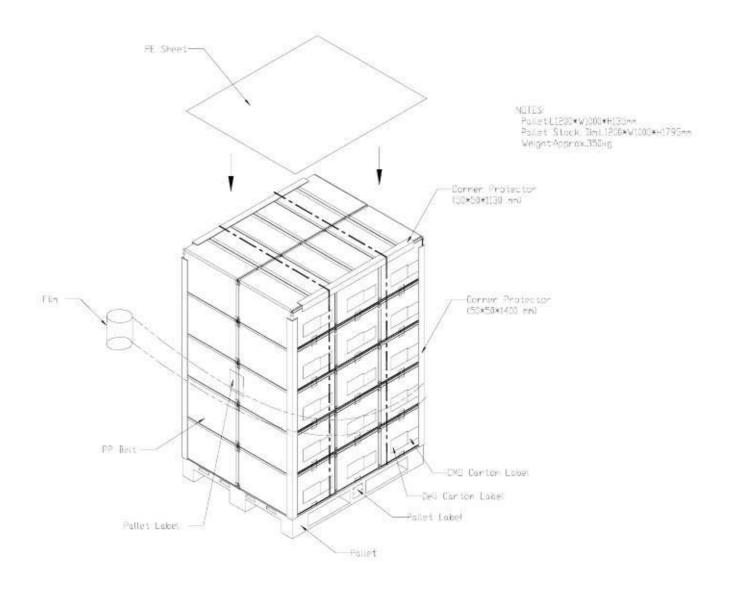


Figure. 9-2 Packing method

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9.3 PALLET FOR AIR FREIGHT

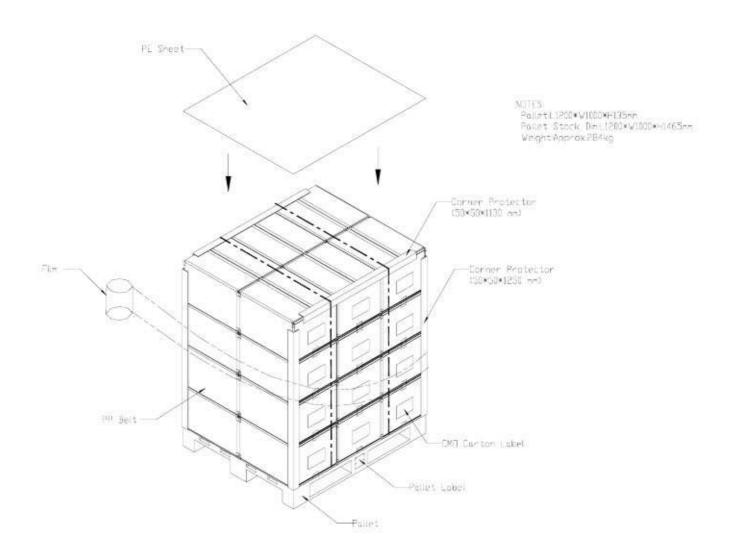


Figure. 9-3 Packing method

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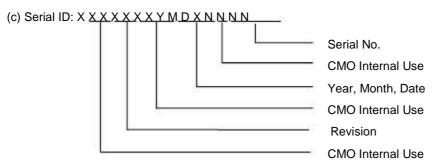
10 DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N141C3 L01
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.



- (d) Production Location: MADE IN XXXX. XXXX stands for production location.
- (e) LEOO: UL compliance remarks for CMO NingBo site production. It won't be available when production location isn't CMO NingBo.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U

- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product





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10.2 CMO CARTON LABEL



(a) Production location: Made In XXXX. XXXX stands for production location.

