

# 4V Drive Nch + Nch MOSFET

# **MP6K13**

#### Structure

Silicon N-channel MOSFET

#### Features

- 1) Low on-resistance.
- 2) High power package(MPT6).
- 3) Low voltage drive(4V drive).

# 

● Dimensions (Unit : mm)

# Application

Switching

Packaging specifications

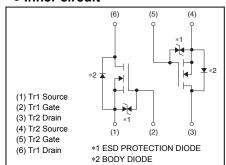
Туре	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	1000
MP6K13		0

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		$V_{DSS}$	30	V
Gate-source voltage		$V_{GSS}$	±20	V
Drain current	Continuous	I <sub>D</sub>	±6.0	Α
	Pulsed	I <sub>DP</sub> *1	±12	Α
Source current (Body Diode)	Continuous	l <sub>s</sub>	1.6	Α
	Pulsed	I <sub>sp</sub> *1	12	Α
Power dissipation		P <sub>D</sub> *2	2.0	W / TOTAL
		' D	1.4	W / ELEMENT
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	-55 to +150	°C

<sup>\*1</sup> Pw≤10µs, Duty cycle≤1%

## • Inner circuit



<sup>\*2</sup> Mounted on a ceramic board.

# ● Electrical characteristics (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gatesource leakage	I <sub>GSS</sub>	-	_	±10	μA	$V_{GS}$ =±20V, $V_{DS}$ =0V
Drainsource breakdown voltage	V <sub>(BR)DSS</sub>	30	-	_	٧	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS (th)</sub>	1.0	-	2.5	٧	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA
Otatia duain accura accetata	*	-	22	31	mΩ	I <sub>D</sub> =6.0A, V <sub>GS</sub> =10V
Static drainsource onstate resistance	R <sub>DS (on)</sub>	-	30	42		I <sub>D</sub> =6.0A, V <sub>GS</sub> =4.5V
		-	35	49		I <sub>D</sub> =6.0A, V <sub>GS</sub> =4.0V
Forward transfer admittance	I Y <sub>fs</sub> I*	3.5	-	_	S	I <sub>D</sub> =6.0A, V <sub>DS</sub> =10V
Input capacitance	C <sub>iss</sub>	-	350	_	pF	V <sub>DS</sub> =10V
Output capacitance	C <sub>oss</sub>	-	160	_	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	-	65	_	pF	f=1MHz
Turnon delay time	t <sub>d(on)</sub> *	-	8	_	ns	I <sub>D</sub> =3.0A, V <sub>DD</sub> ≒15V
Rise time	t <sub>r</sub> *	-	16	_	ns	V <sub>GS</sub> =10V
Turnoff delay time	t <sub>d(off)</sub> *	-	30	_	ns	$R_L$ =5.0 $\Omega$
Fall time	t <sub>f</sub> *	-	7	_	ns	$R_G$ =10 $\Omega$
Total gate charge	Q <sub>g</sub> *	_	5.0		nC	I <sub>D</sub> =6.0A, V <sub>DD</sub> ≒15V
Gatesource charge	Q <sub>gs</sub> *		1.4		nC	V <sub>GS</sub> =5V
Gatedrain charge	Q <sub>gd</sub> *	_	1.9	_	nC	

<sup>\*</sup>Pulsed

# ●Body diode characteristics (Source-Drain) (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward Voltage	V <sub>SD</sub> *	_	_	1.2	V	Is=6.0A, V <sub>GS</sub> =0V

<sup>\*</sup>Pulsed

## ●Electrical characteristic curves (Ta=25°C)

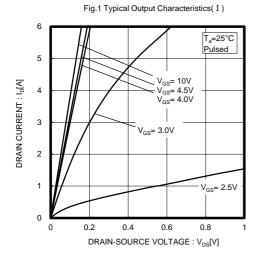


Fig.3 Typical Transfer Characteristics

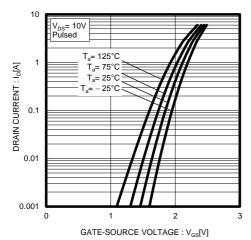


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current( II )

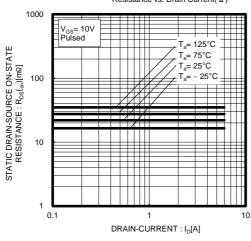


Fig.2 Typical Output Characteristics( II )

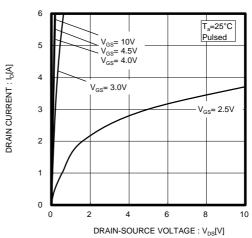


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current( I )

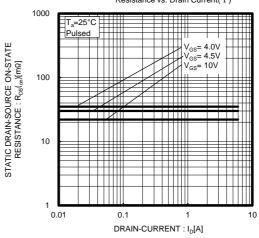
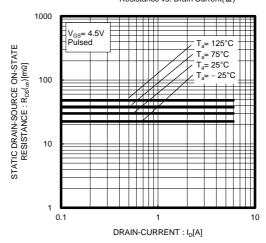
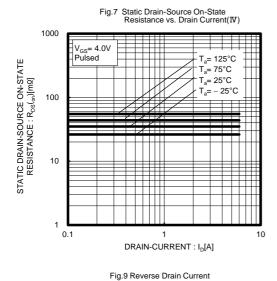


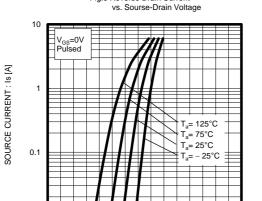
Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)



0.01

0

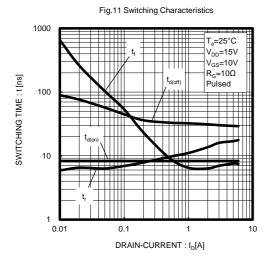


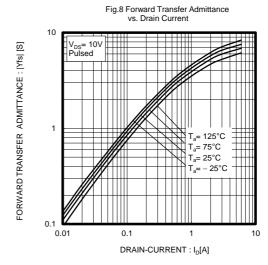


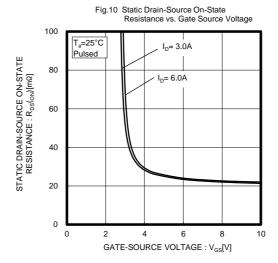
0.5

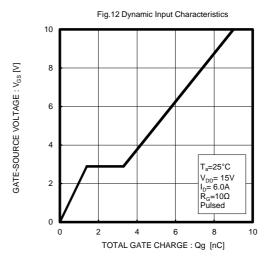
SOURCE-DRAIN VOLTAGE :  $V_{SD}$  [V]

1.5









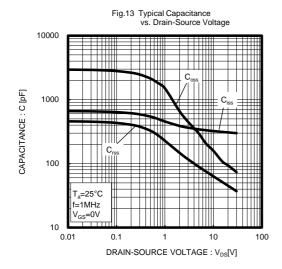


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width

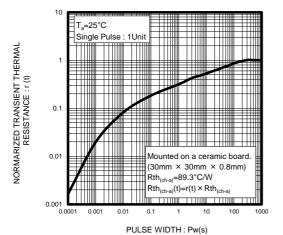


Fig.14 Maximum Safe Operating Aera 100 Operation in this area is limited by R<sub>DS(ON)</sub> (V<sub>GS</sub>=10V) 10 DRAIN CURRENT : I<sub>D</sub> (A) P<sub>w</sub>=1ms -----P<sub>W</sub> = 10ms 0.1 T<sub>a</sub>=25°C Single Pulse : 1Unit
Mounted on a ceramic board.
(30mm × 30mm × 0.8mm) DC operation 0.01 10 0.1 100

DRAIN-SOURCE VOLTAGE :  $V_{DS}[V]$ 

# Measurement circuits

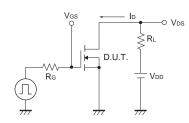


Fig.1-1 Switching Time Measurement Circuit

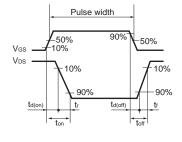


Fig.1-2 Switching Waveforms

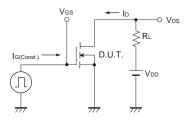


Fig.2-1 Gate Charge Measurement Circuit

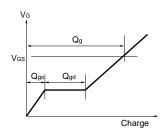


Fig.2-2 Gate Charge Waveform

#### Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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