# M54929P

## PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

## DESCRIPTION

The M54929P is an IIL semiconductor integrated circuit consisting of a PLL frequency synthesizer, suitable for use in a amateur radio equipment.

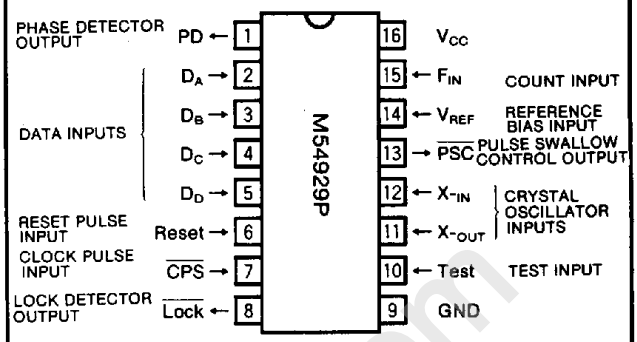
## FEATURES

- Capable of synthesizing frequencies up to 300MHz when used with the M54466L 1/10, 1/11 2 -modulus prescaler
- Programmable divider can operate at frequencies up to 30MHz
- Division ratios from 200 to 3999 can be set using a swallow counter (set from 0 ~ 9 by 4 bits of BCD code) and program divider (set from 20 ~ 3999 by 14 bits of BCD code).
- Four reference frequency division ratios (1/20, 1/100, 1/1000, and 1/1024)
- PLL lock/unlock status display outputs
- Two-stage data latch

## APPLICATION

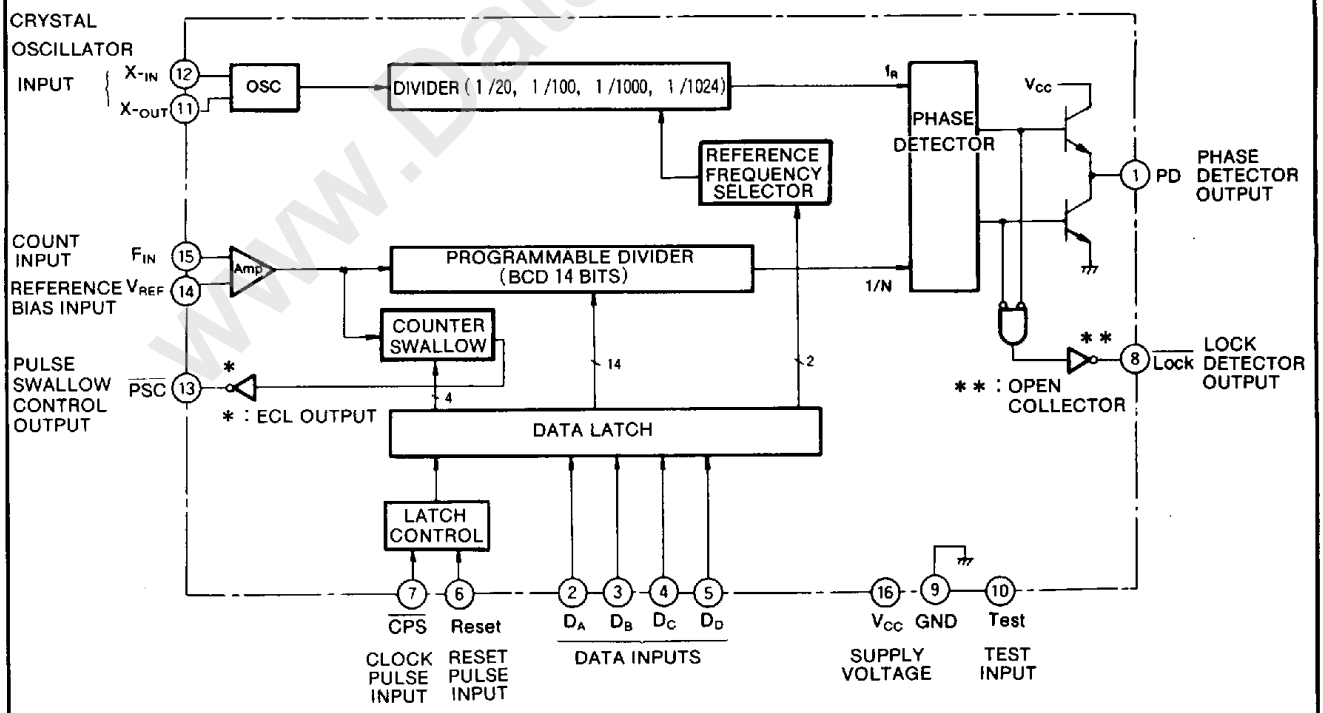
Amateur radio equipment

## PIN CONFIGURATION (TOP VIEW)




Outline 16P4

## BLOCK DIAGRAM





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# M54929P

## PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

## PIN DESCRIPTION

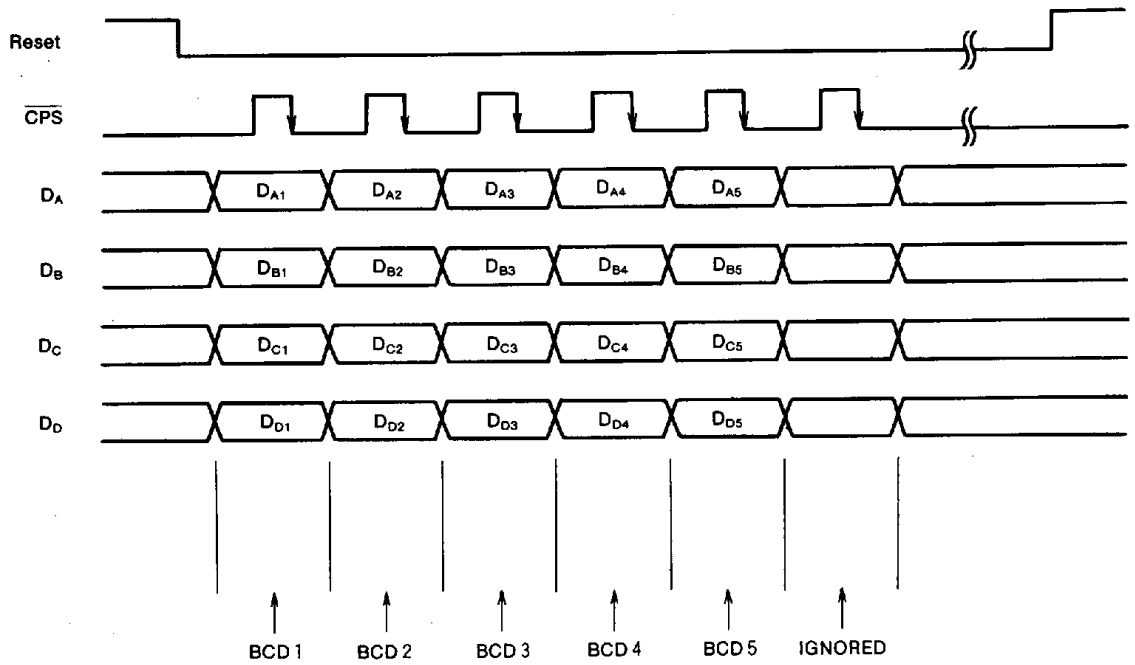
| No. | Symbol | Pin name | Description |
|---|---|---|---|
| 1 | PD | Phase detector output | Three-state High=phase advance, low=phase delay, high impedance=sync |
| 2 | $D_A$ | Data input | Input pin to set division ratio of programmable divider. Data is set with BCD code |
| 3 | $D_B$ | | |
| 4 | $D_C$ | | |
| 5 | $D_D$ | | |
| 6 | Reset | Reset pulse input | Data latch reset input |
| 7 | $\overline{CPS}$ | Clock pulse input | Data read clock input |
| 8 | $\overline{Lock}$ | Lock detector output | Low when PD is high-impedance, high when PD is low or high. Open collector. |
| 9 | GND | GND | 0 V |
| 10 | Test | Test input | Normally set low. When set high, program divider output $F_{IN}/N$ is output at pin 1 (PD), and reference frequency $f_R$ is output at pin 8 ($\overline{Lock}$). |
| 11 | $X\text{-}_{OUT}$ | Crystal oscilltor input | A 10MHz crystal oscillator is used. |
| 12 | $X\text{-}_{IN}$ | | |
| 13 | $\overline{PSC}$ | Pulse swallow control output | Controls division ratio of 1/10, 1/11 2-modulus prescaler (M54466L). ECL level output |
| 14 | $V_{REF}$ | Reference bias | Grounded through a 10000pF capacitor. |
| 15 | $F_{IN}$ | Count input | Count frequency input pin. $f_{max}$=30MHz |
| 16 | $V_{CC}$ | Power supply | 5 V±0.25V |

## PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

## FUNCTION

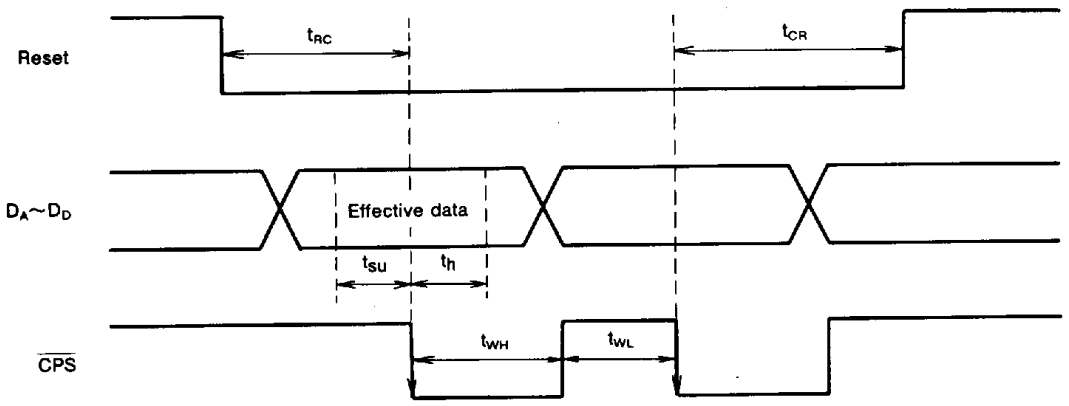
1. DATA INPUT

Configuration of input signals




Note 1 : After the Reset input is set low, five pulses applied at $\overline{CPS}$ (negative-edge trigger) read five sets of 4-bit BCD data.
2 : General parameters (N value, reference frequency) are set at the falling edge of the 5 th $\overline{CPS}$ pulse. Successive data inputs at $\overline{CPS}$ are ignored.
3 : When the reset input is high, signals applied at $\overline{CPS}$, $D_A$ and $D_D$ have no effect.

Timing of input signals

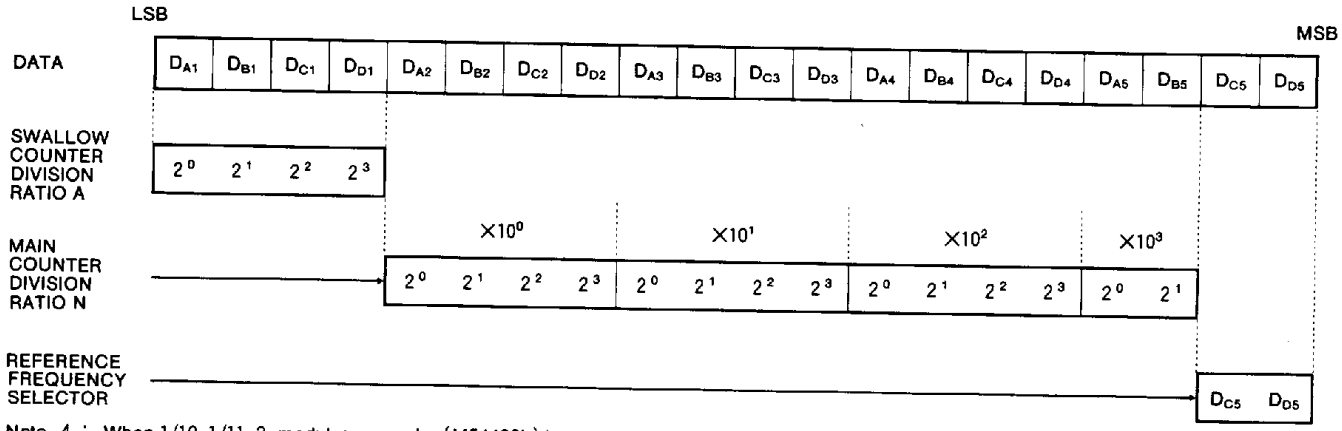



Minimum value $t_{SU}=t_h=t_{WH}=t_{WL}=10\mu S$

$t_{RC}=t_{CR}=20\mu S$

## PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

### 2. CONFIGURATION OF DATA BITS




Note 4 : When 1/10, 1/11 2-modulus prescaler (M54466L) is connected, the overall division ratio M is given by M=A+10N.
5 : When a prescaler is not used, the division ratio is determined by N and the data in the swallow counter is not used.
6 : The reference frequency is selected using the values in the table below.

### Reference frequencies

| BCD 5 | | Division ratio | Reference frequency | Crystal type |
|---|---|---|---|---|
| $D_{C5}$ | $D_{D5}$ | | | |
| L | L | 1024 | 10kHz | 10.24MHz |
| H | L | 1000 | 10kHz | 10MHz |
| L | H | 100 | 100kHz | 10MHz |
| H | H | 20 | 500kHz | 10MHz |

### 3. Example of data coding

(1) The following BCD codes set a reference frequency of 10kHz and a division ratio of 26789 when used with a 1/10, 1/11 2-modulus prescaler.

| $D_{A1}$ | $D_{B1}$ | $D_{C1}$ | $D_{D1}$ | $D_{A2}$ | $D_{B2}$ | $D_{C2}$ | $D_{D2}$ | $D_{A3}$ | $D_{B3}$ | $D_{C3}$ | $D_{D3}$ | $D_{A4}$ | $D_{B4}$ | $D_{C4}$ | $D_{D4}$ | $D_{A5}$ | $D_{B5}$ | $D_{C5}$ | $D_{D5}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | L | L | H | L | L | L | H | H | H | H | L | L | H | H | L | L | H | H | L |
| 9 | | | | 8 | | | | 7 | | | | 6 | | | | 2 | | 10kHz reference frequency | |

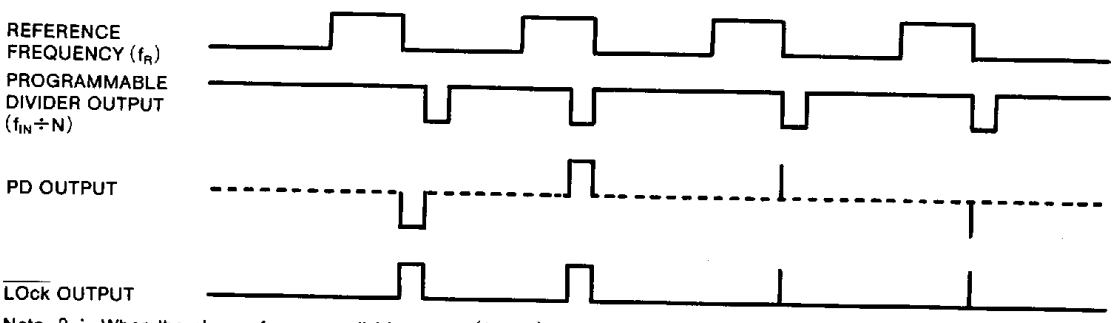
Note 7 : The PLL locks, when $f_{IN}$=26789×10kHz=267.89MHz.

(2) To set a reference frequency of 100kHz and a division ratio of 254, when a prescaler is not used.

| $D_{A1}$ | $D_{B1}$ | $D_{C1}$ | $D_{D1}$ | $D_{A2}$ | $D_{B2}$ | $D_{C2}$ | $D_{D2}$ | $D_{A3}$ | $D_{B3}$ | $D_{C3}$ | $D_{D3}$ | $D_{A4}$ | $D_{B4}$ | $D_{C4}$ | $D_{D4}$ | $D_{A5}$ | $D_{B5}$ | $D_{C5}$ | $D_{D5}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | L | L | H | L | H | L | H | L | L | H | L | L | L | L | L | H |
| X=irrelevant (either high or low) | | | | 4 | | | | 5 | | | | 2 | | | | 0 | | 100kHz reference frequency | |

Note 8 : The PLL locks, when $f_{IN}$=254×100kHz=25.4MHz.

### 4. PD, $\overline{\text{Lock}}$

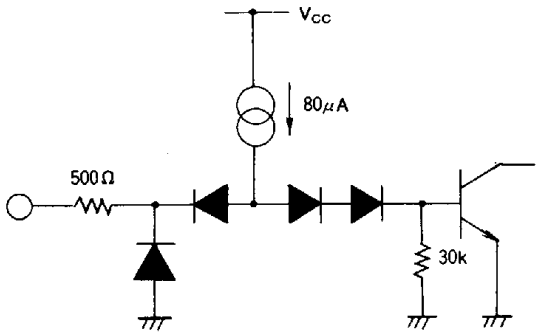



Note 9 : When the phase of program divider output ($f_{IN}$÷N) is delayed with respect to the reference frequency ($f_R$), PD goes low; when the phase of $f_{IN}$÷N is advanced, PD goes high.
10 : Broken lines indicate the high-impedance state.

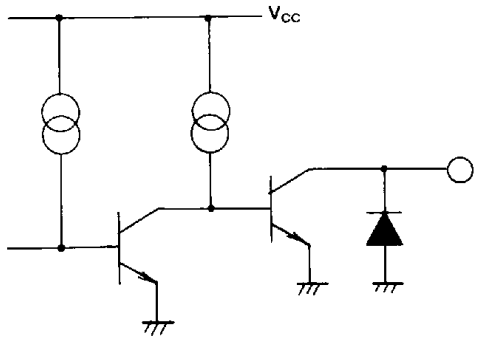
## PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

### I/O CIRCUIT DIAGRAM

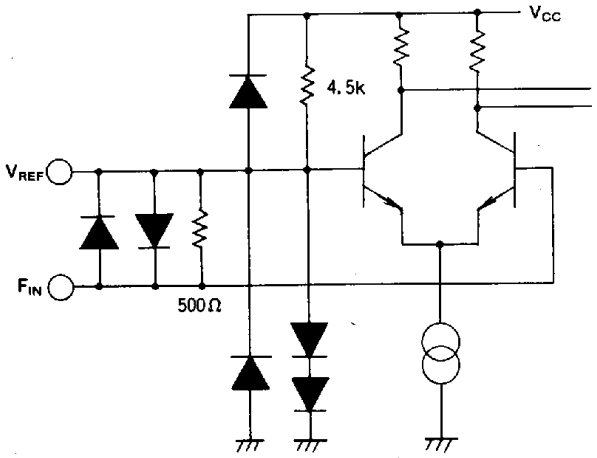
1 $D_A$ through $D_D$, Reset, $\overline{CPS}$, Test inputs



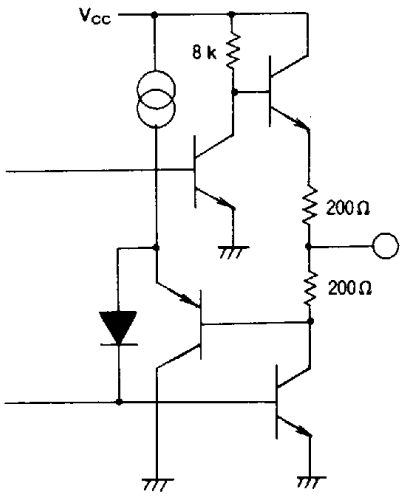

2 $\overline{Lock}$ output



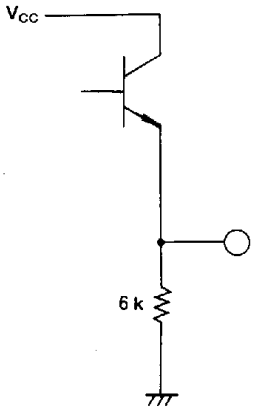

3 $F_{IN}$, $V_{REF}$ inputs



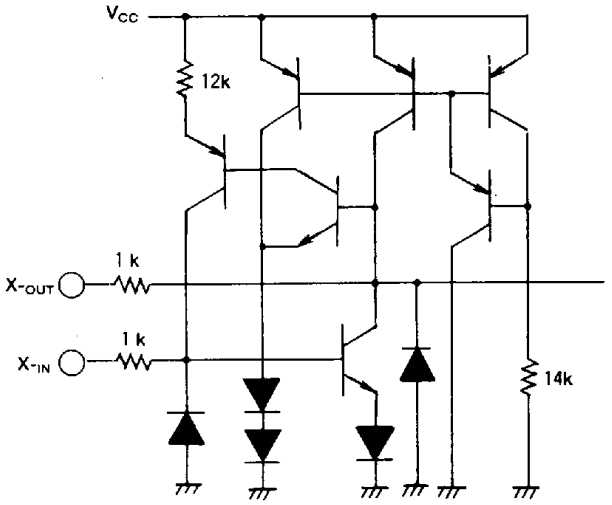

4 PD output




5 PSC output




6 OSC circuit




Note 11 : Resistance and current values shown are typical at $T_a$=25℃.

# PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

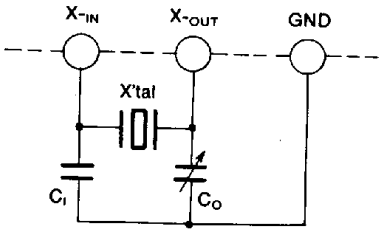
## ABSOLUTE MAXIMUM RATINGS ($T_a$=−20∼+75℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{CC}$ | Supply voltage | | −0.5 | 6.0 | V |
| $V_I$ | Input voltage | $F_{IN}$, $V_{REF}$, $X_{-IN}$, $X_{-OUT}$ input | −0.5 | 2.0 | V |
| | | $D_A$∼$D_D$, Reset, $\overline{CPS}$, Test inputs | | 6.0 | |
| $V_O$ | Output voltage | All outputs | | $V_{CC}$ | V |
| $P_d$ | Power dissipation | $T_a$=75℃ | | 600 | mW |
| Topr | Operating temperature | | −20 | +75 | ℃ |
| Tstg | Storage temperature | | −40 | +125 | ℃ |

## RECOMMENDED OPERATING CONDITIONS ($T_a$=−20∼+75℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit | Remark |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| $V_{CC}$ | Supply voltage | | 4.75 | 5.0 | 5.25 | V | |
| $F_{IN}$ | Input frequency | | 3 | | 30 | MHz | Sine wave input |
| $V_{IN}$ | Input amplitude | $F_{IN}$ = 3∼15MHz | 200 | | 800 | $mV_{P-P}$ | |
| | | $F_{IN}$ =15∼30MHz | 200 | | 800 | | |
| $I_{OL}$ | Low-level output current | $\overline{Lock}$ output | | 1 | 5 | mA | |
| $f_{OSC}$ | Reference frequency | | | 10 | | MHz | |

## CRYSTAL OSCILLATOR CIRCUIT




Note 12 : Specifications of crystal oscillator
Resonant frequency 10MHz±30ppm
Capacitive load 20pF
Effective resistancb<100Ω
13 : Capacitance
$C_I$=56pF, $C_O$=30pF (trimmer)

## ELECTRICAL CHARACTERISTICS ($T_a$=−20∼+75℃, unless otherwise noted)

| Symbol | Parameter | Test pin | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High-level input voltage | Pins 2∼7, 10 | $V_{CC}$=5.5V | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | Pins 2∼7, 10 | $V_{CC}$=5.5V | | | 0.6 | V |
| $I_{IH}$ | High-level input current | Pins 2∼7, 10 | $V_{CC}$=5.5V, $V_{IH}$=5.5V | | | 30 | μA |
| $I_{IL}$ | Low-level input current | Pins 2∼7, 10 | $V_{CC}$=4.5V, $V_{IL}$=0V | | −80 | −160 | μA |
| $V_{OL}$ | Low-level output voltage | Pin 8 | $V_{CC}$=4.5V, $I_{OL}$=5mA | | | 0.5 | V |
| $V_{OHP1}$ | PD high-level output voltage | Pin 1 | $V_{CC}$=4.5V, $I_{OH}$=−1mA | 3.0 | | | V |
| $V_{OHP2}$ | PD high-level output voltage | Pin 1 | $V_{CC}$=5V, $I_{OH}$=−0.1mA | 4.0 | | | V |
| $V_{OLP1}$ | PD low-level output voltage | Pin 1 | $V_{CC}$=4.5V, $I_{OL}$=1mA | | | 1.5 | V |
| $V_{OLP2}$ | PD low-level output voltage | Pin 1 | $V_{CC}$=5V, $I_{OL}$=0.1mA | | | 1.0 | V |
| $I_{PD1}$ | PD leakage current | Pin 1 | $V_{CC}$=5.5V, $V_O$=0.8∼4.0V | | | ±3.0 | μA |
| $I_{PD2}$ | PD leakage current | Pin 1 | $V_{CC}$=5V, $V_O$=2.5V | | | ±1.0 | μA |
| $I_{ILK}$ | $\overline{Lock}$ leakage current | Pin 8 | $V_{CC}$=5.5V, $V_O$=5.5V | | | 30 | μA |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V | | 60 | 90 | mA |
| $V_{OHPSC}$ | PSC high-level output voltage | Pin 13 | $V_{CC}$=5V, $R_L$=3kΩ | 3.2 | | | V |
| $V_{OLPSC}$ | PSC low-level output voltage | Pin 13 | $V_{CC}$=5V, $R_L$=3kΩ | | | 2.6 | V |

Note 14 : All voltages are measured with respect to circuit ground (pin 9).
15 : Currents are taken to be positive (no sign) when flowing into the circuit and negative when flowing out of the circuit. The minimum and maximum values are taken to be absolute values.

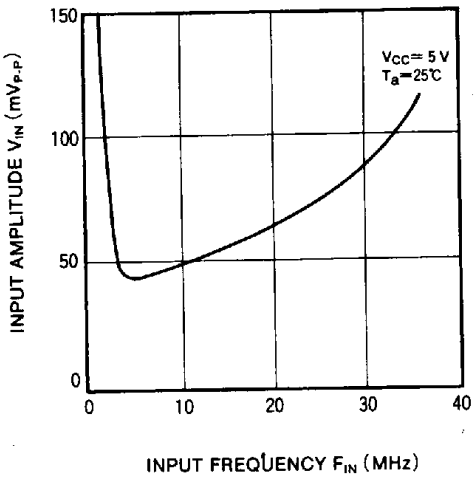
## PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

## AC CHARACTERISTICS ($V_{CC}$= 5 V, $T_a$=25℃, unless otherwise noted)

| Symbol | Parameter | Test pin | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IN1}$ | $F_{IN}$ input sensitivity | 15 | $F_{IN}$ = 3 ~15MHz | | | 200 | $mV_{P-P}$ |
| $V_{IN2}$ | $F_{IN}$ input sensitivity | 15 | $F_{IN}$ =15~30MHz | | | 200 | $mV_{P-P}$ |
| $V_{PSC}$ | $\overline{PSC}$ output amplitude | 13 | $F_{IN}$ =30MHz, $R_L$ = 3 kΩ | 600 | | | $mV_{P-P}$ |

## TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY




## APPLICATION EXAMPLE