M54922P

MITSUBISHI (DGTL LOGIC) 31E D 6249827 0014766 4 MI

PLL FREQUENCY SYNTHESIZER FOR DIGITAL TUNING SYSTEMS

T-77-05-05

DESCRIPTION

The M54922P is a semiconductor integrated circuit consisting of a PLL frequency synthesizer for use in AM/FM electronically tuned radio receivers. It makes use of ECL-IIL process to enable high density and low power consumption. It contains an FM Prescaler allowing the direct input of the local oscillator frequency signal.

The base frequency is provided by a 4.5MHz crystal oscillator.

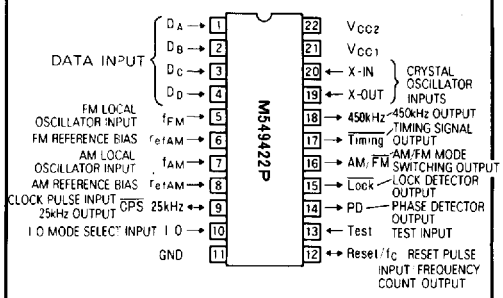
FEATURES

- Built-in FM high-speed prescaler (f_{max}=130MHz)
- Low power consumption (I_{CC}=30mA, typical at V_{CC}=5V)
- Reference frequency selectable from eight values (25k, 12.5k, 10k, 9k, 5k, 4.5k, 2.5k, 1k)
- Modulo-2 swallow counter in FM mode (prescaler ratio 1/16, 1/17)
- Wide range of division ratios (40~65535, binary coded)
- Clock pulse outputs at 450kHz and 500Hz
- Built-in 4.5MHz crystal oscillator (only two external components required)
- PLL rock/unlock status output
- AM/FM mode control output
- High sensitivity AM/FM local oscillator frequency input with built-in amplifier (FM: 160mV$_{p-p}$ at 130MHz, AM: 100mV$_{p-p}$ at 8MHz)

APPLICATION

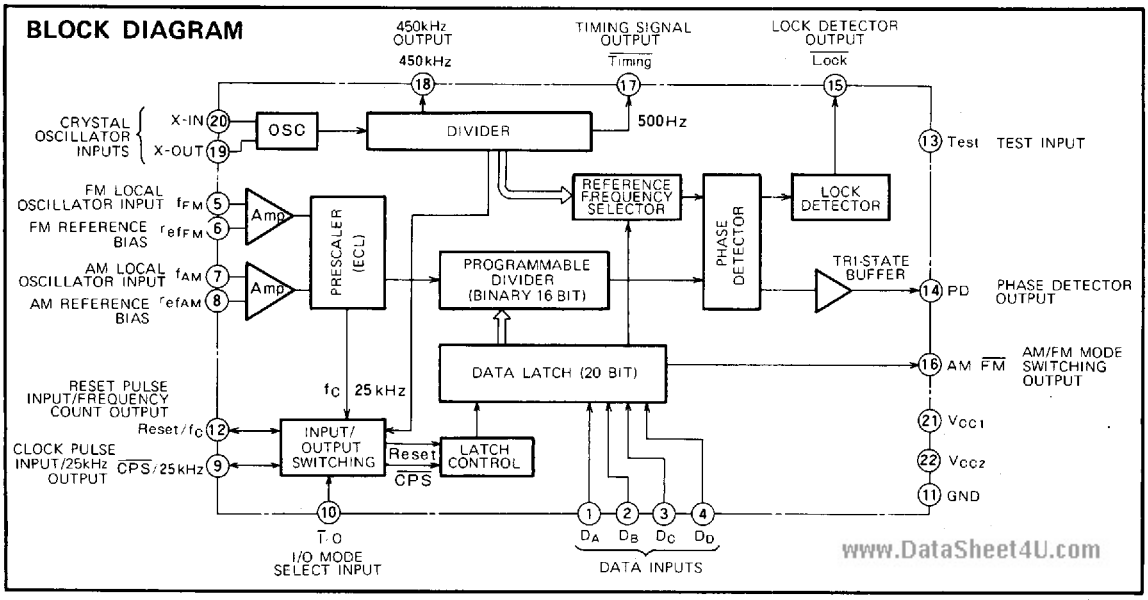
AM/FM Radios

PIN CONFIGURATION (TOP VIEW)



Package Outline 22P4

BLOCK DIAGRAM



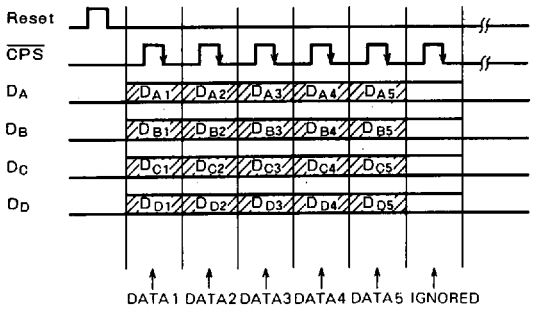
DESCRIPTION OF OPERATION

1. Data Input

(1) External Synchronization

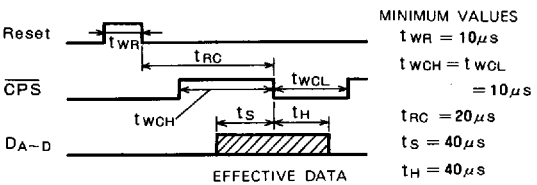
For reading data with external synchronization, set the I/O mode select input to the low state. In this condition, the $\overline{CPS}$/25kHz pin becomes the $\overline{CPS}$ input and reset/FC pin acts as a reset input.

(Input signal formatting)



Note 1. After the reset input goes low, 4x5 bits of data are read by means of 5CPS input pulses (negative edge triggered).
2. Data for the sixth and following CPS input pulses is ignored.

(Input signal timing)

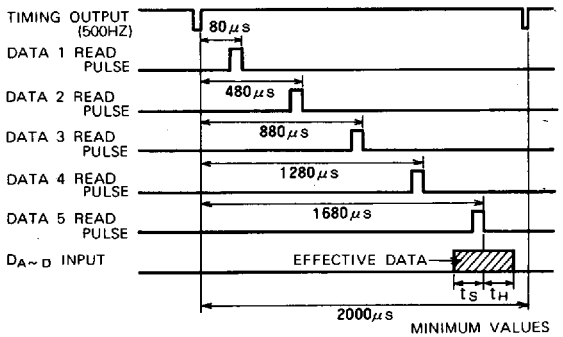


MINIMUM VALUES
$t_{WR} = 10\mu s$
$t_{WCH} = t_{WCL} = 10\mu s$
$t_{RC} = 20\mu s$
$t_S = 40\mu s$
$t_H = 40\mu s$

(2) Internal Synchronization

When the I/O mode select input is set to a high-state, data reading timing is fixed. The timing of data read operations is performed by an internally generated read clock pulse as described in the figure.

(Internally generated read clock pulse timing)



MINIMUM VALUES
$t_S = 40\mu s$
$t_H = 40\mu s$

2. AM/FM Mode Setting and Reference Frequency Selection

AM/FM mode selection and reference frequency selection is performed by means of the data 5 (D_{A5}, D_{B5}, D_{C5}, D_{D5}).

When D_{A5} is read as a high level, the AM mode is selected, enabling the f_{AM} input as well (maximum input frequency 8MHz). For this mode the F_{FM} input is disabled.

When D_{A5} is read as a low level, the FM mode is selected, enabling the f_{FM} input as well (maximum input frequency 130MHz). For this condition the f_{AM} input is disabled.

The selection of reference frequencies is as described in table 1.

Table 1. Reference frequency selection

Data 5				Mode	Reference frequency	AM/FM output
D_{A5}	D_{B5}	D_{C5}	D_{D5}			
L	L	L	L	FM	2.5k	L
H	L	L	L	AM	2.5k	H
L	H	L	L	FM	25k	L
H	H	L	L	AM	25k	H
L	L	H	L	FM	12.5k	L
H	L	H	L	AM	12.5k	H
L	H	H	L	FM	5k	L
H	H	H	L	AM	5k	H
L	L	L	H	FM	4.5k	L
H	L	L	H	AM	4.5k	H
L	H	L	H	FM	9k	L
H	H	L	H	AM	9k	H
L	L	H	H	FM	1k	L
H	L	H	H	AM	1k	H
L	H	H	H	FM	10k	L
H	H	H	H	AM	10k	H

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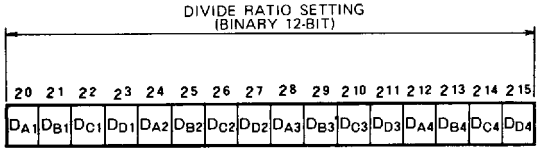
3. Divide Ratio Selection

The divide ratio of the programable divider is set by means of data 1 through data 4. Binary data coding is used. The coding differs for AM and FM modes.

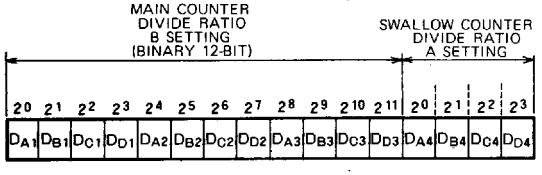
(1) AM mode

The programable divider acts as a normal presettable counter. The divide ratio is set in a binary 16-bit coded format.



(2) FM mode

The programable divider acts as a Modulo-2 swallow counter. The divide ratio is determined by the main counter divide ratio B (binary 12-bit) and the swallow counter divide ratio A (binary 4-bit).



Overall Divide ratio N is determined by

$N=A+16B$

4. Data Coding Example

(1) AM mode, Reference frequency 10kHz, N=207

D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}	D_{A5}	D_{B5}	D_{C5}	D_{D5}
H	H	H	H	L	L	H	H	L	L	L	L	L	L	L	L	H	H	H	H
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}				

$N=2^0+2^1+2^2+2^3+2^6+2^7=1+2+4+8+64+128$
$=207$

REFERENCE FREQUENCY 10KHZ IS SELECTED

AM MODE SELECTION

Note 3. If the PLL goes into lock, $f_{AM}=10\times207=2070kHz$

(2) FM mode, Reference frequency 25kHz, N=2972

D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}	D_{A5}	D_{B5}	D_{C5}	D_{D5}
H	L	L	H	H	H	L	H	L	L	L	L	L	L	H	H	L	H	L	L
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^0	2^2	2^3	2^4				

$N=2^0+2^3+2^4+2^5+2^7=$
$1+8+16+32+128=185$

A=12

REFERENCE FREQUENCY 25kHz IS SELECTED

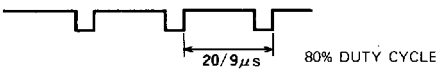
FM MODE SELECTION

Note 4. Overall divide ratio N is given by $N=A+16B$
$=12+16\times185$
$=2972$

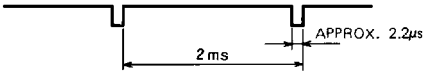
Note 5. If the PLL goes into lock, $f_{FM}=25\times2972=74300kHz$
$=74.3MHz$

5. Clock Signal Output Waveform

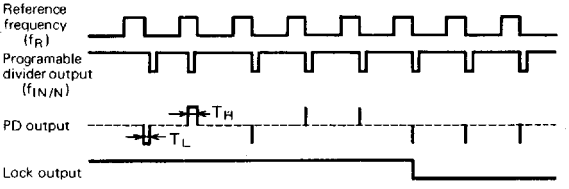
(1) 450kHz output (pin 18)



(2) Timing output (pin 17)



6. PD and Lock Signal Output



Note 1. When the progrannable divider output ($f_{IN}\div N$) lags the reference frequency (f_R) the PD output is low. When it leads the PD output becomes high.

2. If the phase difference T_L or T_H remains below 2.2μs for over three periods of the reference frequency, the lock output goes low indicating the lock condition.

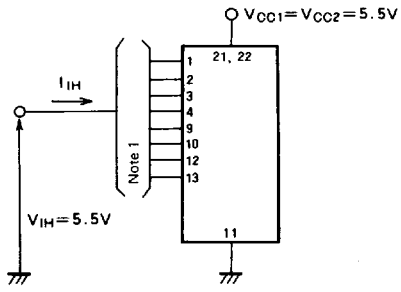
3. The broken line indicates the high impedance state.

PIN DESCRIPTION

Symbol	Name	Description
D_A	Data input	Divide ratio input for programable divider. By modification of the mask pattern, BCD coding is also available.
D_B		
D_C		
D_D		
f_{FM}	FM local oscillator input	Direct input Enable (f_{max}=130MHz) Built-in amplifier (input sensitivity 160mV_{p-p})
ref_{FM}	FM reference bias	Grounded through 1000pF capacitor
f_{AM}	AM local oscillator input	Built-in amplifier (input sensitivity 100mV_{p-p})
ref_{AM}	AM reference bias	Crounded through 10000pF capacitor
$\overline{CPS}$/25kHz	Clock pulse input/25kHz output	I/O pin. Data reading clock input when I/O mode select input (pin 10) is low. 25kHz pulse output when pin 10 is high.
$\overline{I/O}$	I/O mode select input	I/O pin ($\overline{CPS}$/25kHz, reset/f_C) input or output mode select. Set to high for use with the M50170P.
GND	Ground	0V
Reset/f_C	Reset pulse input/frequency count output	I/O pin. Data latch reset input when I/O mode select pin (pin 10) is low. Frequency count output ($f_{FM/160}$, $f_{AM/8}$) when pin 10 is high.
Test	Test input	Normally set to low-state. When set to high-state, pin 14 is the programmable divider output and pin 15 is the reference frequency output.
PD	Phase detector output	Tri-state output. Phase lead for high-state, phase lag for low-state and high-Z for phase coincidence.
$\overline{Lock}$	Lock detector output	Low for PLL lock and high for PLL unlock. Open collector output.
AM/$\overline{FM}$	AM/FM mode switching	AM/FM mode switching output. Low for FM and high for AM. Open collector Output.
$\overline{Timing}$	Timing signal output	500Hz clock pulse output Open collector.
450 kHz	450kHz output	450kHz clock pulse output Open collector
X-IN	Crystal oscillator inputs	4.5MHz crystal input
X-OUT		
V_{CC1}	Power supply 1	5V ± 0.5V I^2L (4.5MHz → 500Hz divider) power supply
V_{CC2}	Power supply 2	5V ± 0.5V ECL and I^2L power supply for all circuits except 4.5MHz → 500Hz divider

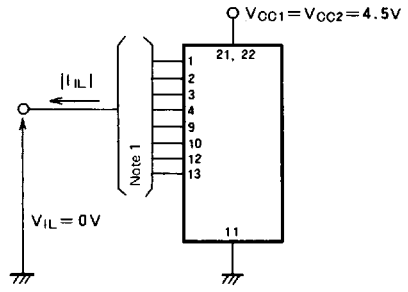
MEASUREMENT CIRCUITS

1



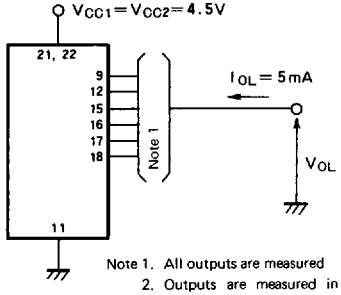
Note 1. All inputs are measured

2



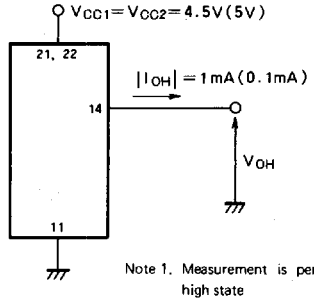
Note 1. All inputs are measured

3



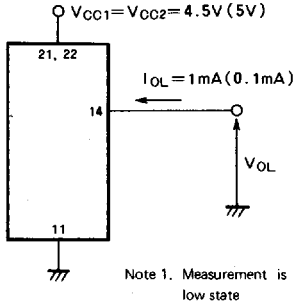
Note 1. All outputs are measured
2. Outputs are measured in the on state

4



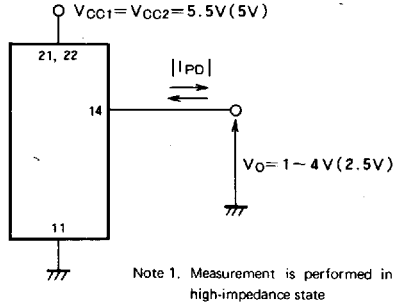
Note 1. Measurement is performed in the high state

5



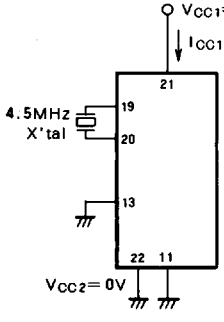
Note 1. Measurement is performed in the low state

6



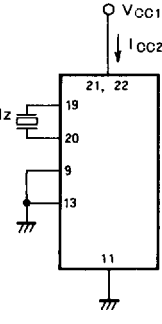
Note 1. Measurement is performed in the high-impedance state

7



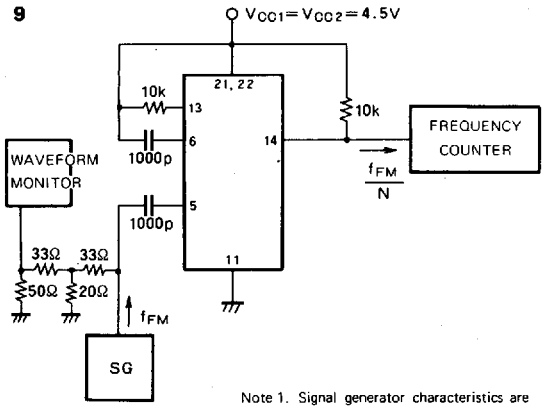
Note 1. 4.5MHz crystal is used.
2. All input pins except the test pin (pin 13) are left open

8



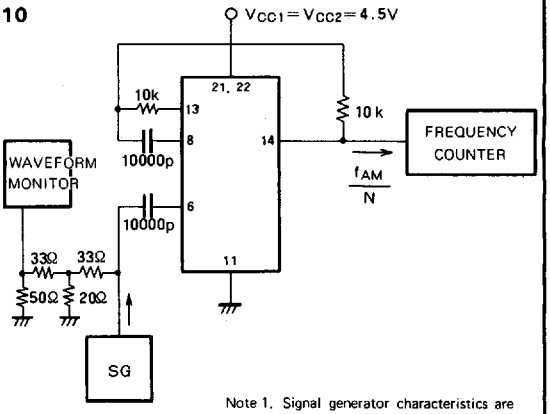
Note 1. 4.5MHz crystal is used.
2. The test pin (pin 13) and I/O pin (pin 9) are grounded
3. The FM mode is selected (with the prescaler enabled)
4. All output pins are left open

9



Note 1. Signal generator characteristics are as follows
(1) 160mV$_{p\text{-}p}$ (60~130MHz)
400mV$_{p\text{-}p}$ (8~60MHz)
(2) Sinewave output
(3) Output impedance Z_0 approx. 50Ω
2. Test pin (pin 13) is set to high and the output from pin 14 (PD) of $f_{FM/N}$ is counted.

10



Note 1. Signal generator characteristics are as follows
(1) 100mV$_{p\text{-}p}$ (2~8.0MHz)
200mV$_{p\text{-}p}$ (0.5~5MHz)
(2) Sinewave output
(3) Output impedance approx. 50Ω
2. Test pin (pin 13) is set to high and the output from pin 14 (PD) of $f_{AM/N}$ is counted.

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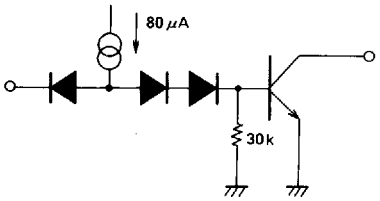
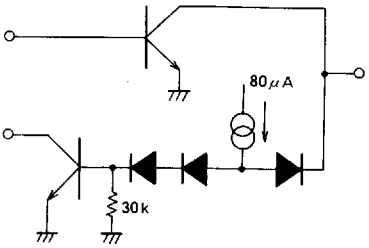
INPUT/OUTPUT CIRCUITS

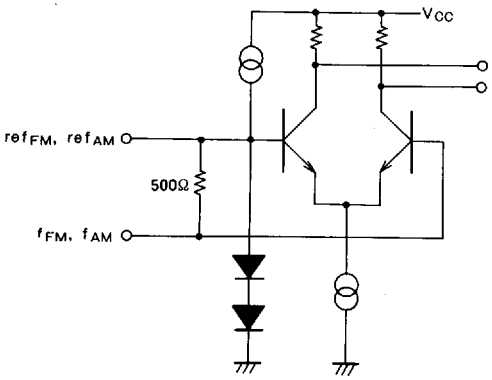
(1) I/O, D_A, D_B, D_C, D_D, Test inputs



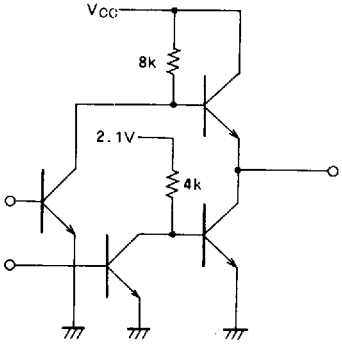
(2) $\overline{CPS}$/25kHz, Reset/f_C input/output



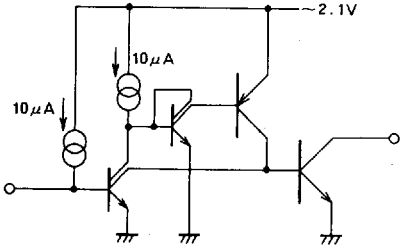
(3) f_{FM}, f_{AM} inputs



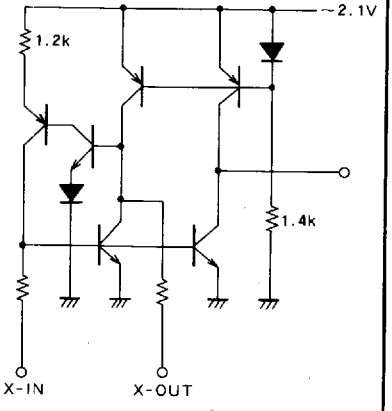
(4) PD output



(5) AM/$\overline{FM}$, $\overline{Lock}$, $\overline{Timing}$, 450kHz outputs



(6) OSC circuit



Note: Resistance and current values are typical values for T_a=25°C.

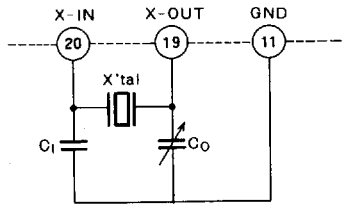
ABSOLUTE MAXIMUM RATING (Ta = −20 ~ +75 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
V_{CC}	Supply voltage	V_{CC1}, V_{CC2}	−0.5	6.0	V
V_I	Input voltage		−0.5	6.0	V
V_O	Output voltage			V_{CC}	V
P_D	Power dissipation	Ta = 75°C		300	mW
Topr	Operating temperature		−20	+75	°C
Tstg	Storage temperature		−40	+125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.5 ~ 5.5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ	Max.	
V_{CC}	Supply voltage	V_{CC1}, V_{CC2}		4.5	5	5.5	V
f_{Local}	Input frequency	f_{AM}		0.5		8	MHz
		f_{FM}		8		130	
V_{Local}	Input amplitude	f_{AM}	0.5 ~ 2MHz	200		800	mV_{P-P}
			2 ~ 8MHz	100		800	
		f_{FM}	8 ~ 60MHz	400		800	mV_{P-P}
			60 ~ 130MHz	160		800	
I_{OL}	Low-level output current	Pin 9, 12, 15, 16, 17, 18 outputs			1	5	mA
f_{OSC}	Reference oscillator frequency				4.5		MHz

Crystal Element Connection Circuit



Note 1. Crystal specifications
Resonant frequency 4.5MHz±30ppm
Load capacitance 20pF
Effective resistance 100Ω, max.
2. Capacitance values
C_I=56pF
C_O=30pF (trimmer)

ELECTRICAL CHARACTERISTICS (Ta = −20~+75°C, unless otherwise noted)

Symbol	Parameter	in	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	1, 2, 3, 4, 9, 10, 12, 13	$V_{CC1}=V_{CC2}=5.5V$	2.0			V
V_{IL}	Low-level input voltage	1, 2, 3, 4, 9, 10, 12, 13	$V_{CC1}=V_{CC2}=5.5V$			0.6	V
I_{IH}	High-level input current	1, 2, 3, 4, 9, 10, 12, 13	$V_{CC1}=V_{CC2}=5.5V$ $V_{IH}=5.5V$			30	μA
I_{IL}	Low-level input current	1, 2, 3, 4, 9, 10, 12, 13	$V_{CC1}=V_{CC2}=4.5V$ $V_{IL}=0V$		−80	−160	μA
V_{OL}	Low-level output voltage	9, 12, 15, 16, 17, 18	$V_{CC1}=V_{CC2}=4.5V$ $I_{OL}=5mA$			0.5	V
V_{OHP1}	PD high-level output voltage	14	$V_{CC1}=V_{CC2}=4.5V$ $I_{OH}=-1mA$	2.4			V
V_{OHP2}		14	$V_{CC1}=V_{CC2}=5V$ $I_{OH}=-0.1mA$	4.0			V
V_{OLP1}	PD low-level output voltage	14	$V_{CC1}=V_{CC2}=4.5V$ $I_{OL}=1mA$			0.5	V
V_{OLP2}		14	$V_{CC1}=V_{CC2}=5V$ $I_{OL}=0.1mA$			0.2	V
I_{PD1}	PD leakage current	14	$V_{CC1}=V_{CC2}=5.5V$ $V_O=1\sim4V$			±1.0	μA
I_{PD2}		14	$V_{CC1}=V_{CC2}=5V$ $V_O=2.5V$		±0.1	±100	nA
I_{CC1}	Circuit current		$V_{CC1}=5.5V$, $V_{CC2}=0V$		3	6	mA
I_{CC2}			$V_{CC1}=V_{CC2}=5.5V$		30	50	mA

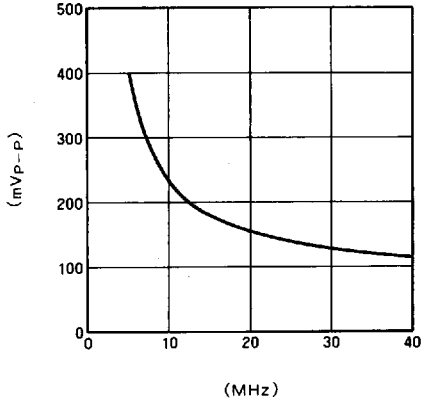
Note 1. All voltages are measured with respect to circuit ground (pin 11) at 0V.
2. Currents are taken to be positive when flowing into the circuit and negative when flowing out of the circuit, the minimum and maximum values taken to be absolute values.
3. The typical values are for V_{CC}=5V and T_a=25°C.

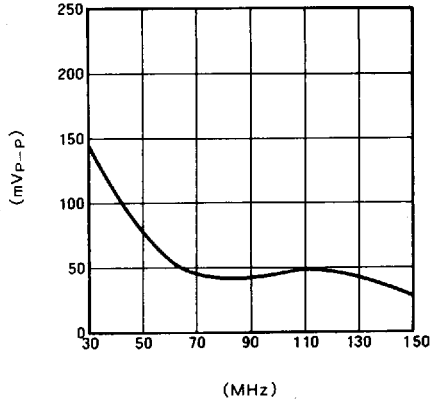
AC CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{FM1}	FM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$ $f_{FM}=60\sim130MHz$			160	mV_{P-P}
V_{FM2}	FM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$ $f_{FM}=8\sim60MHz$			400	mV_{P-P}
V_{AM1}	AM input sensitivity	7	$V_{CC1}=V_{CC2}=4.5V$ $f_{AM}=2\sim8.0MHz$			100	mV_{P-P}
V_{AM2}	AM input sensitivity	7	$V_{CC1}=V_{CC2}=4.5V$ $f_{AM}=0.5\sim2MHz$			200	mV_{P-P}

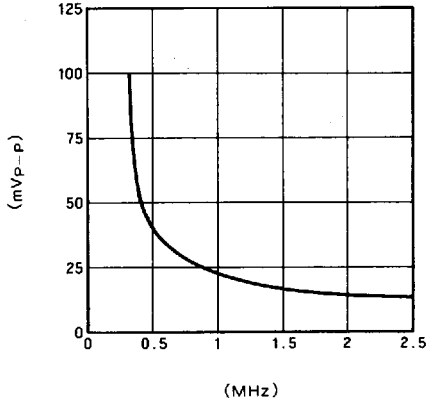
TYPICAL INPUT SENSITIVITY CHARACTERISTICS ($V_{CC1}=V_{CC2}=5V$, $Ta=25°C$)

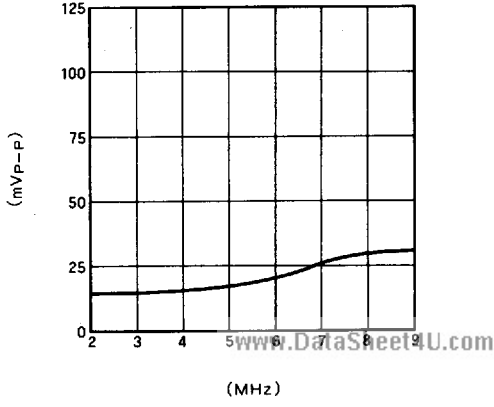
(1) MINIMUM FM INPUT AMPLITUDE VS INPUT FREQUENCY





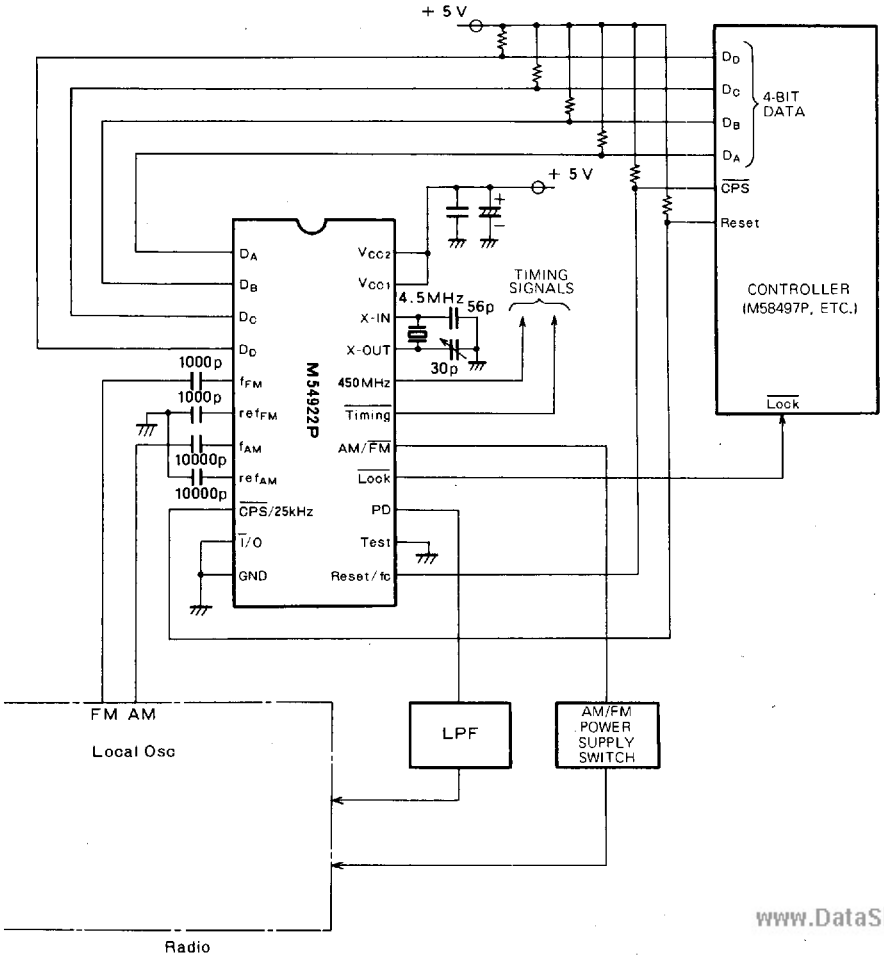
(2) MINIMUM AM INPUT AMPLITUDE VS INPUT FREQUENCY





APPLICATION EXAMPLES

1. External Synchronization



2. Internal Synchronization