ATT7030A User Manual

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Chapter 1 Introduction

§1.1 Features

• High accuracy, less than 0.1% over a dynamic range of 1000 to 1;
• Active energy measure accord with 1S, 0.5S, supports IEC 687/1036, GB/T 17215-1998;
• Provide active energy measurement;
• Provide negative power indication REVP when any one phase active power is negative;
• Provide negative phase indication when 3-phase combined power is negative, which can be used for stopping reverse situation NEGP;
• Provide phase-cut indication PA/PB/PC;
• Provide calibration pulse output for active energy: CF1;
• Provide pulse output F1/F2 for driving electromechanical counter and stepper motor;
• Selectable calculating mode for 3 phase energy combined;
• Adjustable meter constant;
• Startup current 0.1%;
• Accurate measure for active power which contain 21st harmonic;
• Provide gain and phase compensation, nonlinear compensation for little current;
• Supplies resistance network calibration;
• Compatible with 3-phase 3-wire and 3-phase 4-wire;
• Single +5V power supply;
• QFP44 package.

§1.2 Functional description

ATT7030A is a high accuracy 3-phase active electronic energy metering chip which is suitable for 3-phase 3-wire and 3-phase 4-wire.

ATT7030A incorporates 6 second-order sigma-delta ADCs, reference voltage circuitry and the entire signal processing required calculating digital power.

ATT7030A is suitable for measuring active power; it provides phase-cut indication, negative power indication, and negative phase indication for 3-phase combined power.

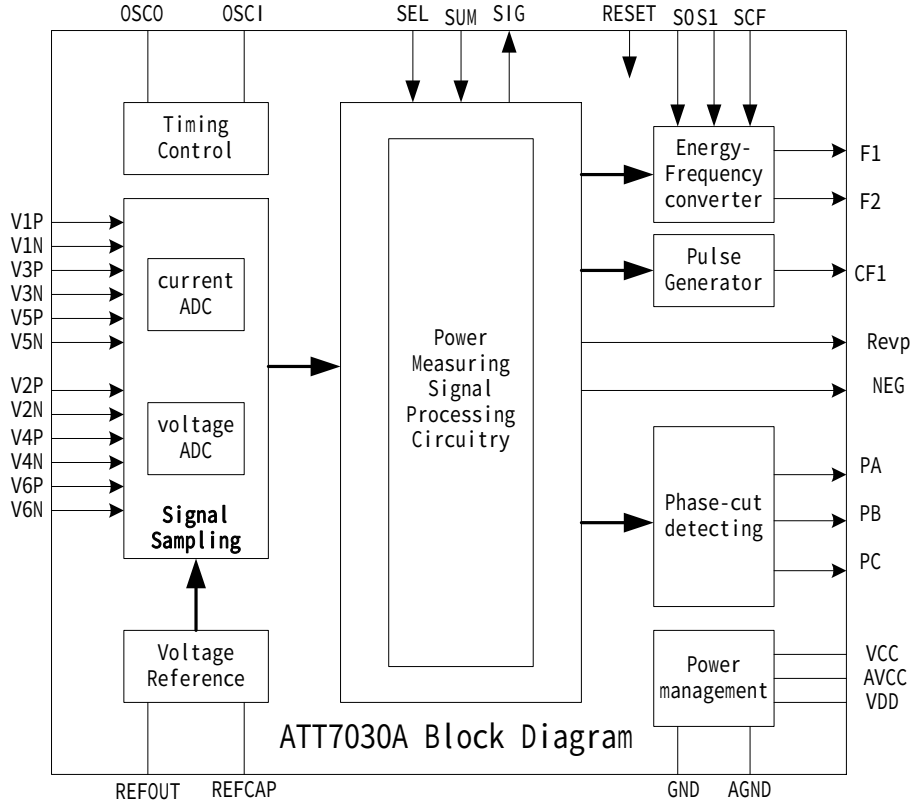
ATT7030A provides pulse output which can be used directly to calibrate error.

ATT7030A provides low frequency pulse output which can be used to drive electromechanical counter..

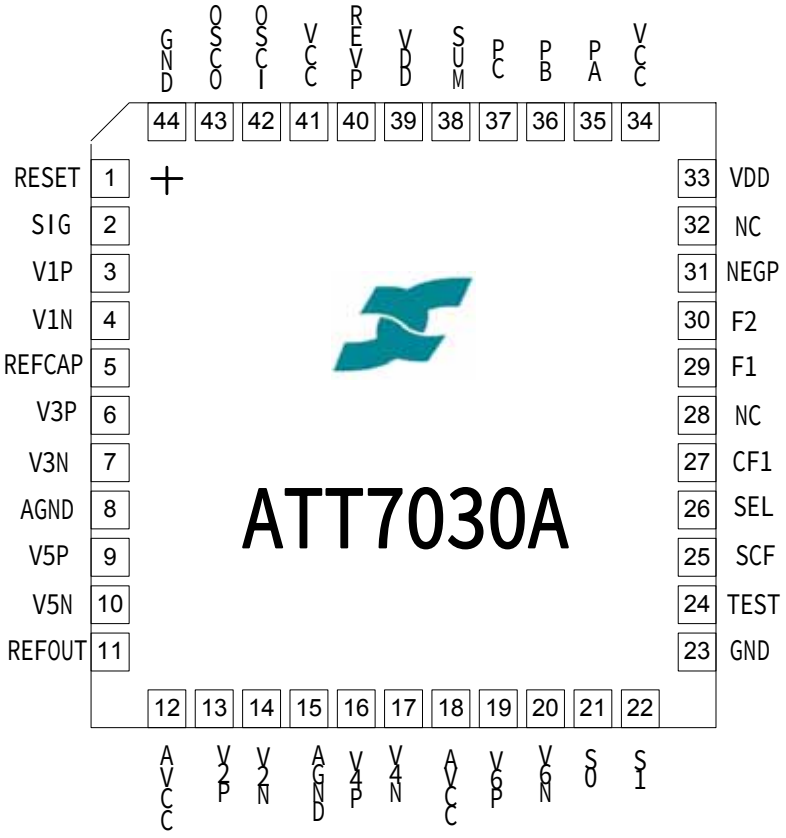
ATT7030A supports resistance network calibration. The system error can be calibrated to suffice class 1S via adjusting resistance network. The pulse for active energy (CF1) can be connected directly to standard meter for calibration. Refer to chapter 3 for detailed calibration method.

Power supply monitor circuitry safeguards ATT7030A's performance.

§1.3 Block diagram



§1.4 Pin definition



Pin	Name	I/O	Description
1	RESET	I	ATT7030A reset, low active. Internally pull-high 47K resistance.
2	SIG	O	SIG is low level when normal work.
3,4	V1P/V1N	I	Analog inputs for A phase current channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage.
5	REFCAP	O	Internal reference voltage, 2.4V, can be connected to external reference voltage. This pin should be decoupled with a 10μF and a 0.1uF capacitor to AGND.
6,7	V3P/V3N	I	Analog inputs for B phase current channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage.
8	AGND	AGND	The analog ground is the ground reference for all analog circuitry.

9,10	V5P/V5N	I	Analog inputs for C phase current channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage.
11	REFOUT	O	Reference voltage output, acts as bias for input signals.
12	AVCC	AVCC	Analog power supply, the supply voltage should be maintained at 5V±5 % for specified operation. This pin should be decoupled with a 10μF and a 0.1uF capacitor to AGND.
13,14	V2P/V2N	I	Analog inputs for A phase voltage channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage.
15	AGND	AGND	The analog ground is the ground reference for all analog circuitry.
16,17	V4P/V4N	I	Analog inputs for B phase voltage channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage.
18	AVCC	AVCC	Analog power supply, the supply voltage should be maintained at 5V±5 % for specified operation. This pin should be decoupled with a 10μF and a 0.1uF capacitor to AGND.
19,20	V6P/V6N	I	Analog inputs for C phase voltage channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage.
21,22	S0/S1	I	Select coefficient for output frequency. Internally pull-high 300K resistance.
23	GND	GND	Digital ground.
24	TEST	I	Test pin, should tie to GND normally. Internally pull-low 47K resistance.
25	SCF	I	Select coefficient for output frequency, cooperate with S0/S1. Internally pull-high 300K resistance.

26	SEL	I	System mode selection, high for 3-phase 4-wire, low for 3-phase 3-wire. Internally pull-high 300K resistance.
27	CF1	O	Active energy pulse output.
28	NC	---	No connection
29,30	F1/F2	O	Low frequency active energy pulse output denotes 3-phase average active power. Be used for driving electromechanical counter.
31	NEGP		NEGP: when 3-phase active power is negative, output high level. When 3-phase active power is positive, output low level.
32	NC	---	No connection
33,39	VDD	VDD	3.0V Power output. This pin should be decoupled with a 10μF and a 0.1uF capacitor to GND.
34,41	VCC	VCC	Digital power supply, the supply voltage should be maintained at 5V±5%. This pin should be decoupled with a 10μF and a 0.1uF capacitor to GND.
35	PA	O	Phase A power-cut indication, outputs high level when phase A voltage loss.
36	PB	O	Phase B power-cut indication, outputs high level when phase B voltage loss.
37	PC	O	Phase C power-cut indication, outputs high level when phase C voltage loss.
38	SUM	I	3-phase combined energy addition mode select. Internally pull-low 300K resistance. 0: denotes absolute addition in 3-phase 4-wire mode, algebraic addition in 3-phase 3-wire mode. 1: denotes algebraic addition in 3-phase 4-wire mode, absolute addition in 3-phase 3-wire mode.
40	REVP	O	Goes high when any one phase active power is negative, goes low when all phase active power is positive.
42	OSCI	I	System oscillator input. Oscillator frequency is 24.576MHz.
43	OSCO	O	System oscillator output.
44	GND	GND	Digital ground.

Note: In application circuitry schematics, both analog ground and digital ground (Pin 8, 15, 23, and 44) must be short connected to guarantee equipotential.

§1.5 Application diagram

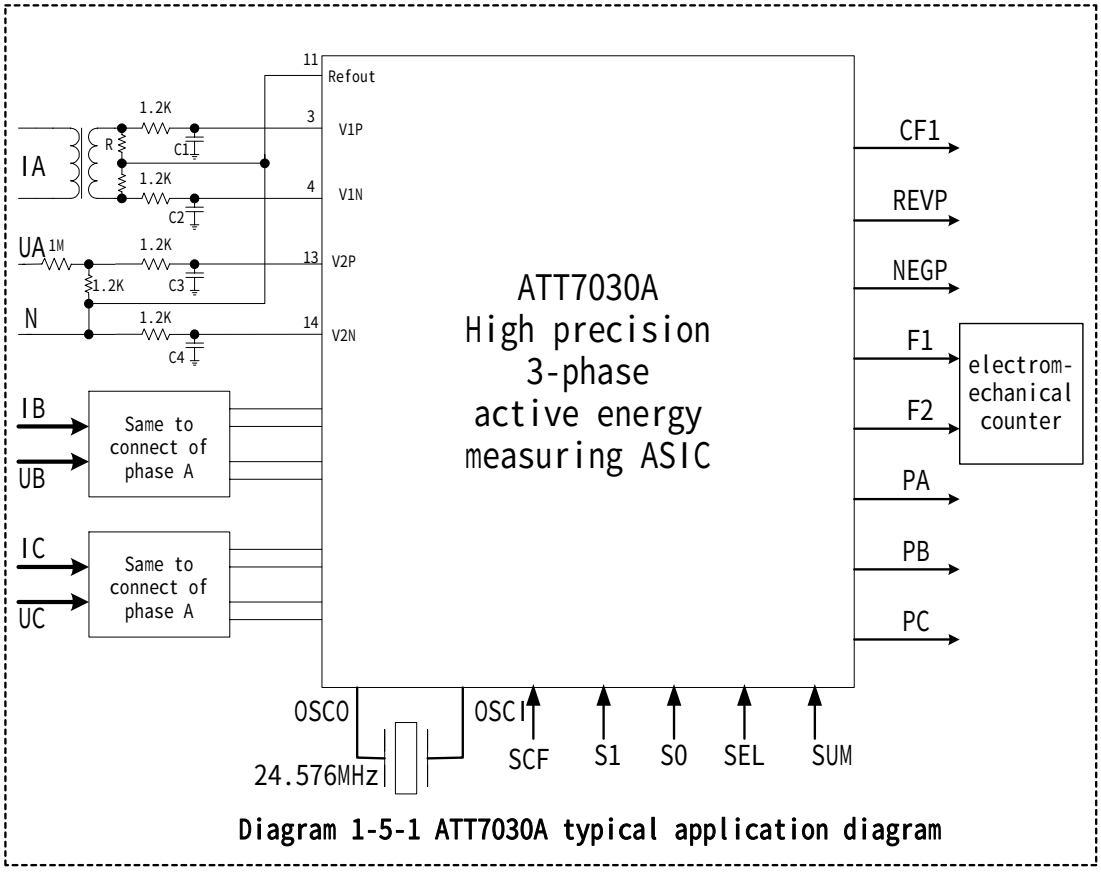


Diagram 1-5-1 ATT7030A typical application diagram

Chapter 2 System Functions

§2.1 Power supply monitor

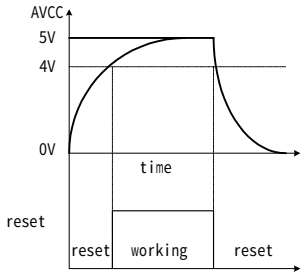


Diagram 2-1 power supply monitor

ATT7030A contains an on-chip power supply monitor. The analog supply (AVCC) is continuously monitored by the ATT7030A. If the supply is less than 4V±5%, the ATT7030A will be reset. This is useful to ensure correct device start-up at power-on and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to false trigger due to noisy supplies, as illustrated in the figure 2-1. The power supply should be decoupled so that the ripple at AVCC does not exceed 5V±5% for normal operation.

§2.2 ADC

There are 6 ADCs in ATT7030A, all of which use fully differential voltage inputs, with a maximum input voltage of ±1.0V. For proper application, we suggest that voltage channel input set at 0.5V and current channel input (at base current –Ib) set at 0.1V.

The typical value of reference voltage (Refcap and Refout) is 2.4V.

Block diagram of ADC in ATT7030A:

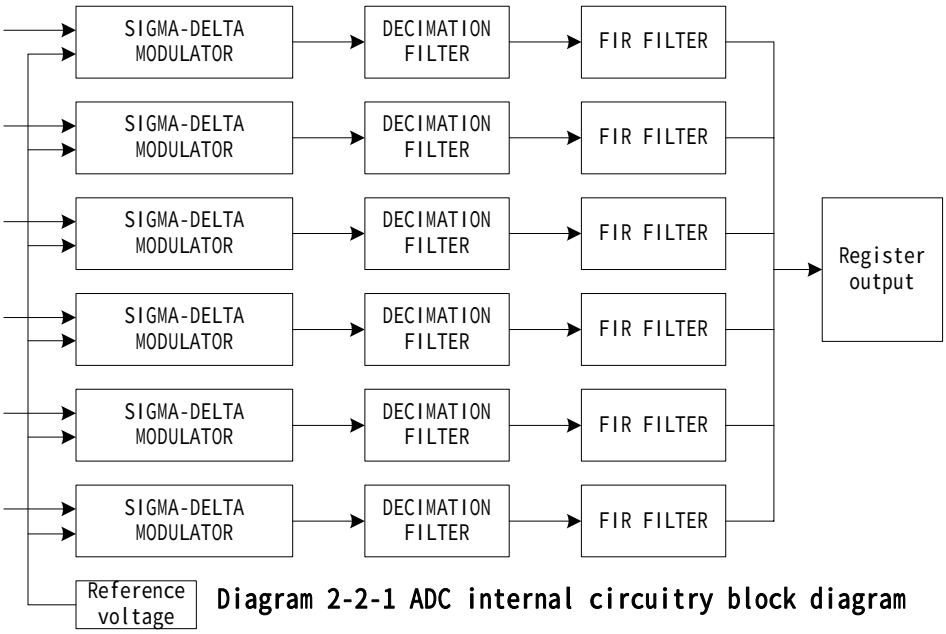


Diagram 2-2-1 ADC internal circuitry block diagram

Typical input circuitry:

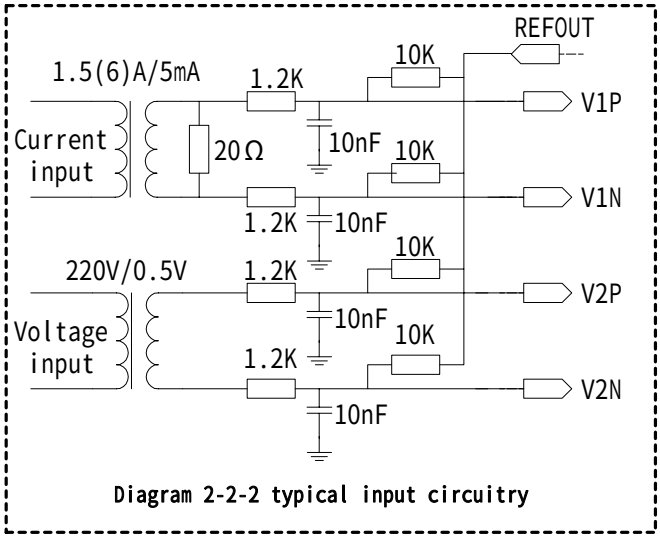


Diagram 2-2-2 typical input circuitry

§2.3 Active power measure

Calculation of active power for each phase is achieved by multiplication, addition and digital filtering, which act on input voltage and current signals.

The over-sampling of sigma-delta ADC guarantees sampling rate of input signals, and the sampled data contains information for up to 21st harmonic. And according to the formula P= $\frac{1}{N}\sum_{n=0}^{N}U(n)\bullet I(n)$, the active power contains information for up to 21st harmonic.

The measure elements of active power is illustrated in the nether figure, 3-phase combined active power Pt=Pa+Pb+Pc.

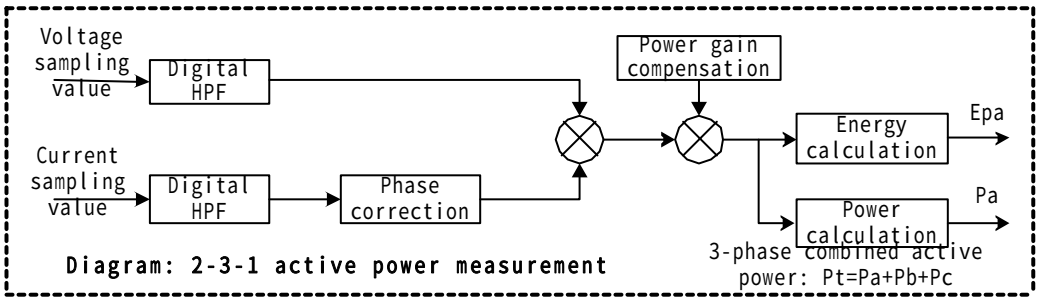


Diagram: 2-3-1 active power measurement

§2.4 Active energy measure

Calculation of active energy is achieved via instantaneous active power integrating to the time.

The formula of single phase active energy: $Ep=\int p(t)dt$

The 3-phase combined active energy could be summated according to algebraic addition mode or absolute addition mode, which could be set.

Algebraic addition mode: Ept=Epa+Epb+Epc

Absolute addition mode: Ept=|Epa|+|Epb|+|Epc|

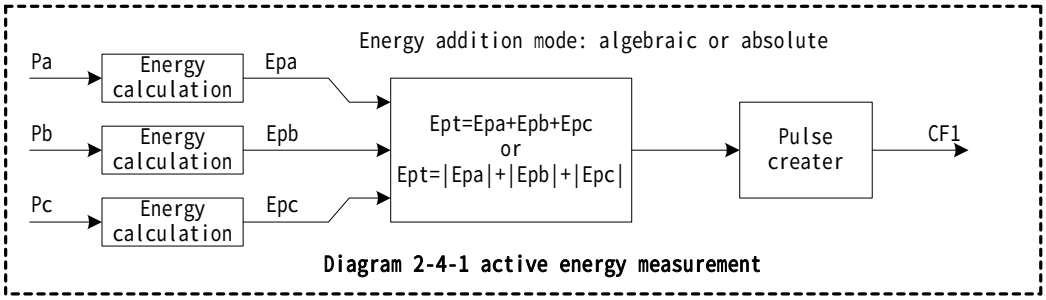


Diagram 2-4-1 active energy measurement

§2.5 power direction judgement

ATT7030A supplies real time active power direction indication.

Negative power indication REVP: if any one phase active power is negative, REVP would output high level, goes low when 3 phase power is positive.

Negative power indication NEGP: if 3-phase combined active power is negative, NEGP would output high level, goes low when 3-phase combined active power is positive. Noticed that NEGP be effectual only in algebraic mode. If we select absolute addition mode, NEGP would output low level all the time.

§2.6 Voltage-depreciation detecting

ATT7030A can detect A/B/C 3 phase voltage-depreciation status basing on configured threshold voltage.

In 3-phase 4-wire mode, threshold voltage is about 50mv for voltage channel input. In 3-phase 3-wire mode, threshold voltage is about 300mv for voltage channel input.

Voltage-depreciation status could be indicated by power-cut indication PA/PB/PC.

Power-cut indication PA/PB/PC output high level denotes A/B/C 3-phase voltage is less than configured threshold voltage, output low level denotes A/B/C 3-phase voltage is higher than configured threshold voltage.

§2.7 Hardware port detecting

ATT7030A can detect hardware port automatically. System will reset when hardware port changes.

ATT7030A has external input port: S0/S1/SCF, SEL, and SUM.

§2.8 Application for 3-phase 3-wire and 3-phase 4-wire

In 3-phase 4-wire mode, ATT7030A uses 3 element measurement method, 3-phase combined power calculated formula is:

$$P_4=\dot{U}_A\dot{I}_A+\dot{U}_B\dot{I}_B+\dot{U}_C\dot{I}_C$$

In 3-phase 3-wire mode, ATT7030A uses 2 element measurement method, 3-phase combined power calculated formula is:

$$P_3=\dot{U}_{AB}\dot{I}_A+\dot{U}_{CB}\dot{I}_C$$

In 3-phase 3-wire mode, phase B channel doesn't take part in power measurement. Only phase A and phase C channel take part in power measurement.

§2.9 energy pulse output

ATT7030A provides two kinds of pulse output: high-frequency pulse output CF1 and low-frequency pulse output F1/F2.

This is energy pulse illustrated diagram:

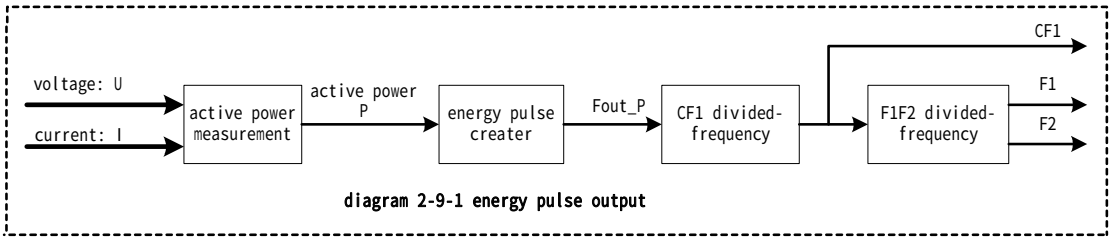


diagram 2-9-1 energy pulse output

In power measurement signal processing circuitry, switched voltage and current signal multiply to get hold of instantaneous power, which integrating to the time to turn into energy. A/B/C phase energy is summated according to algebraic addition mode or absolute addition mode, through switching the result to frequency signal and divided-frequency, then we get hold of high-frequency energy pulse output signal which could be used to calibrate. On this foundation, divided-frequency again can get hold of low-frequency pulse output signal which could be used to drive stepper motor.

Underside is divided-frequency sketch map when high-frequency output constant is 64. The pulse-width of energy pulse output is 90ms. When pulse cycle is less than 180ms, energy pulse output duty cycle is 1 : 1.

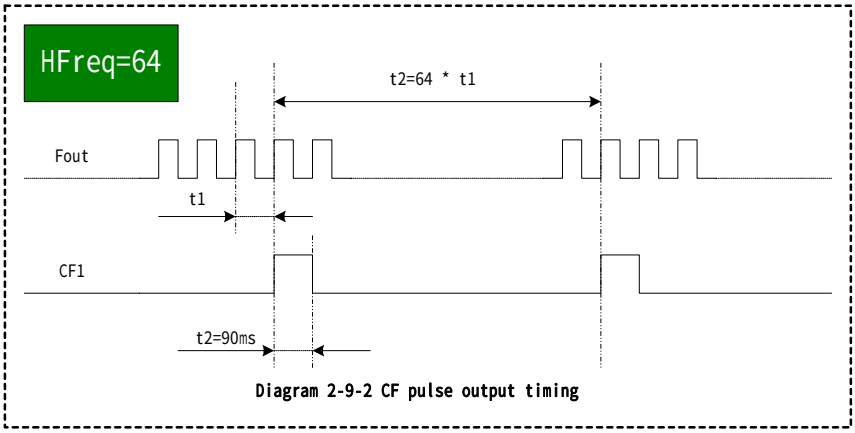


Diagram 2-9-2 CF pulse output timing

Underside is divided-frequency sketch map when low-frequency output constant is 16. The pulse-width of energy pulse output (F1/F2) is 275ms. When pulse cycle is less than 550ms, energy pulse output duty cycle is 1 : 1.

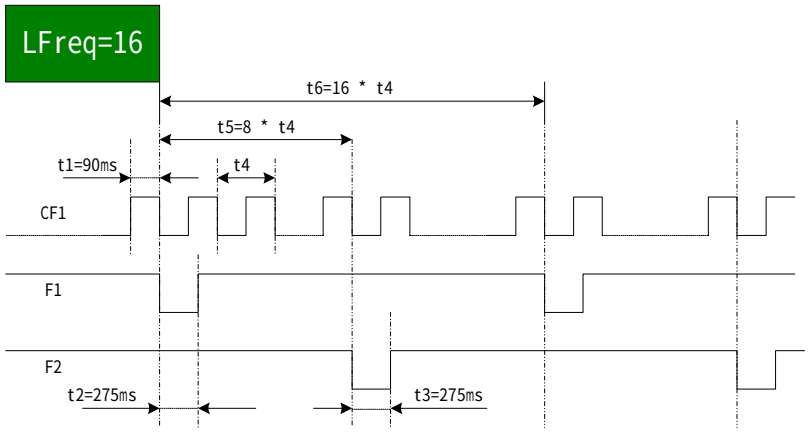


Diagram 2-9-3 F1F2 pulse output timing

Chapter 3 Calibration

§3.1 Calibration elements

ATT7030A supplies resistance network calibration, which calibrates the energy meter via adjusting resistance value in voltage sampling channel. The system active error can be calibrated to suffice class 1S/0.5S.

Start-up and creep:

When current input is rated current (Ib), the sampling voltage is 0.1V, ATT7030A can start-up at 0.1%Ib and prevents creeping at 0.08%Ib.

Single-phase high-frequency output CF formula:

Voltage channel input: Vu

Current channel input: Vi

ATT7030A ADC gain: G = 0.648

Single-phase high-frequency output: CF = 1600*Vu*Vi*G^2/HFreq

Single-phase low-frequency output: LF = CF/Lfreq

HFreq is decided by SCF/S1/S0

List 3-1:

SCF	S1	S0	Hfreq	LFreq
0	0	0	256	16
0	0	1	128	16
0	1	0	128	8
0	1	1	128	4
1	0	0	64	16
1	0	1	64	8
1	1	0	64	4
1	**1**	**1**	Reserved	

When Vu=0.5v, Vi=0.1v, the relation in CF and SCF/S1/S0:

List 3-2:

SCF	S1	S0	HFreq	LFreq	CF(Hz)
0	0	0	256	16	0.1312
0	0	1	128	16	0.2624
0	1	0	128	8	0.2624
0	1	1	128	4	0.2624
1	0	0	64	16	0.5249
1	0	1	64	8	0.5249
1	1	0	64	4	0.5249
1	**1**	**1**	Reserved		

Design advisement:

① We should calculate CF basing on rated voltage Un (Unit: volt), rated current Ib (Unit: amp) and selected calibration constant (Unit: imp/kWh). Then select HFreq in list 3-2 according on CF.

CF calculated formula: CF = EC*Un*Ib/3600000

② When selected electromechanical counter ratio is N:1, we could calculate LFreq according to formula: LFreq=EC*2/N

③ Basing on HFreq and LFreq, we can select SCF/S0/S1 according to list 3-2.

§3.2 Design instance

If Rated voltage: Un = 220V

Rated current: Ib = 5A

Calibration constant: 1600 imp/kWh

Electromechanical counter ratio: 400:1

Then CF=EC*Un*Ib/3600000=1600*220*5/3600000=0.4889Hz

Input ADC current and voltage signal is 0.1V and 0.5V in rated current and rated voltage. According to CF and list 3-2, we select HFreq=64.

LFreq=EC*2/N=1600*2/400=8

SCF/S1/S0=101

§3.3 Reference design circuit diagram

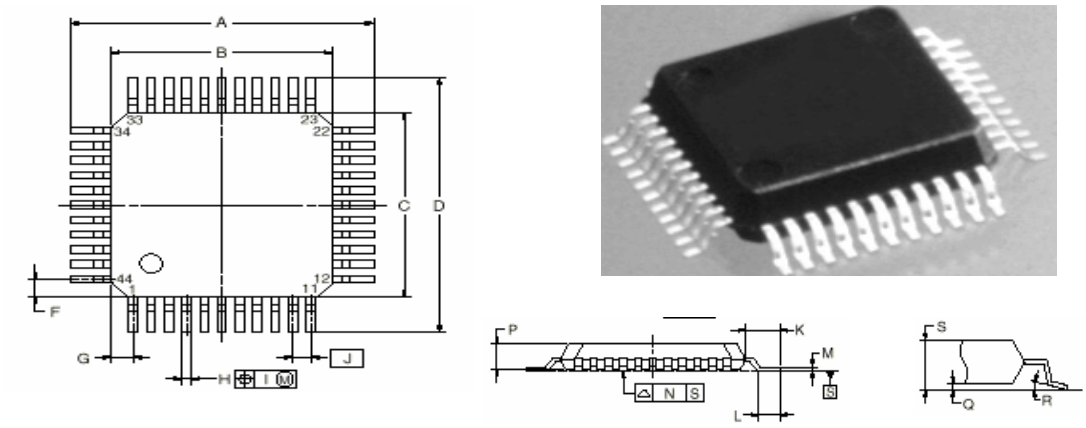
Chapter 4 Electrical Characteristics

§4.1 Electrical parameter

Test object	minimum	typical	Max	unit	Test condition
VCC	4.75	5	5.25	V	
VDD		3.0		V	
Reference voltage	2.3	2.4	2.6	V	
Reference power TC		30		ppm	
Input voltage range			±1.5	V	Difference input Vpp
VOH(F1,F2)	4.5			V	IOH=10mA
VOL(F1,F2)			0.5	V	IOL=10mA
VOH(CF1, REVP, NEGP)	4.5			V	IOH=5mA
VOL(CF1, REVP, NEGP)			0.5	V	IOL=5mA
Logic input high-level	2.5			Vmin	
Logic input low-level			0.8	Vmax	
Logic output high-level	4.5			Vmin	Ioh=2mA
Logic output low-level			0.5	Vmax	Iol=2mA
Reference voltage output resistance: Minimum load resistance Maximum load capacitance	 2	130	 100	 Ω KΩ pF	
Positive power supply current		28		mA	VDD=3.0V ; VCC=5V
ADC bit digit		16		bit	
ADC sampling speed		3.2		kHz	
ADC dynamic range		88		DB	
ADC whole harmonic distortion		-95		DB	
ADC channel disturbance		-92		DB	
Crystal frequency		24.576		MHz	
Temperature range	-40		85	℃	

§4.2 Packaging information

Packaging information: 44Pin QFP (Quad Flat Package 10X10)



NOTE 1. Controlling dimension ---millimeter.

2. Each lead centerline is located within 0.12mm (0.005inch) of
Its true position (T.P.) at maximum material condition

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	0.535 +0.017 -0.016
B	10.0±0.2	0.394 +0.008 -0.009
C	10.0±0.2	0.394 +0.008 -0.009
D	13.6±0.4	0.535 +0.017 -0.016
F	1.0	0.039
G	1.0	0.039
H	0.35 +0.08 -0.07	0.014±0.003
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 +0.008 -0.009
L	0.8±0.2	0.031 +0.009 -0.008
M	0.17 +0.08 -0.07	0.007 +0.003 -0.004
N	0.10	0.004
P	2.7±0.1	0.106 +0.005 -0.004
Q	0.1±0.1	0.004±0.004
R	3° +7° -3°	3° +7° -3°
S	3.0 MAX	0.019 MAX

NEC CODE	P44GB-80-3B4-4
EIAJ CODE	
Weight(Reference Value)	0.54g