

MOS INTEGRATED CIRCUIT μ PD16364

160-BIT HIGH-VOLTAGE CMOS DRIVER

DESCRIPTION

The μ PD16364 is a high-voltage CMOS driver for EL display. It consists of 4 × 40/8 × 20-bit data latch, 160-bits data latch, 160-bit level shifter, and a high-voltage CMOS driver. The logic circuit operates on 5-V power supply (CMOS level input), so that it can be connected to a micro-controller. The driver block is comprised of 60 V, 25 mA MAX. high-voltage output buffer, and both the logic block and driver block employ a CMOS, allowing operation with low power consumption.

FEATURES

- High-voltage Full CMOS process
- High-voltage output (60 V, 25 mA MAX.)
- $4 \times 40/8 \times 20$ -bit data latch (4/8-bit data input)
- High-speed data transfer (fcLK = 16 MHz: in cascade connection)

Package

Wide operating temperature range (T_A = -40 to +85°C)

ORDERING INFORMATION

Part Number

 μ PD16364N -××× TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

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1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.





Remark This figure does not specify the TCP package.

Caution Be sure to use all the VDD1, VDD2, VSS1, and VSS2 pins. Keep the VSS1 and VSS2 pins at the same voltage level.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Description
EIO1	Enable I/O1	I/O	L,/R pin = "L" level: Input
			L,/R pin = "H" level: Output
EIO2	Enable I/O2	I/O	L,/R pin = "H" level: Input
			L,/R pin = "L" level: Output
SCK	Shift Clock Input	Input	Fall edge operation. Input shift clock for 4 x 40/8 x 20-bit data latch.
DST	Data Strobe Input Input Fall edge operation. Data are latched to 160-bits data late		Fall edge operation. Data are latched to 160-bits data latch and also set
			outputs of OUT1 to OUT160.
Do to D7	Data Input	Input	Data input. When BS is low level, D4 to D7 pins should be connected to V_{SS1}
			or V _{DD1} .
L,/R	Select Left or Right	Input	Refer to 4.TRUTH TABLE
	Shift		
OC	Output Control	Input	When OC pin is low level, output is normal operation.
			When OC pin is high level, output become low level.
REV	Invert Input Data	Input	When REV pin is low level, input data D_0 to D_7 are latched without inversion.
			When REV pin is high level, input data D ₀ to D ₇ are inverted before latching.
BS	Bus Select	Input	When BS pin is low level, data bus is4 bits.
			When BS pin is high level, data bus is 8 bits.
OUT1 to	High-voltage output	Output	Output level is Vss2 or VDD2. These outputs are changed by falling edge of
OUT160			DST pin.
V _{DD1}	Logic power supply	_	Logic power supply
VDD2	Driver power supply	_	Driver power supply
Vss1	Logic ground	-	Grounding
Vss2	Driver around	_	Grounding

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4. TRUTH TABLE

Shift Register Block (4 x 40 data latch, BS = L)

L,/R	SCK	1	2	3	 40
L level	D3	1	5	9	 157
	D ₂	2	6	10	 158
	D1	3	7	11	 159
	Do	4	8	12	 160
H level	D₃	160	156	152	 4
	D2	159	155	151	 3
	D1	158	154	150	 2
	Do	157	153	149	 1

Shift Register Block (8 x 20 data latch, BS = H)

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L,/R	SCK	1	2	3	 20
L level	D7	1	9	17	 153
	D ₆	2	10	18	 154
	D₅	3	11	19	 155
	D4	4	12	20	 156
	D3	5	13	21	 157
	D ₂	6	14	22	 158
	D1	7	15	23	 159
	Do	8	16	24	 160
H level	D7	160	152	144	 8
	D ₆	159	151	143	 7
	D₅	158	150	142	 6
	D4	157	149	141	 5
	Dз	156	148	140	 4
	D ₂	155	147	139	 3
	D1	154	146	138	 2
	Do	153	145	137	 1

Control Block

L,/R	EIO1	EIO2
H level	Out	In
L level	In	Out

Driver Block

OC	REV	Dn	Driver Output
L	L	L	L
L	L	Н	Н
L	Н	L	н
L	Н	Н	L
Н	х	х	L (All driver outputs are L.)

5. ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V _{DD1}	-0.5 to +6.0	V
Driver Part Supply Voltage	V _{DD2}	-0.5 to +60	V
Logic Part Input Voltage	VI1	–0.5 to V _{DD1} + 0.5	V
Logic Part Output Voltage	V ₀₁	-0.5 to V _{DD1} + 0.5	V
Driver Part Output Voltage -	V _{O2}	-0.5 to V _{DD2} + 0.5	V
Logic Part Output Current	lo ₁	±10	mA
Driver Part Output Current	lo2	±25	mA
Operating Ambient Temperature	TA	-40 to +85	°C
Storage Temperature	Tstg	-55 to +125	°C

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Cautions 1. $T_A \ge 25^{\circ}C$, load should be alleviated at a rate of -4.5 mW/°C.

2. Product qualify may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range ($T_A = -40$ to $+85^{\circ}C$, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V _{DD1}		4.5	5.0	5.5	V
Driver Part Supply Voltage	V _{DD2}		20		55	V
High-Level Input Voltage	Vін		0.8 Vdd1		Vdd1	V
Low-Level Input Voltage	VIL		0		0.2 Vdd1	V
Driver Part Output Current	lol2				+20	mA
	Іон2				-20	mA

Caution Turn of and off power sequence must be as follows:

Turn-on sequence: $V_{DD1} \rightarrow Input \rightarrow V_{DD2}$

Turn-off sequence: $V_{DD2} \rightarrow Input \rightarrow V_{DD1}$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	Voh1	Logic, Іон1 = -0.4 mA,	V _{DD1} - 0.4			V
	Vон2	OUT1 to OUT160, Iон2 = -1.0 mA	Vdd2 - 0.4			V
Low-Level Output Voltage	Vol1	Logic, IoL1 = 0.4 mA			0.4	V
	Vol2	OUT1 to OUT160, IoL2 = 1.0 mA			0.4	V
High-Level Input Current	Ін	VI = VDD1			5.0	μA
Low-Level Input Current	١L	V1 = 0 V			-5.0	μA
High-Level Input Voltage	VIH	Logic	0.8 VDD1			V
Low-Level Input Voltage	VIL	Logic			0.2 VDD1	V
Ron Variance	Rvar	OUT1 to OUT160 (in one chip			±30	%
		under constant T _i ^{Note1})				
Logic Part Dynamic Current	IDD1	Note2			10	mA
Consumption						
Driver Part Dynamic Current	DD2	Note2			10	mA
Consumption						
Standby Current	standby	Note3			500	μA

Electrical Characteristics (TA = -40 to +85°C, VDD1 = 4.5 to 5.5 V, VDD2 = 55 V, VSS1 = VSS2 = 0 V,)

Notes 1. $R_{var} = (1 - Xn/X_{avg}) \times 100$

Xn = Impedance of OUTn, Xavg = Impedance of average

 $I_{OH2} = -1.0 \text{ mA}, I_{OL2} = 1.0 \text{ mA}$

- 2. fsck = 16 MHz, fbst = 36 kHz, VIN = Vbb1 or Vss1, no load
- 3. VIN = VDD1 or VSS1, no load

Switching Characteristics	$(T_{A} = -40 \text{ to } +85^{\circ}\text{C})$	$V_{DD1} = 45 \text{ to } 55 \text{ V}$	$V_{DD2} = 55 V$	$V_{551} = V_{552} = 0 V$
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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Enable Pulse Delay Time	tPLH1	$DST\downarrow \rightarrow EIOn\uparrow, C_{L} = 30 \ pF$			70	ns
	tPHL2	Last SCK $\downarrow \rightarrow$ EIOn \downarrow , CL = 30 pF			40	ns
Driver Output Delay Time	tphl3	DST↓ → OUT1 to OUT160,			7	μS
	t PLH3	C∟ = 2000 pF			7	μS
Input Capacitance	С				20	pF

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK Cycle Time	tcscк		62			ns
SCK Pulse Width	PWclk		20			ns
DST Cycle Time	t CDST		1000			ns
DST High-Level Pulse Width	PWdst		30			ns
DST-SCK Time	tdst-sck	$DST{\downarrow} \to 1st \: SCK \: {\downarrow}$	100			ns
SCK-DST Time	tsck-dst	Last SCK $\downarrow \rightarrow$ DST \downarrow	30			ns
Data Setup Time	t SETUP		20			ns
Data Hold Time	t HOLD		20			ns
REV Setup Time	t RSETUP		40			ns
REV Hold Time	t RHOLD		30			ns
EIO-SCK Time1	teio-sck1	$EIOn \downarrow \to 1st \ SCK \downarrow$	22			ns
EIO-SCK Time2	teio-sck2	$EIOn^{\uparrow} \to 1st \ SCK \ \uparrow$	25			ns

Timing Requirement ($T_A = -40$ to $+85^{\circ}$ C, $V_{DD1} = 4.5$ to 5.5 V, $V_{DD2} = 55$ V, $V_{SS1} = V_{SS2} = 0$ V, $t_r = t_f = 13.0$ ns)

Switching Characteristics and Timing Requirements Waveform

Timing requirement waveform



Switching characteristics waveform





2 20 ო IC12 data reading 2 **2**0 ო IC3 data reading 2 20 ო IC2 data reading 2 ג ר IC1 data reading ო 2 SCK D₀ to D₇ DST IC1 EIO2 IC2 EI01 / IC3 EI02 IC11 EI01 / IC12 EI02 IC1 EI01 / IC1 EI02 OUT1-OUT160

Timing Example (640 dots x 3/line, BS = H, L,/R = H)

6. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μ PD16364.

For more details, refer to the Semiconductor Device Mounting Technology Manual (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

 μ PD16364N-×××: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm ² : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm ² : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

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NOTES FOR CMOS DEVICES -

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NFC

NEC Semiconductor Device Reliability/Quality Control System (C10983E) Semiconductor Device Mounting Technology (C10535E)

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