

KM48C514D, KM48V514D**CMOS DRAM***512K x 8Bit CMOS Dynamic RAM with Extended Data Out***DESCRIPTION**

This is a family of 524,288 x 8 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), Access time(-5,-6,-7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 512Kx8 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for microcomputer, personal computer and portable machines.

FEATURES• **Part Identification**

- KM48C514D/DL (5V, 1K Ref.)
- KM48V514D/DL (3.3V, 1K Ref.)

• **Active Power Dissipation**

Unit : mW

Speed	3.3V (1K Ref.)	5V (1K Ref.)
-5	-	470
-6	255	385
-7	235	360

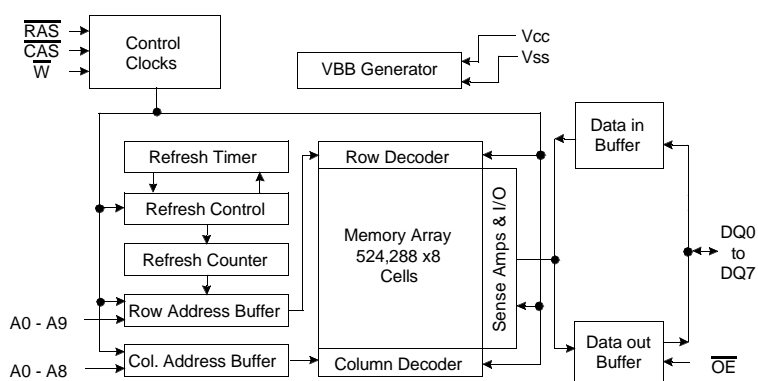
• **Refresh Cycles**

Part NO.	V _{CC}	Refresh cycle	Refresh period	
			Normal	L-ver
C514D	5V	1K	16ms	128ms
V514D	3.3V			

• **Performance Range**

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}	Remark
-5	50ns	15ns	84ns	20ns	5V Only
-6	60ns	15ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V

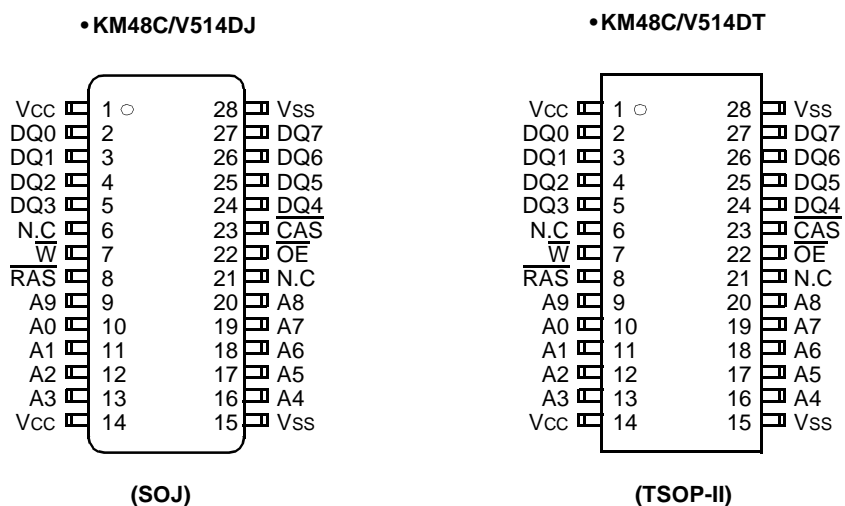
- Extended Data Out Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 28-pin SOJ 400mil & TSOP(II) 400mil packages
- Dual +5V±10% power supply(5V product)
- Dual +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM

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KM48C514D, KM48V514D**CMOS DRAM****PIN CONFIGURATION (Top Views)**

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Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 - 7	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection

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KM48C514D, KM48V514D**CMOS DRAM****ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3* ¹	2.4	-	V _{CC} +1.0* ¹	V
Input Low Voltage	V _{IL}	-0.3* ²	-	0.8	-1.0* ²	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{IN} +0.3V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V



KM48C514D, KM48V514D**CMOS DRAM****DC AND OPERATING CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM48V514D	KM48C514D	
I _{CC1}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
I _{CC2}	Don't care	Don't care	1	2	mA
I _{CC3}	Don't	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
I _{CC4}	Don't care	-5	-	85	mA
		-6	55	70	mA
		-7	50	65	mA
I _{CC5}	Normal L	Don't care	0.5	1	mA
			100	150	uA
I _{CC6}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
I _{CC7}	L	Don't care	200	300	uA
I _{CCS}	L	Don't care	100	200	uA

I_{CC1}* : Operating Current (\overline{RAS} and \overline{CAS} , Address cycling @trc=min.)I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)I_{CC3}* : \overline{RAS} -only Refresh Current ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address cycling @trc=min.)I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address cycling @t_{HPC}=min.)I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current (\overline{RAS} and \overline{CAS} cycling @trc=min.)I_{CC7} : Battery back-up current, Average power supply current, Battery back-up modeInput high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})= $0.2V$, $\overline{CAS}=0.2V$,

DQ=Don't care, TRC=125us, TRAS=TRASmin~300ns

I_{CCS} : Self Refresh Current $\overline{RAS}=\overline{CAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0 \sim A9=V_{CC}-0.2V$ or $0.2V$ DQ0 ~ DQ7= $V_{CC}-0.2V$, $0.2V$ or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6} and I_{CC7}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, t_{HPC}.

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KM48C514D, KM48V514D**CMOS DRAM****CAPACITANCE** ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$ or 3.3V , $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A9]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ7]	CDQ	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C}\leq T_A\leq 70^\circ\text{C}$, See note 1,2)Test condition (5V device) : $V_{CC}=5.0\text{V}\pm 10\%$, $V_{ih}/V_{il}=2.4/0.8\text{V}$, $V_{oh}/V_{ol}=2.0/0.8\text{V}$ Test condition (3.3V device) : $V_{CC}=3.3\text{V}\pm 0.3\text{V}$, $V_{ih}/V_{il}=2.2/0.7\text{V}$, $V_{oh}/V_{ol}=2.0/0.8\text{V}$

Parameter	Symbol	-5*1		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	84		104		124		ns	
Read-modify-write cycle time	t _{RWC}	116		138		163		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		15		15		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	t _{CEZ}	3	13	3	13	3	18	ns	6,12
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		50		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	17		17		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	8	10K	10	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	35	20	45	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	15	35	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	8		10		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	25		30		35		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	8
Write command set-up time	t _{WCS}	0		0		0		ns	7
Write command hold time	t _{WCH}	10		10		10		ns	
Write command pulse width	t _{WP}	10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	13		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	8		10		15		ns	

Note) *1 : 5V only



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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 ^{*1}		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	8		10		15		ns	9
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	32		32		42		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	67		77		92		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	42		47		57		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	45		52		62		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		28		35		40	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		ns	11
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		ns	11
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tCP	8		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		ns	
$\overline{\text{OE}}$ access time	tOEA		15		15		20	ns	3
$\overline{\text{OE}}$ to data delay	tOED	13		13		18		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	3	13	3	13	3	18	ns	6
$\overline{\text{OE}}$ to output in low-Z	tOLZ	3		3		3		ns	
$\overline{\text{OE}}$ command hold time	tOEH	15		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	15	3	15	3	20	ns	6,12
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	13	3	13	3	18	ns	6
$\overline{\text{W}}$ to data delay	tWED	13		13		18		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	tOCH	5		5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		5		5		ns	
$\overline{\text{OE}}$ precharge time	tOEP	5		5		5		ns	
$\overline{\text{W}}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRASS	100		100		100		us	13,14,15
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRPS	90		110		130		ns	13,14,15
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	13,14,15

Note) *1 : 5V only



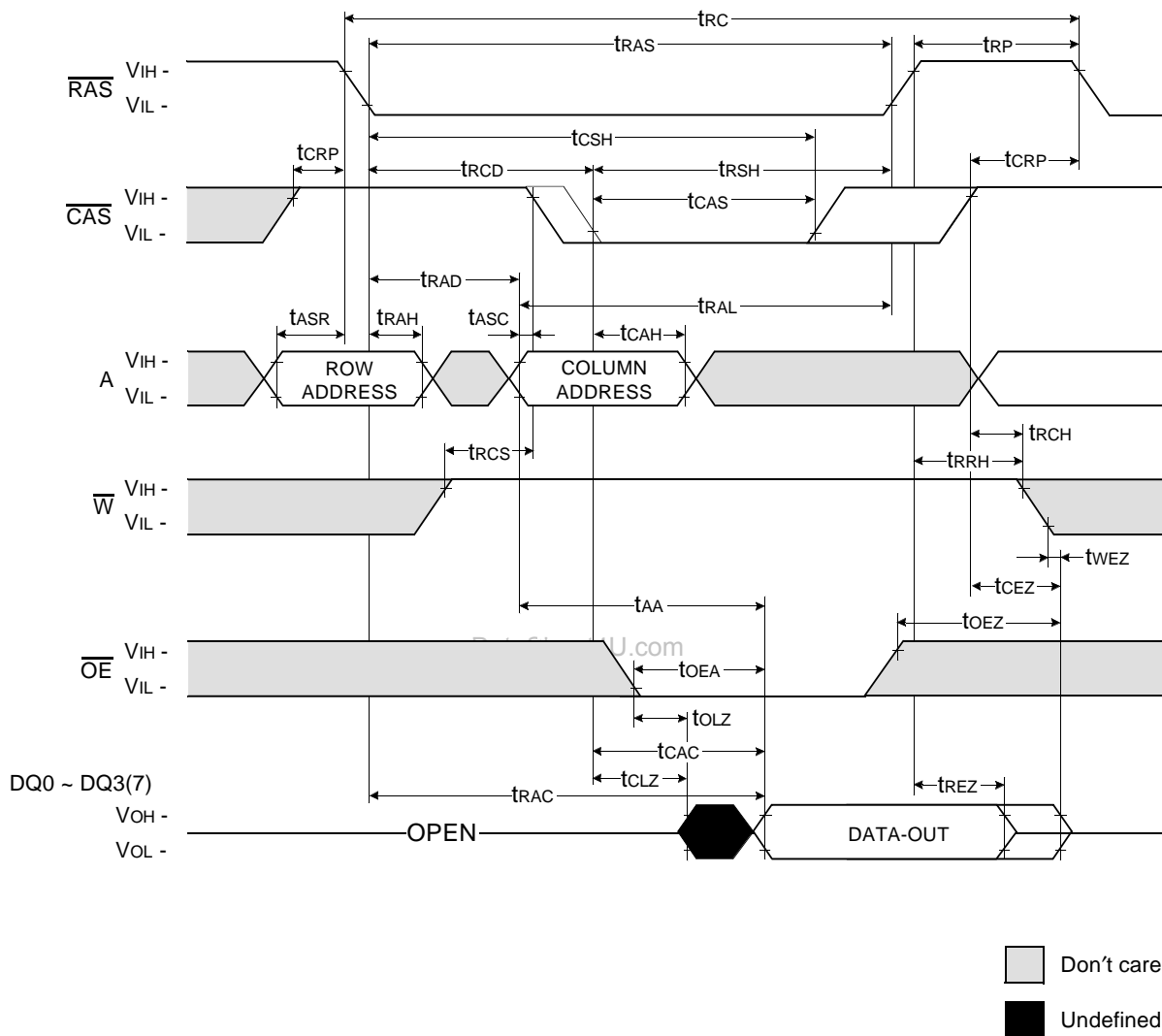
KM48C514D, KM48V514D**CMOS DRAM****NOTES**

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.
Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only.
If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only.
If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. $t_{\text{ASC}} \geq 6\text{ns}$, Assume $t_{\text{T}} = 2.0\text{ns}$
12. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going.
If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
13. If $t_{\text{RASS}} \geq 100\text{us}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
14. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 1024(1K) cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6us interval, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

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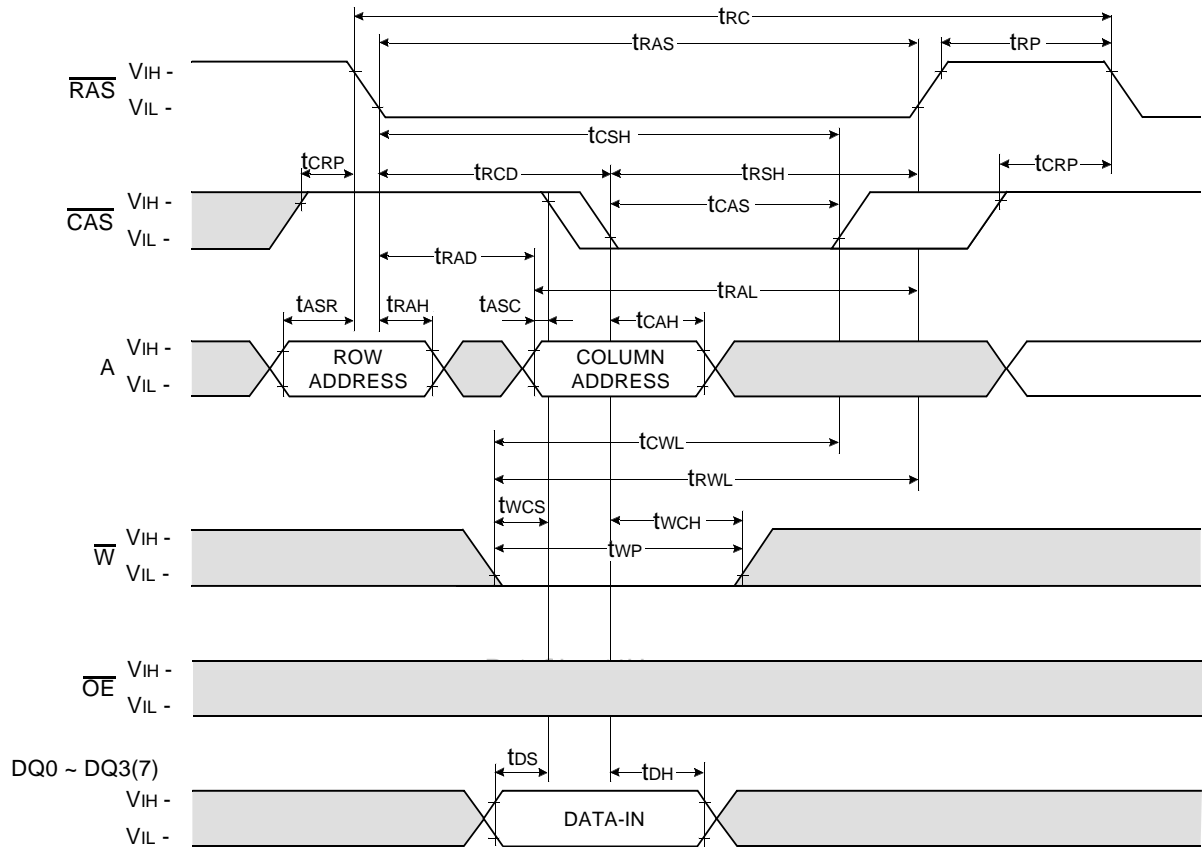
CMOS DRAM

READ CYCLE



KM48C514D, KM48V514D**CMOS DRAM****WRITE CYCLE (EARLY WRITE)**

NOTE : DOUT = OPEN



Don't care
 Undefined



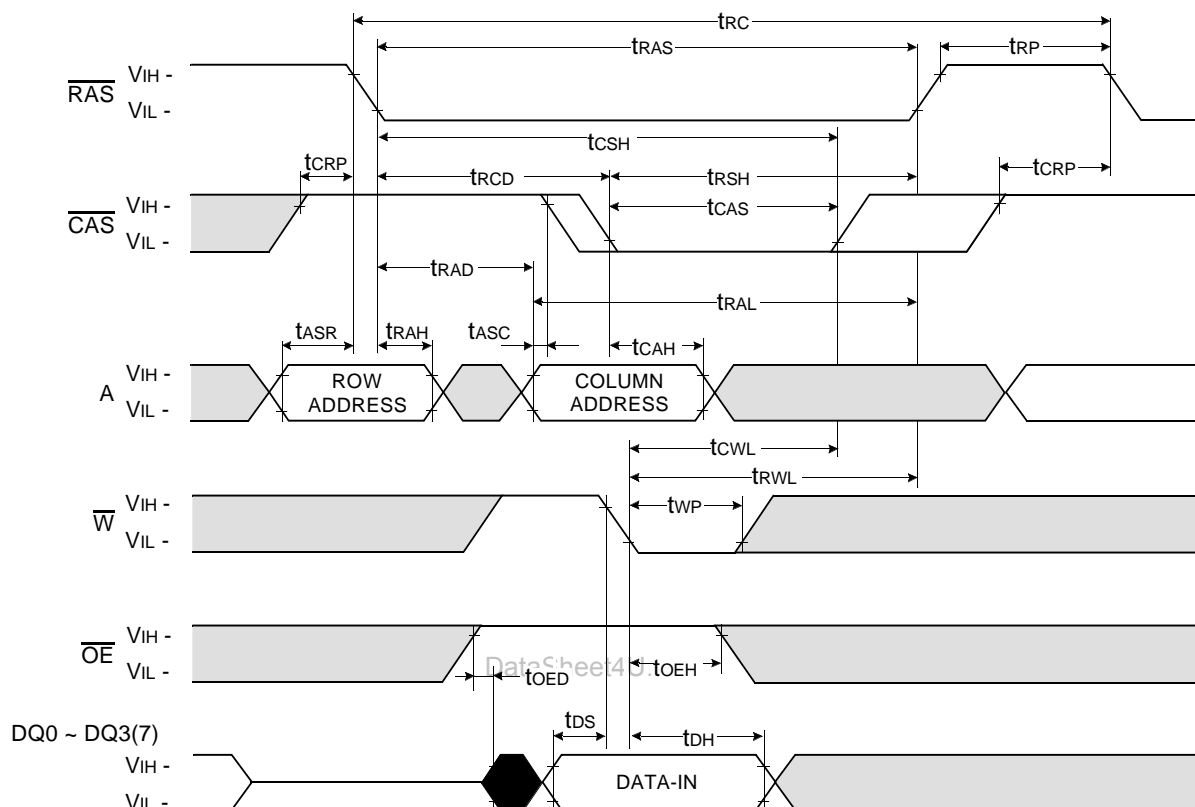
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WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

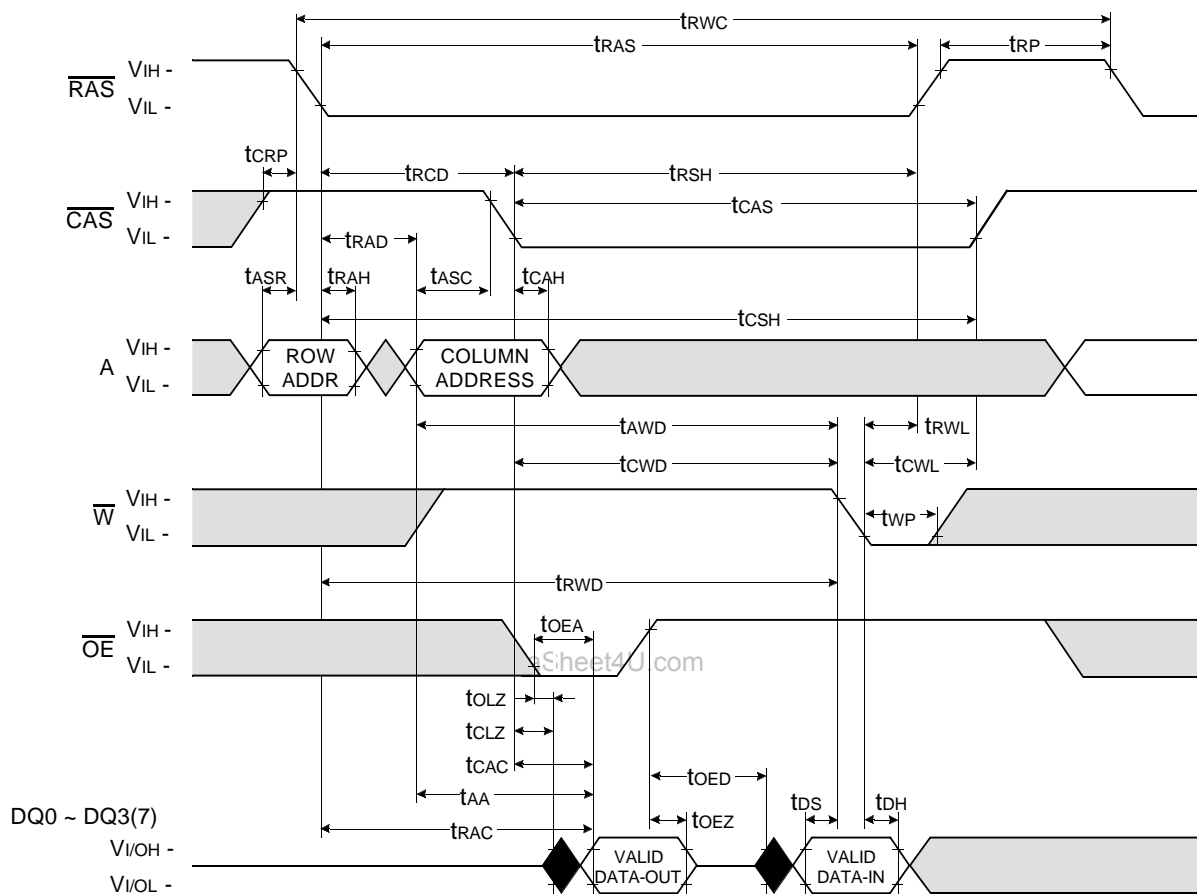


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CMOS DRAM

READ - MODIFY - WRITE CYCLE



Don't care
 Undefined

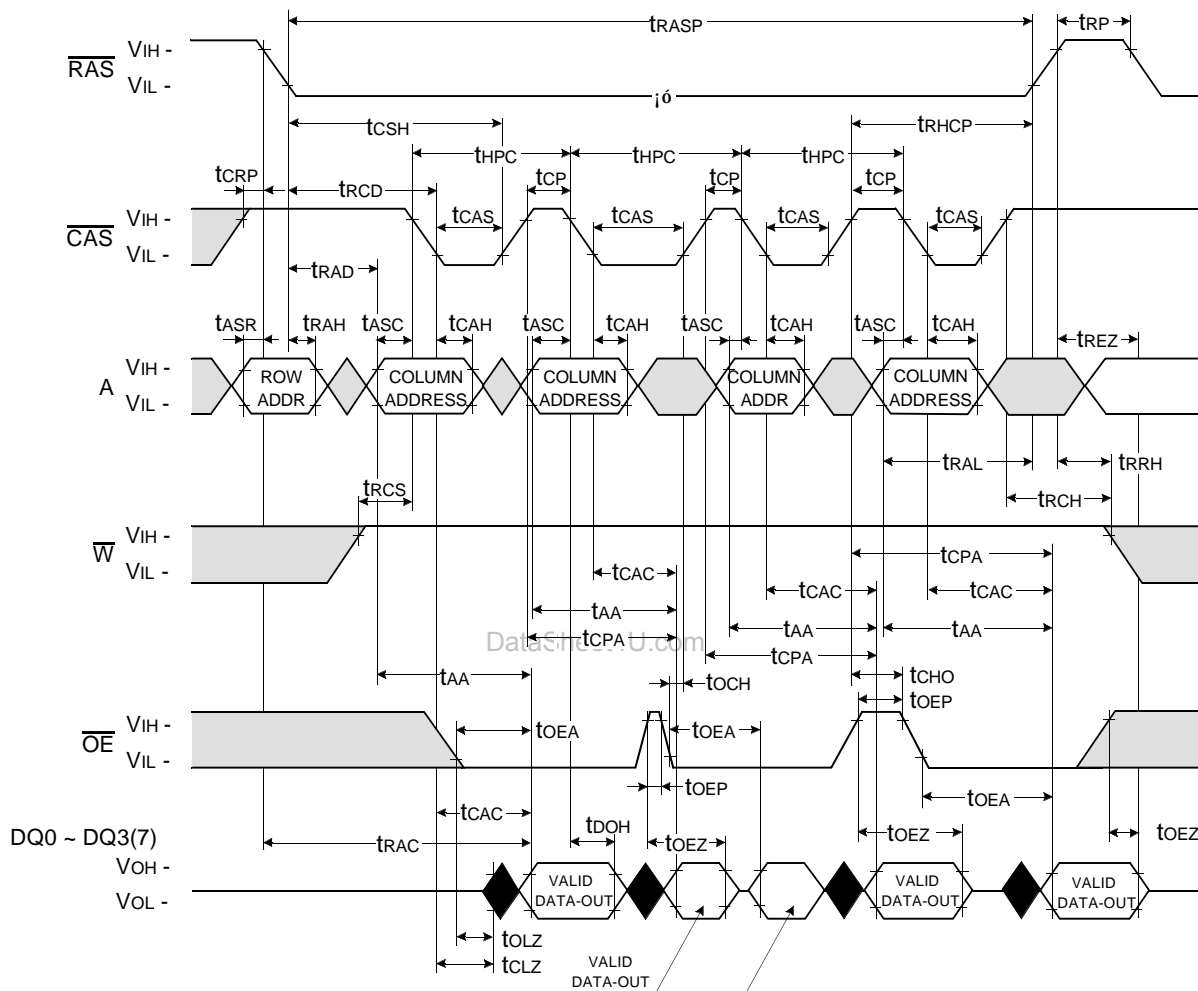


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CMOS DRAM

HYPER PAGE READ CYCLE



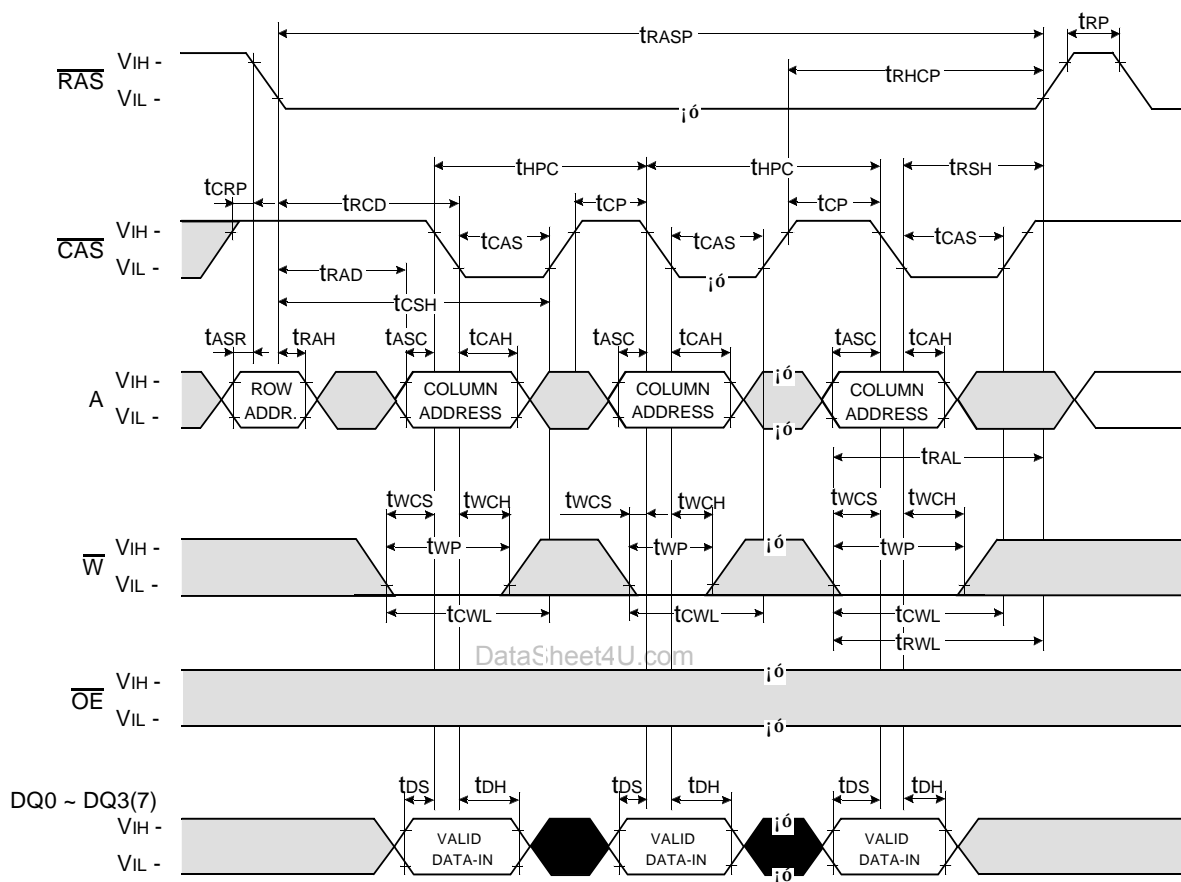
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CMOS DRAM

HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : Dout = OPEN



Don't care
 Undefined

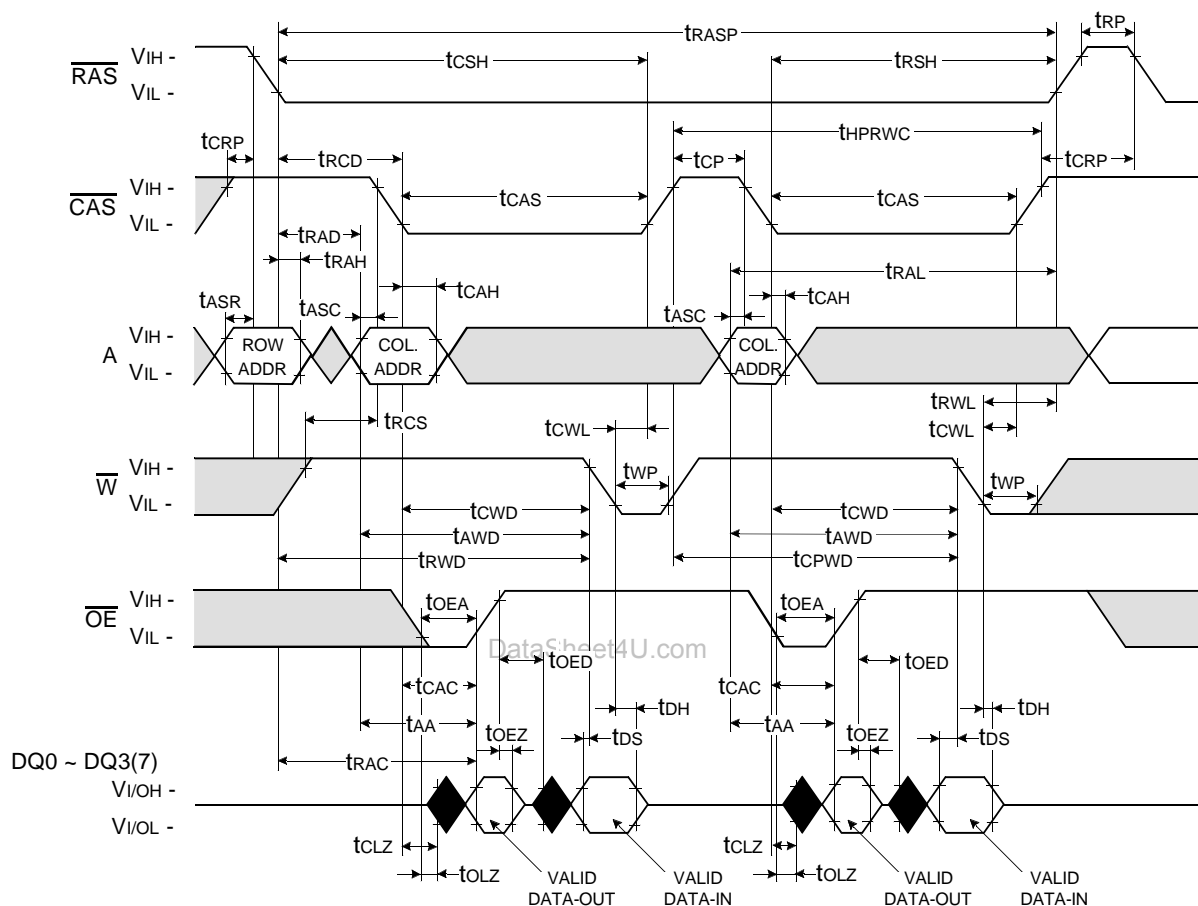


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CMOS DRAM

HYPER PAGE READ-MODIFY-WRITE CYCLE



Don't care
 Undefined

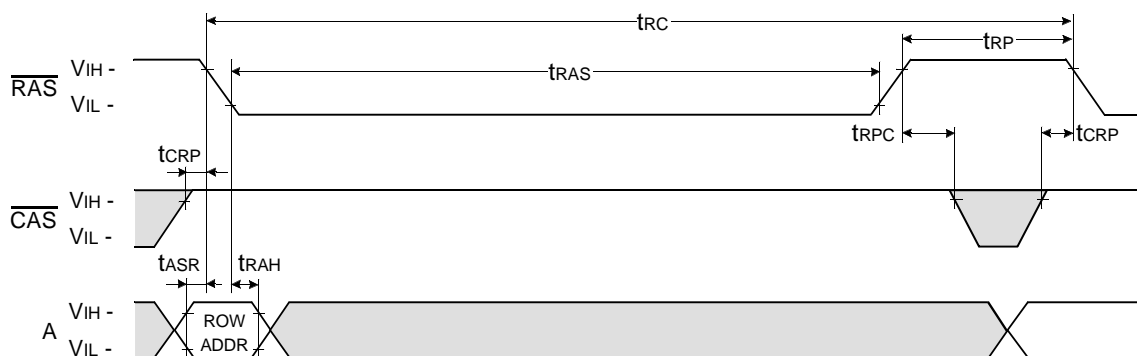
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

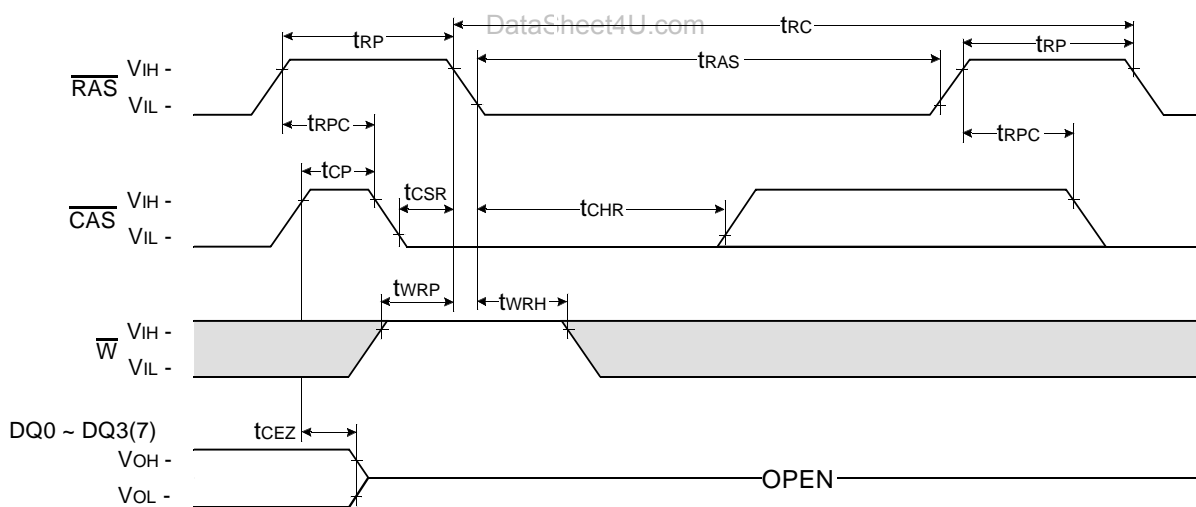
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

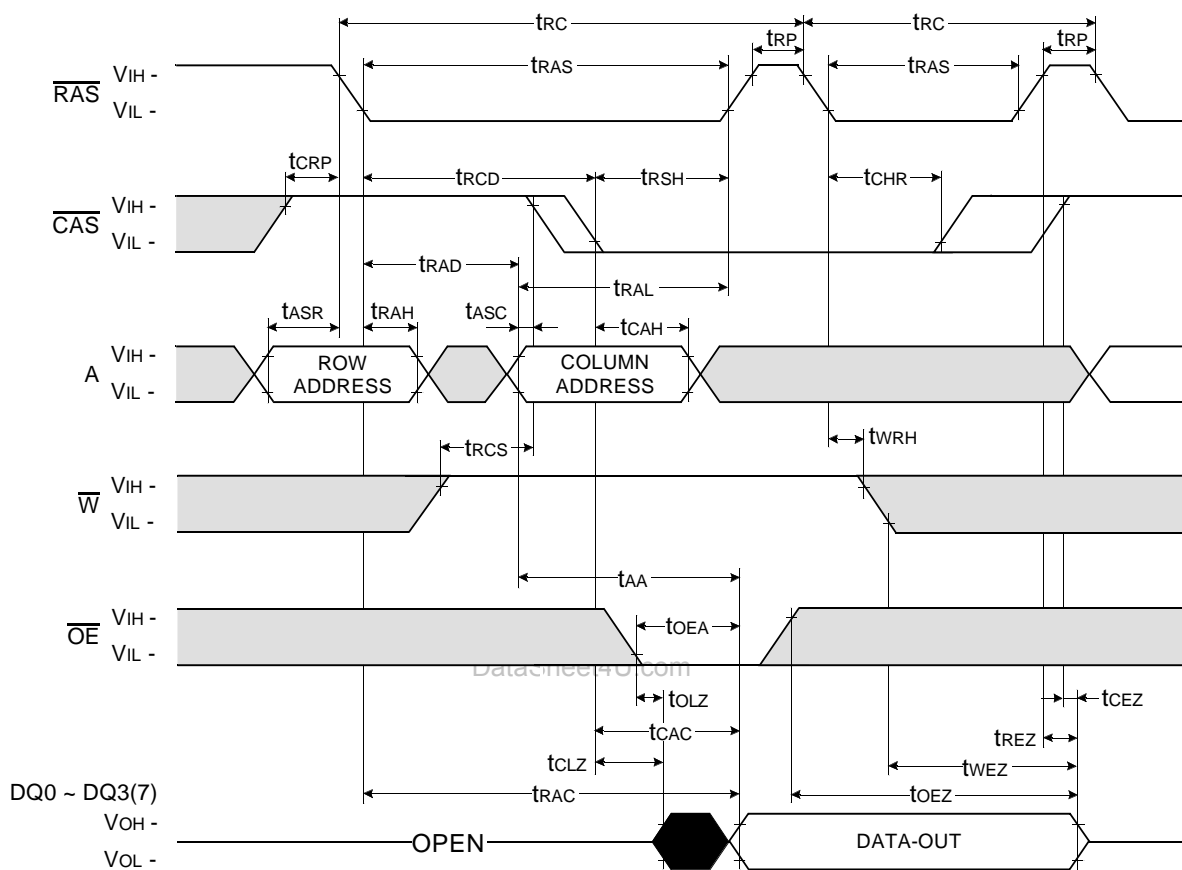


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HIDDEN REFRESH CYCLE (READ)



Don't care
 Undefined



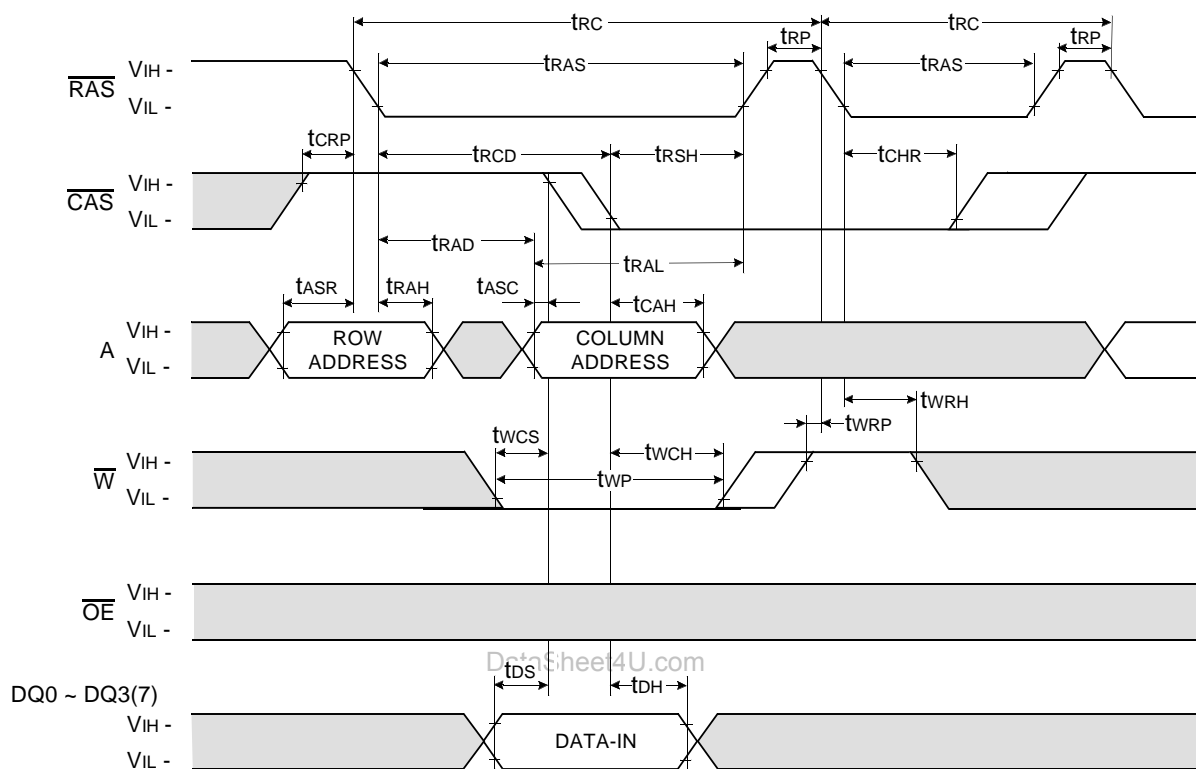
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CMOS DRAM

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

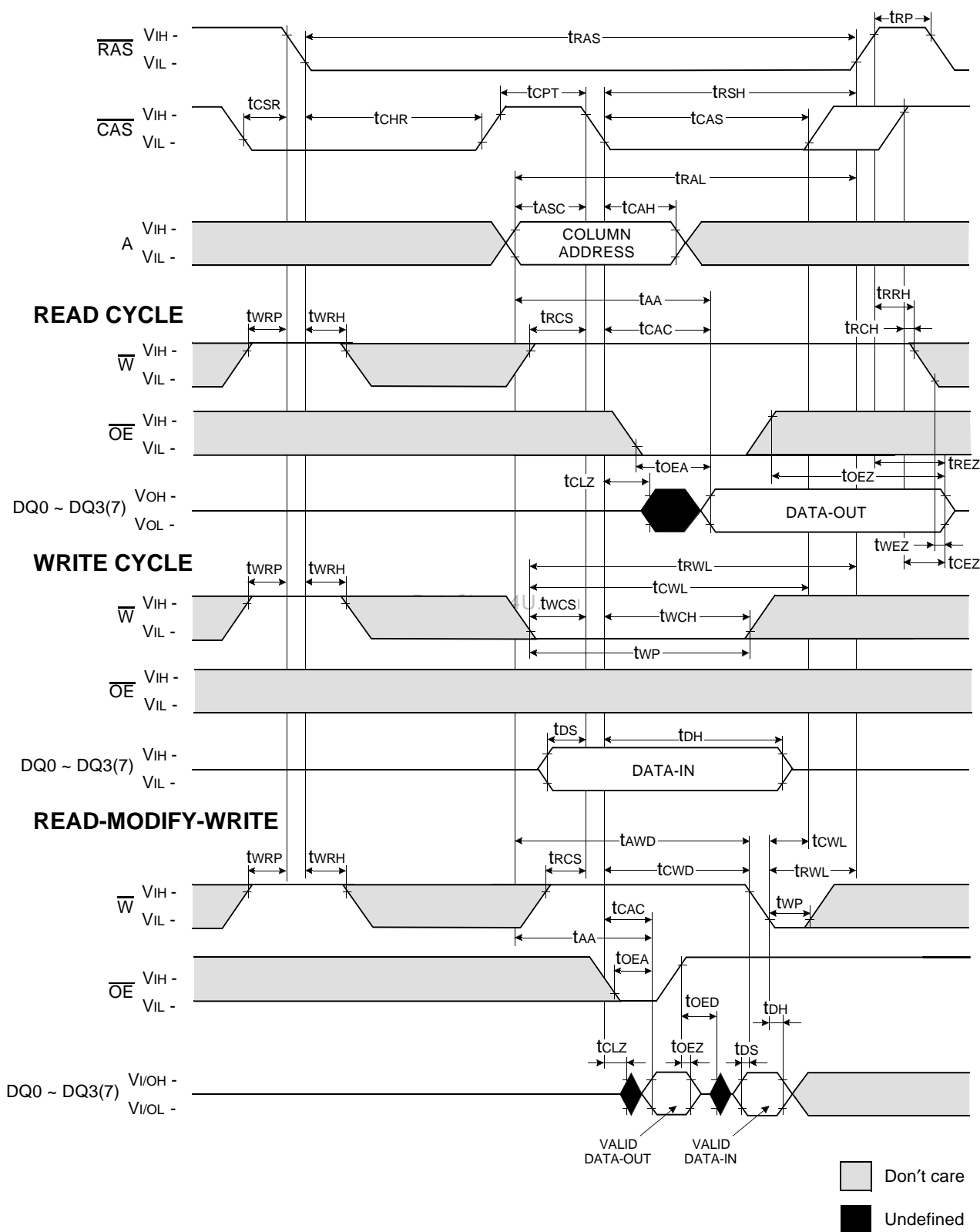


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CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE

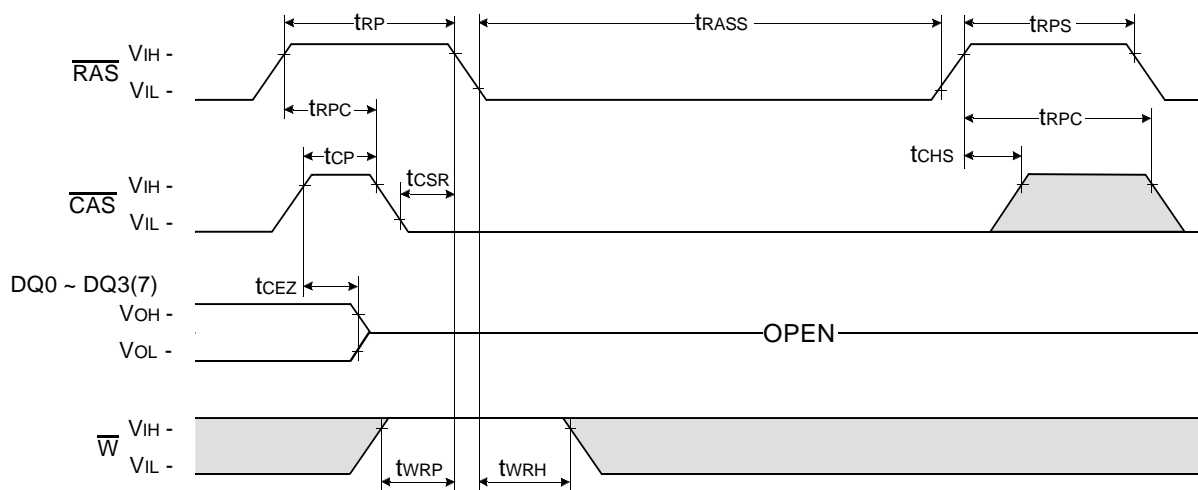


KM48C514D, KM48V514D

CMOS DRAM

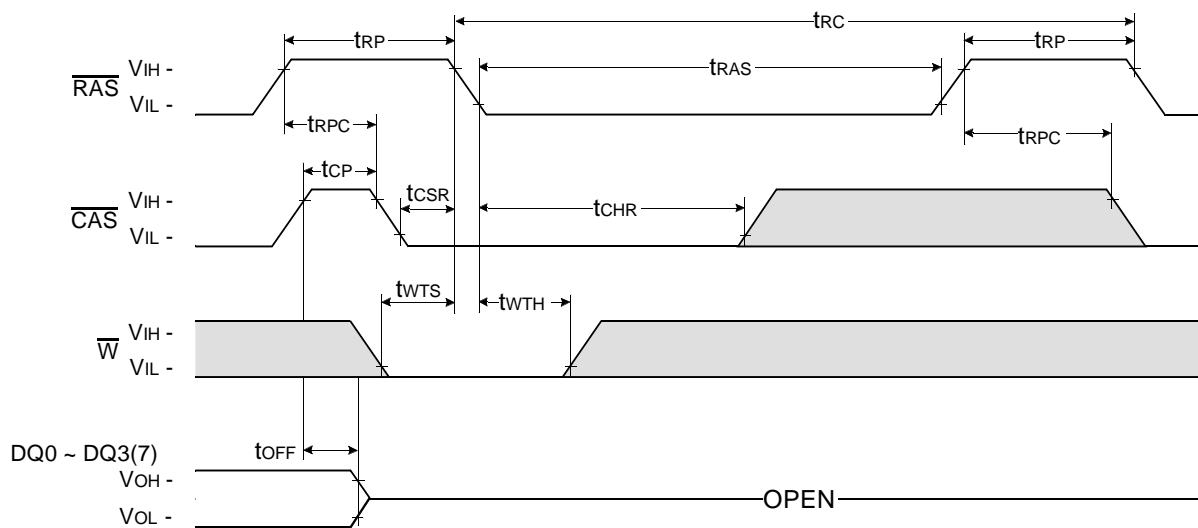
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



Don't care
 Undefined



ELECTRONICS

KM48C514D, KM48V514D

CMOS DRAM

PACKAGE DIMENSION

