ANALOG DEVICES

High Efficiency, Synchronous Step-Down Switching Regulators

ADP1149/1149-3.3/1149-5

FEATURES
Operation to 48 V Input Voltage
Ultrahigh Efficiency (Up to 95%)
Current Mode Operation for Excellent Line and Load
   Transient Response
High Efficiency Maintained Over Wide Current Range
Logic Controlled Micropower Shutdown
Short Circuit Protection
Very Low Dropout Operation
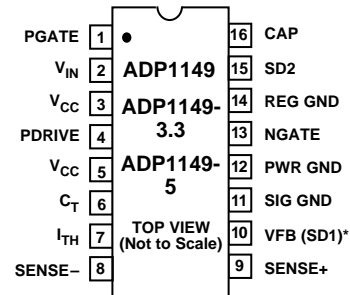Synchronous FET Switching for High Efficiency
Adaptive Nonoverlap Gate Drives

APPLICATIONS
Notebook and Palmtop Computers
Portable Instruments
Battery Operated Digital Devices
Industrial Power Distribution
Avionics Systems
Telecom Power Supplies

PIN CONFIGURATIONS
16-Lead Plastic DIP
16-Lead Plastic SO

PGATE	1	16 CAP
V_{IN}	2	15 SD2
V_{CC}	3	14 REG GND
PDRIVE	4	13 NGATE
V_{CC}	5	12 PWR GND
C_T	6	11 SIG GND
I_{TH}	7	10 VFB (SD1)*
SENSE–	8	9 SENSE+

ADP1149
ADP1149-3.3
ADP1149-5
TOP VIEW
(Not to Scale)

*FIXED OUTPUT VERSIONS = SD1

GENERAL DESCRIPTION
The ADP1149 is a family of synchronous step-down switching regulator controllers featuring automatic-sleep mode to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250 kHz using a constant off-time current-mode architecture.

Special onboard regulation and level-shift circuitry allow operation at input voltages from dropout to 48 V (60 V absolute maximum). The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide

input range converters. Current-mode operation provides excellent line and load transient response. The operating current level is user programmable via an external current sense resistor.

The ADP1149 incorporates automatic power saving sleep mode operation when load currents drop below the level required for continuous operation. In sleep mode, standby power is reduced to only about 8 mW at V_{IN} = 12 V. In shutdown, both MOSFETs are turned off.
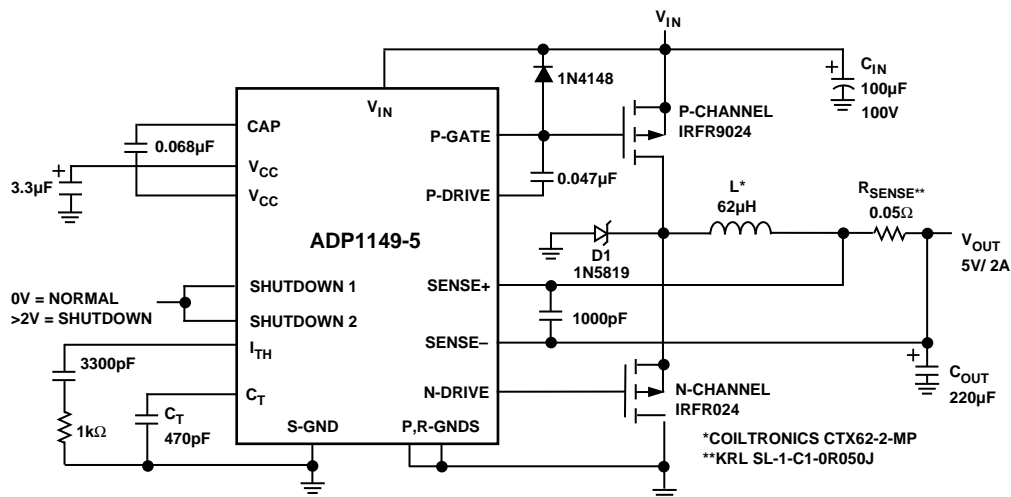

Figure 1. Typical Application

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

(@ T_A = +25°C, V_{IN} = 12 V, V_{10} = 0 V,[1] unless otherwise noted)

Parameter	Symbol	Conditions[2]	Min	Typ	Max	Units
FEEDBACK VOLTAGE						
ADP1149 Only*	V_{10}	V_{IN} = 9 V	1.21	1.25	1.29	V
FEEDBACK CURRENT						
ADP1149 Only*	I_{10}			0.2	1.0	µA
REGULATED OUTPUT VOLTAGE	V_{OUT}	V_{IN} = 9 V				
ADP1149-3.3*		I_{LOAD} = 700 mA	3.23	3.33	3.43	V
ADP1149-5*		I_{LOAD} = 700 mA	4.9	5.05	5.2	V
OUTPUT VOLTAGE LINE REGULATION	dV_{OUT}	V_{IN} = 9 V to 48 V, I_{LOAD} = 700 mA	–40		+40	mV
OUTPUT VOLTAGE LOAD REGULATION	dV_{OUT}					
ADP1149-3.3*		5 mA < I_{LOAD} < 2 A		40	65	mV
ADP1149-5.0*		5 mA < I_{LOAD} < 2 A		60	100	mV
SLEEP MODE OUTPUT RIPPLE*	dV_{OUT}	I_{LOAD} = 0 A		50		mV p-p
INPUT DC SUPPLY CURRENT*[3]	I_Q					
Normal Mode		V_{IN} = 12 V		2	2.8	mA
		V_{IN} = 48 V		2.2	3.0	mA
Sleep Mode		V_{IN} = 12 V		0.6	0.9	mA
		V_{IN} = 48 V		0.8	1.1	mA
Shutdown		V_{IN} = 12 V, V_{15} = 2 V		135	170	µA
		V_{IN} = 48 V, V_{15} = 2 V		300	390	µA
INTERNAL REGULATOR VOLTAGE* (Sets MOSFET Gate Drive Levels)	V_{CC}	V_{IN} = 12 V to 48 V, I_S = 20 mA	9.75	10.25	11	V
V_{CC} DROPOUT VOLTAGE	V_2-V_3	V_{IN} = 5 V, I_3 = 10 mA		200	250	mV
P GATE TO SOURCE VOLTAGE (OFF)	$V_{IN}-V_1$	V_{IN} = 12 V*	–0.2	0		V
		V_{IN} = 48 V*	–0.2	0		V
CURRENT SENSE THRESHOLD VOLTAGE	V_9-V_8					
ADP1149 Only		V_8 = 5 V, V_{10} = 1.32 V (Forced)		25		mV
		V_8 = 5 V, V_{10} = 1.1 V* (Forced)	130	150	170	mV
ADP1149-3.3		V_8 = 3.5 V (Forced)		25		mV
		V_8 = 2.9 V (Forced)*	130	150	170	mV
ADP1149-5.0		V_8 = 5.3 V (Forced)		25		mV
		V_8 = 4.4 V (Forced)*	130	150	170	mV

NOTES

*Denotes specifications that apply over the full operating temperature range.

[1]Pin 10 is a shutdown pin on the ADP1149-3.3 and ADP1149-5 fixed output voltage versions and must be at ground potential for testing.

[2]T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

ADP1149AR, ADP1149AR-3, ADP1149AR-5: $T_J = T_A + (P_D \times 110°C/W)$
ADP1149AN, ADP1149AN-3, ADP1149AN-5: $T_J = T_A + (P_D \times 70°C/W)$

[3]Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) . . . . –15 V to +60 V
V_{CC} Output Current (Pin 3) . . . . 50 mA
V_{CC} Input Voltage (Pin 5) . . . . 20 V
Continuous Output Current (Pins 4, 13) . . . . 50 mA
Sense Voltages (Pins 10, 15) . . . . –0.3 V to V_{CC}
Shutdown Voltages (Pins 10, 15) . . . . 7 V
Operating Temperature Range . . . . 0°C to +70°C
Junction Temperature . . . . +125°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C

ORDERING GUIDE

Model	Output Voltage	Package Description*
ADP1149AN	ADJ	PDIP
ADP1149AR	ADJ	SO-16
ADP1149AN-3.3	3.3 V	PDIP
ADP1149AR-3.3	3.3 V	SO-16
ADP1149AN-5	5 V	PDIP
ADP1149AR-5	5 V	SO-16

*For outline information see Package Information section.

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