



A42L2604 Series

Preliminary

4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE

Document Title

4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	June 13, 2001	Preliminary
0.1	Modify symbol H ₁ dimensions in TSOP 24L package information	July 10, 2001	
0.2	Add -45 grade and modify the AC, DC data Add -U type spec.	November 30, 2001	



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Preliminary

4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE

Features

- Organization: 4,194,304 words X 4 bits
- Part Identification
 - A42L2604 (2K Ref.)
 - A42L2604-L (2K Ref. with self-refresh)
- Single 3.3V power supply/built-in VBB generator
- Low power consumption
 - Operating: 80mA (-45 max)
 - Standby: 1mA (TTL), 1mA (CMOS), 350μA (Self-refresh current)
- High speed
 - 45/50 ns $\overline{\text{RAS}}$ access time
 - 20/22 ns column address access time
 - 12/13 ns $\overline{\text{CAS}}$ access time
 - 18/20 ns EDO Page Mode Cycle Time
- Industrial operating temperature range: -40°C to +85°C for -U
- Fast Page Mode with Extended Data Out
- 2K Refresh Cycle in 32ms
- Read-modify-write, $\overline{\text{RAS}}$ -only, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$, Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
 - 300mil, 24/26-pin SOJ
 - 300mil, 24/26-pin TSOP type II package

General Description

The A42L2604 is a new generation randomly accessed memory for graphics, organized in a 4,194,304-word by 4-bit configuration. This product can execute Write and Read operation via CAS pin.

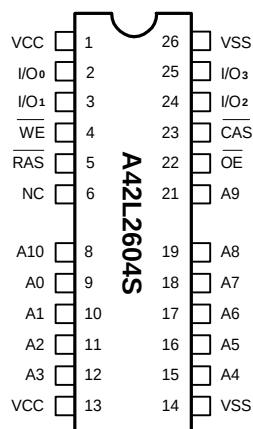
The A42L2604 offers an accelerated Fast Page Mode

cycle with a feature called Extended Data Out (EDO).

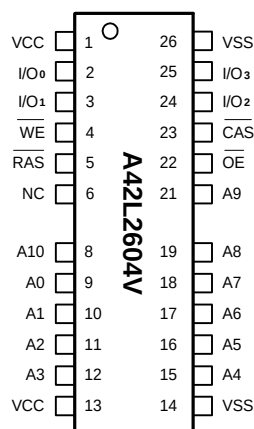
This allow random access of up to 2048(2K Ref.) words within a row at a 56/50 MHz EDO cycle, making the A42L2604 ideally suited for graphics, digital signal processing and high performance computing systems.

Pin Configuration

■ SOJ



■ TSOP



Pin Descriptions

Symbol	Description
A0 – A10	Address Inputs (2K product)
I/O ₀ - I/O ₃	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
VCC	3.3V Power Supply
VSS	Ground
NC	No Connection

Selection Guide

Symbol	Description	-45	-50	Unit
t _{RAC}	Maximum $\overline{\text{RAS}}$ Access Time	45	50	ns
t _{AA}	Maximum Column Address Access Time	20	22	ns
t _{CAC}	Maximum $\overline{\text{CAS}}$ Access Time	12	13	ns
t _{OE}	Maximum Output Enable ($\overline{\text{OE}}$) Access Time	12	13	ns
t _{RC}	Minimum Read or Write Cycle Time	76	84	ns
t _{PC}	Minimum EDO Cycle Time	18	20	ns

Functional Description

The A42L2604 reads and writes data by multiplexing an 22-bit address into a 11-bit(2K) row and column address. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are used to strobe the row address and the column address, respectively.

A Read cycle is performed by holding the $\overline{\text{WE}}$ signal high during $\overline{\text{RAS}}/\overline{\text{CAS}}$ operation. A Write cycle is executed by holding the $\overline{\text{WE}}$ signal low during $\overline{\text{RAS}}/\overline{\text{CAS}}$ operation; the input data is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs later. The data inputs and outputs are routed through 4 common I/O pins, with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and $\overline{\text{OE}}$ controlling the in direction.

EDO Page Mode operation all 2048(2K) columns within a selected row to be randomly accessed at a high data rate. A EDO Page Mode cycle is initiated with a row address latched by $\overline{\text{RAS}}$ followed by a column address latched by $\overline{\text{CAS}}$. While holding $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ can be toggled to strobe changing column addresses, thus achieving shorter cycle times.

The A42L2604 offers an accelerated Fast Page Mode cycle through a feature called Extended Data Out, which keeps the output drivers on during the $\overline{\text{CAS}}$ precharge time (t_{cp}). Since data can be output after $\overline{\text{CAS}}$ goes high, the user is not required to wait for valid data to appear before starting the next access cycle. Data-out will remain

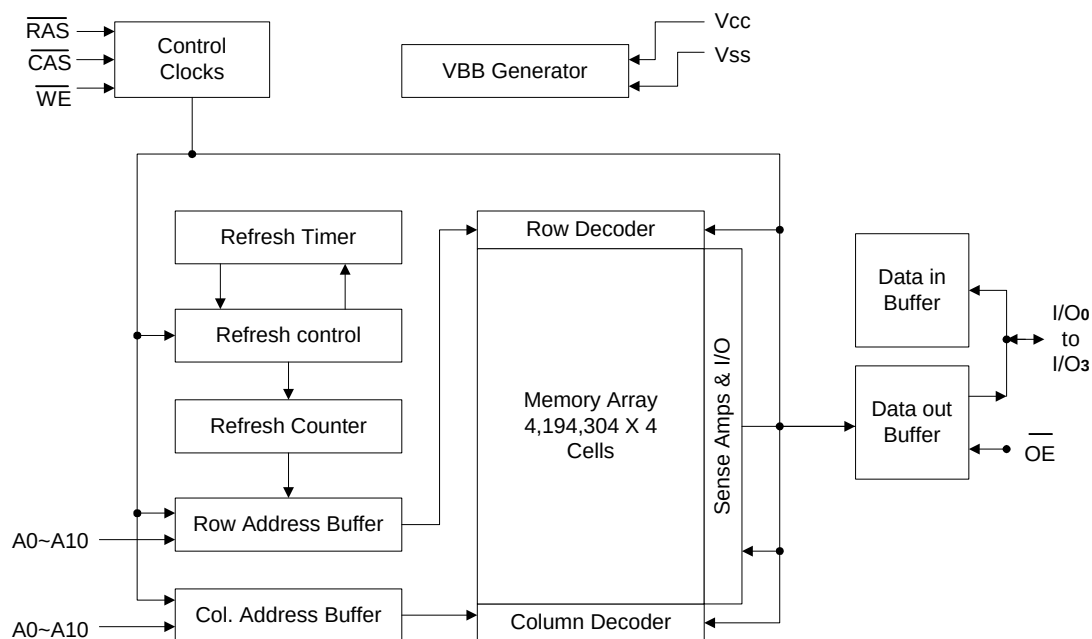
valid as long as $\overline{\text{RAS}}$ and $\overline{\text{OE}}$ are low, and $\overline{\text{WE}}$ is high; this is the only characteristic which differentiates Extended Data Out operation from a standard Read or Fast Page Read.

A memory cycle is terminated by returning both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high. Memory cell data will retain its correct state by maintaining power and accessing all 2048(2K) combinations of the 11-bit(2K) row addresses, regardless of sequence, at least once every 32ms through any $\overline{\text{RAS}}$ cycle (Read, Write) or RAS Refresh cycle ($\overline{\text{RAS}}$ -only, CBR, or Hidden). The CBR Refresh cycle automatically controls the row addresses by invoking the refresh counter and controller.

Power-On

The initial application of the VCC supply requires a 200 μs wait followed by a minimum of any eight initialization cycles containing a $\overline{\text{RAS}}$ clock. During Power-On, the VCC current is dependent on the input levels of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.

It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with VCC or be held at a valid V_{ih} during Power-On to avoid current surges.

Block Diagram

Recommended Operating Conditions ($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -40°C to $+85^\circ\text{C}$)

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.0	3.3	3.6	V
VSS	Input High Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.0	-	VCC + 0.3	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

Truth Table

Function	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Address	I/Os
Standby	H	H	X	X	X	High-Z
Read: Word	L	L	H	L	Row/Col.	Data Out
Read	L	L	H	L	Row/Col.	Data Out
Write: Word (Early)	L	L	L	X	Row/Col.	Data In
Write (Early)	L	L	L	X	Row/Col.	Data In
Read-Write	L	L	H→L	L→H	Row/Col.	Data Out → Data In
EDO-Page-Mode Read: Hi-Z						
-First cycle	L	H→L	H	H→L	Row/Col.	Data Out
-Subsequent Cycles	L	H→L	H	H→L	Col.	Data Out
EDO-Page-Mode Write (Early)						
-First cycle	L	H→L	L	X	Row/Col.	Data In
-Subsequent Cycles	L	H→L	L	X	Col.	Data In
EDO-Page-Mode Read-Write						
-First cycle	L	H→L	H→L	L→H	Row/Col.	Data Out → Data In
-Subsequent Cycles	L	H→L	H→L	L→H	Col.	Data Out → Data In
Hidden Refresh Read	L→H→L	L	H	L	Row/Col.	Data Out
Hidden Refresh Write	L→H→L	L	L	X	Row/Col.	Data In → High-Z
$\overline{\text{RAS}}$ -Only Refresh	L	H	X	X	Row	High-Z
CBR Refresh	H→L	L	X	X	X	High-Z
Self Refresh (L-ver only)	H→L	L	H	X	X	High-Z



Absolute Maximum Ratings*

Input Voltage (Vin) -0.5V to +4.6V
 Output Voltage (Vout) -0.5V to +4.6V
 Power Supply Voltage (VCC) -0.5V to +4.6V
 Operating Temperature (TOPR) 0°C to +70°C
 Storage Temperature (TSTG) -55°C to +150°C
 Soldering Temperature X Time (TSOLDER)
 260°C X 10sec
 Power Dissipation (PD) 1W
 Short Circuit Output Current (Iout) 50mA
 Latch-up Current 200mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 3.3V, VSS = 0V, Ta = 0°C to +70°C or -40°C to +85°C)

Symbol	Parameter	-45		-50		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.			
IIL	Input Leakage Current	-5	+5	-5	+5	μA	0V ≤ Vin ≤ Vin + 0.3V Pins not under Test = 0V	
IoL	Output Leakage Current	-5	+5	-5	+5	μA	DOOUT disabled, 0V ≤ Vout ≤ + VCC	
Icc1	Operating Power Supply Current	-	80	-	75	mA	RAS, UCAS, LCAS and Address cycling; trc = min.	1, 2
Icc2	TTL Standby Power Supply Current	-	1	-	1	mA	RAS = UCAS = LCAS = VIH	
Icc3	Average Power Supply Current, RAS Refresh Mode	-	80	-	75	mA	RAS and Address cycling, UCAS = LCAS = VIH, trc = min.	1
Icc4	EDO Page Mode Average Power Supply Current	-	40	-	35	mA	RAS = VIL, UCAS, LCAS and Address cycling; tpc = min.	1, 2
Icc5	CAS -before- RAS Refresh Power Supply Current	-	75	-	70	mA	RAS, UCAS and LCAS cycling; trc = min.	1
Icc6	CMOS Standby Power Supply Current	-	1	-	1	mA	RAS = UCAS = LCAS = VCC - 0.2V	
Icc7	Self Refresh Mode Current	-	350	-	350	μA	RAS = CAS ≤ VSS + 0.2V All other input high levels are VCC - 0.2V or input low levels are VSS + 0.2V	
VOH	Output Voltage	2.4	-	2.4	-	V	Iout = -2.0mA	
VOL		-	0.4	-	0.4	V	Iout = 2.0mA	

AC Characteristics ($V_{CC} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$ or $-40^\circ C$ to $+85^\circ C$)

Test Conditions:

Input timing reference level: $V_{IH}/V_{IL}=2.0V/0.8V$

Output reference level: $V_{OH}/V_{OL}=2.0V/0.8V$

Output Load: 2TTL gate + CL (50pF)

Assumed $t_r=2ns$

#	Std Symbol	Parameter	-45		-50		Unit	Notes
			Min.	Max.	Min.	Max.		
	t_r	Transition Time (Rise or Fall)	1	50	1	50	ns	4, 5
1	t_{RC}	Random Read or Write Cycle Time	76	-	84	-	ns	
2	t_{RP}	$\overline{RAS}$ Precharge Time	27	-	30	-	ns	
3	t_{RAS}	$\overline{RAS}$ Pulse Width	45	10K	50	10K	ns	
4	t_{CAS}	$\overline{CAS}$ Pulse Width	7	10K	8	10K	ns	
5	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	33	11	37	ns	6
6	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	8	25	9	28	ns	7
7	t_{RSH}	$\overline{CAS}$ to $\overline{RAS}$ Hold Time	7	-	8	-	ns	
8	t_{CSH}	$\overline{CAS}$ Hold Time	35	-	37	-	ns	
9	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
10	t_{ASR}	Row Address Setup Time	0	-	0	-	ns	
11	t_{RAH}	Row Address Hold Time	7	-	8	-	ns	
12	t_{CLZ}	$\overline{CAS}$ to Output in Low Z	3	-	3	-	ns	8
13	t_{RAC}	Access Time from $\overline{RAS}$	-	45	-	50	ns	6,7
14	t_{CAC}	Access Time from $\overline{CAS}$	-	12	-	13	ns	6, 12
15	t_{AA}	Access Time from Column Address	-	20	-	22	ns	7, 12
16	t_{OEA}	Access Time from $\overline{OE}$	-	12	-	13	ns	
17	t_{AR}	Column Address Hold Time from $\overline{RAS}$	40	-	45	-	ns	
18	t_{RCS}	Read Command Setup Time	0	-	0	-	ns	
19	t_{RCH}	Read Command Hold Time	0	-	0	-	ns	9

AC Characteristics (continued) ($V_{CC} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$ or $-40^\circ C$ to $+85^\circ C$)

Test Conditions:

Input timing reference level: $V_{IH}/V_{IL}=2.0V/0.8V$

Output reference level: $V_{OH}/V_{OL}=2.0V/0.8V$

Output Load: 2TTL gate + CL (50pF)

Assumed $t_r=2ns$

#	Std Symbol	Parameter	-45		-50		Unit	Notes
			Min.	Max.	Min.	Max.		
20	t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	0	-	0	-	ns	9
21	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	-	22	-	ns	
22	t_{COH}	Output Hold After $\overline{CAS}$ Low	-	2	-	3	ns	
23	t_{OFF}	Output Buffer Turn-Off Delay Time	-	2	-	3	ns	8, 10
24	t_{ASC}	Column Address Setup Time	0	-	0	-	ns	
25	t_{CAH}	Column Address Hold Time	7	-	8	-	ns	
26	t_{OES}	$\overline{OE}$ Low to $\overline{CAS}$ High Set Up	10	-	10	-	ns	
27	t_{WCS}	Write Command Setup Time	0	-	0	-	ns	11
28	t_{WCH}	Write Command Hold Time	7	-	8	-	ns	11
29	t_{WCR}	Write Command Hold Time to $\overline{RAS}$	40	-	45	-	ns	
30	t_{WP}	Write Command Pulse Width	7	-	8	-	ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12	-	13	-	ns	
32	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	-	8	-	ns	
33	t_{DS}	Data-in setup Time	0	-	0	-	ns	
34	t_{DH}	Data-in Hold Time	7	-	8	-	ns	
35	t_{DHR}	Data-in Hold Time to $\overline{RAS}$	40	-	45	-	ns	
36	t_{RWC}	Read-Modify-Write Cycle Time	104	-	114	-	ns	
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	59	-	65	-	ns	11
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	26	-	28	-	ns	11
39	t_{AWD}	Column Address to $\overline{WE}$ Delay Time (Read-Modify-Write)	34	-	37	-	ns	11

AC Characteristics (continued) ($V_{CC} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$ or $-40^\circ C$ to $+85^\circ C$)

Test Conditions:

Input timing reference level: $V_{IH}/V_{IL}=2.0V/0.8V$

Output reference level: $V_{OH}/V_{OL}=2.0V/0.8V$

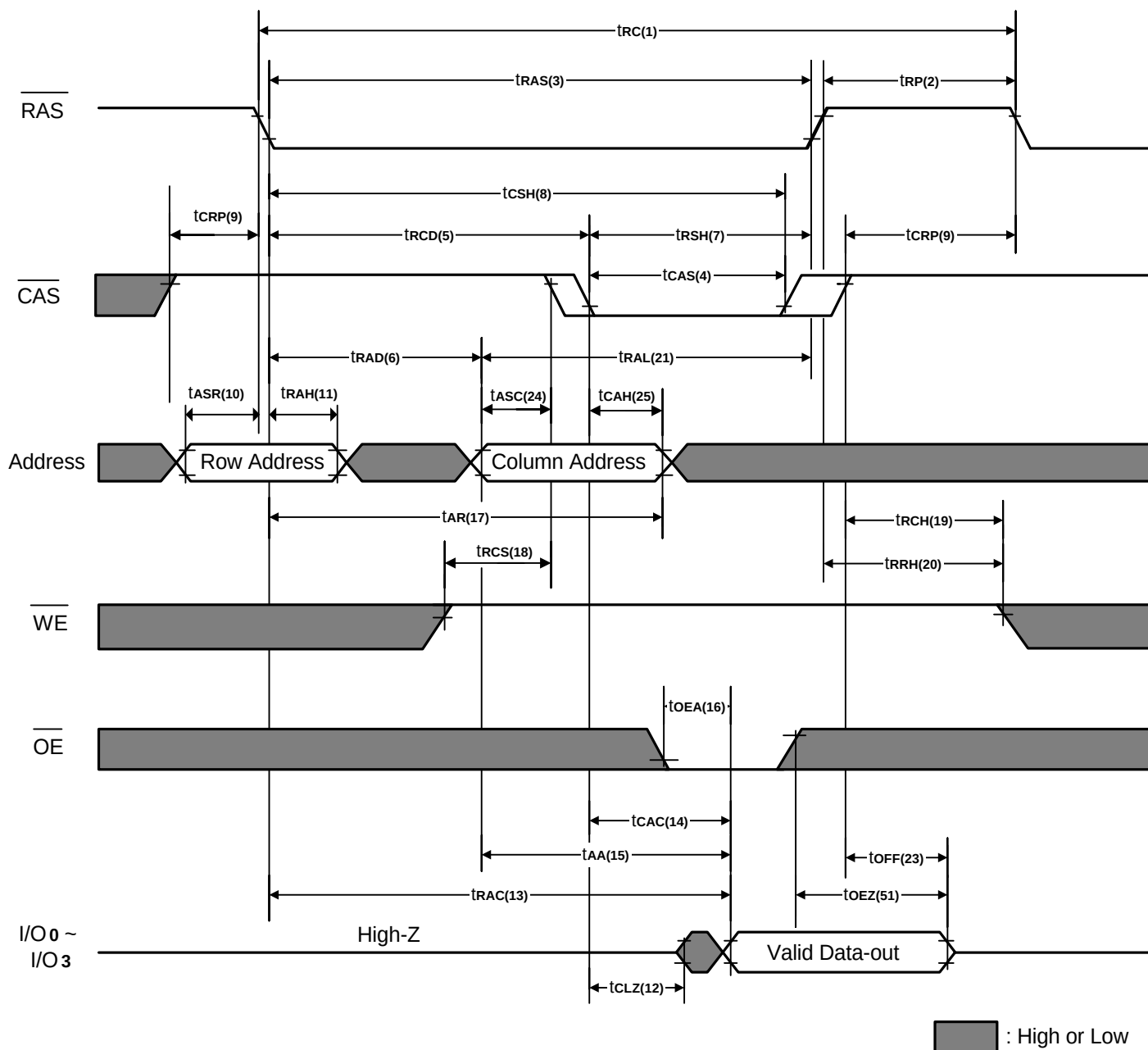
Output Load: 2TTL gate + CL (50pF)

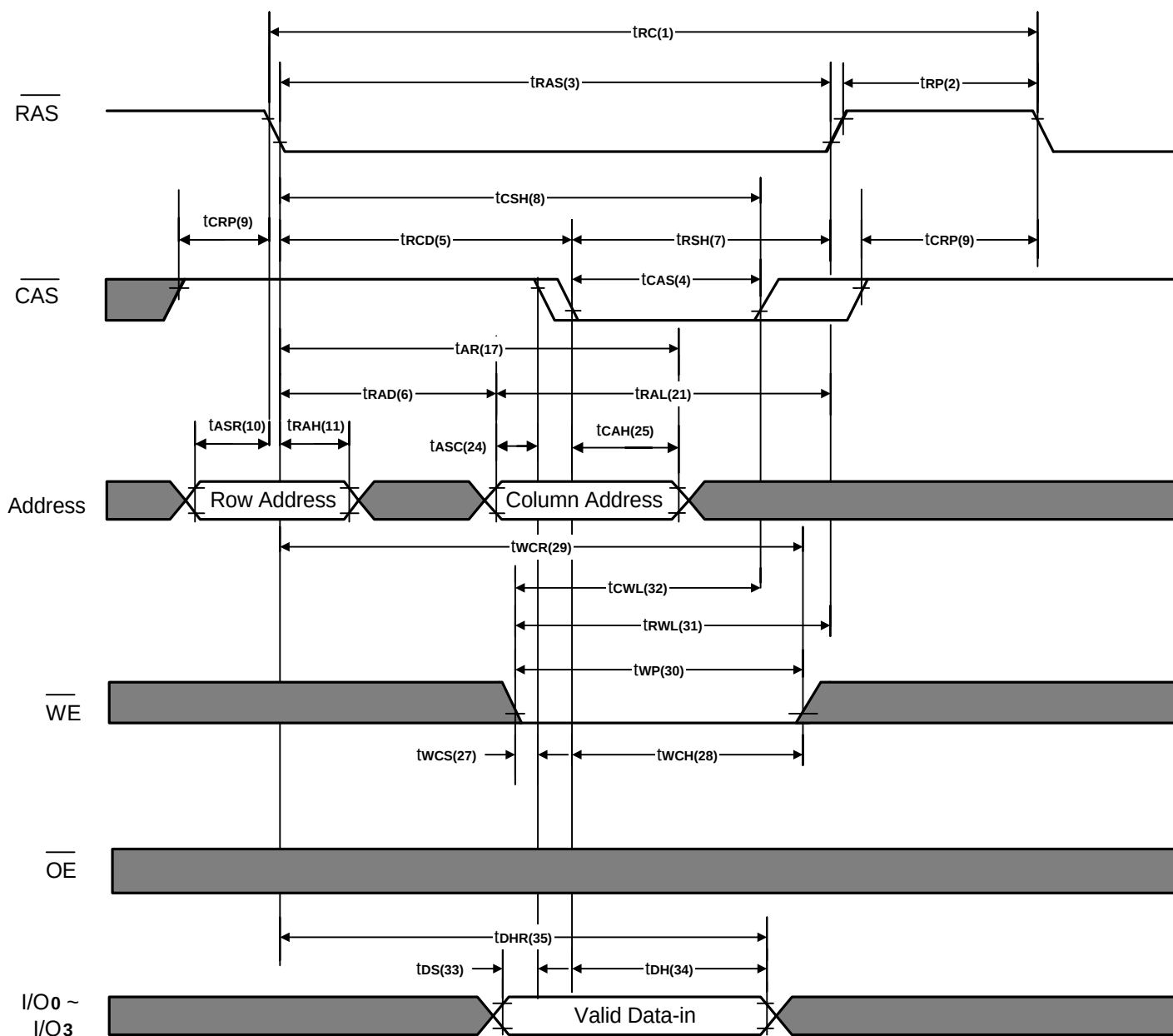
Assumed $t_r=2ns$

#	Std Symbol	Parameter	-45		-50		Unit	Notes
			Min.	Max.	Min.	Max.		
40	toEH	$\overline{OE}$ Hold Time from $\overline{WE}$	7	-	8	-	ns	
41	toEP	$\overline{OE}$ High Pulse Width	5	-	5	-	ns	
42	tPC	Read or Write Cycle Time (EDO Page)	18	-	20	-	ns	13
43	tCPA	Access Time from $\overline{CAS}$ Precharge (EDO Page)	-	21	-	23	ns	12
44	tCP	$\overline{CAS}$ Precharge Time	7	-	8	-	ns	
45	tPCM	EDO Page Mode RMW Cycle Time	46	-	50	-	ns	
46	tCRW	EDO Page Mode $\overline{CAS}$ Pulse Width (RMW)	35	-	38	-	ns	
47	tRASP	$\overline{RAS}$ Pulse Width (EDO Page)	45	200K	50	200K	ns	
48	tCSR	$\overline{CAS}$ Setup Time ($\overline{CAS}$ -before- $\overline{RAS}$)	5	-	5	-	ns	3
49	tCHR	$\overline{CAS}$ Hold Time ($\overline{CAS}$ -before- $\overline{RAS}$)	10	-	10	-	ns	3
50	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10	-	10	-	ns	
51	toEZ	Output Buffer Turn-off Delay from $\overline{OE}$	-	2	-	3	ns	8
52	tRASS	$\overline{RAS}$ pulse width ($\overline{C}$ -B- $\overline{R}$ self refresh)	100	-	100	-	μs	
53	tRPS	$\overline{RAS}$ precharge time ($\overline{C}$ -B- $\overline{R}$ self refresh)	76	-	84	-	ns	
54	tCHS	$\overline{CAS}$ hold time ($\overline{C}$ -B- $\overline{R}$ self refresh)	-50	-	-50	-	ns	

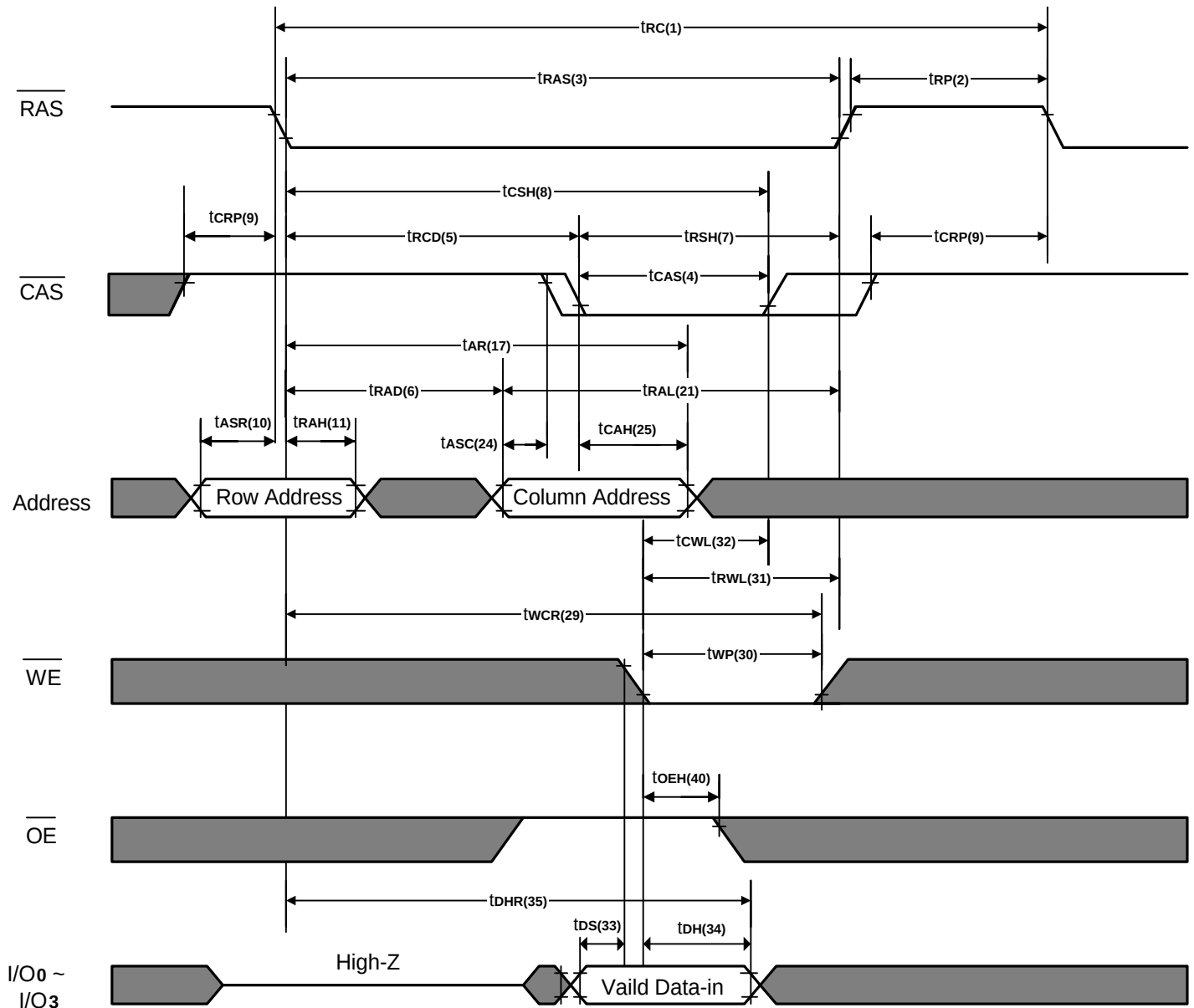
Notes:

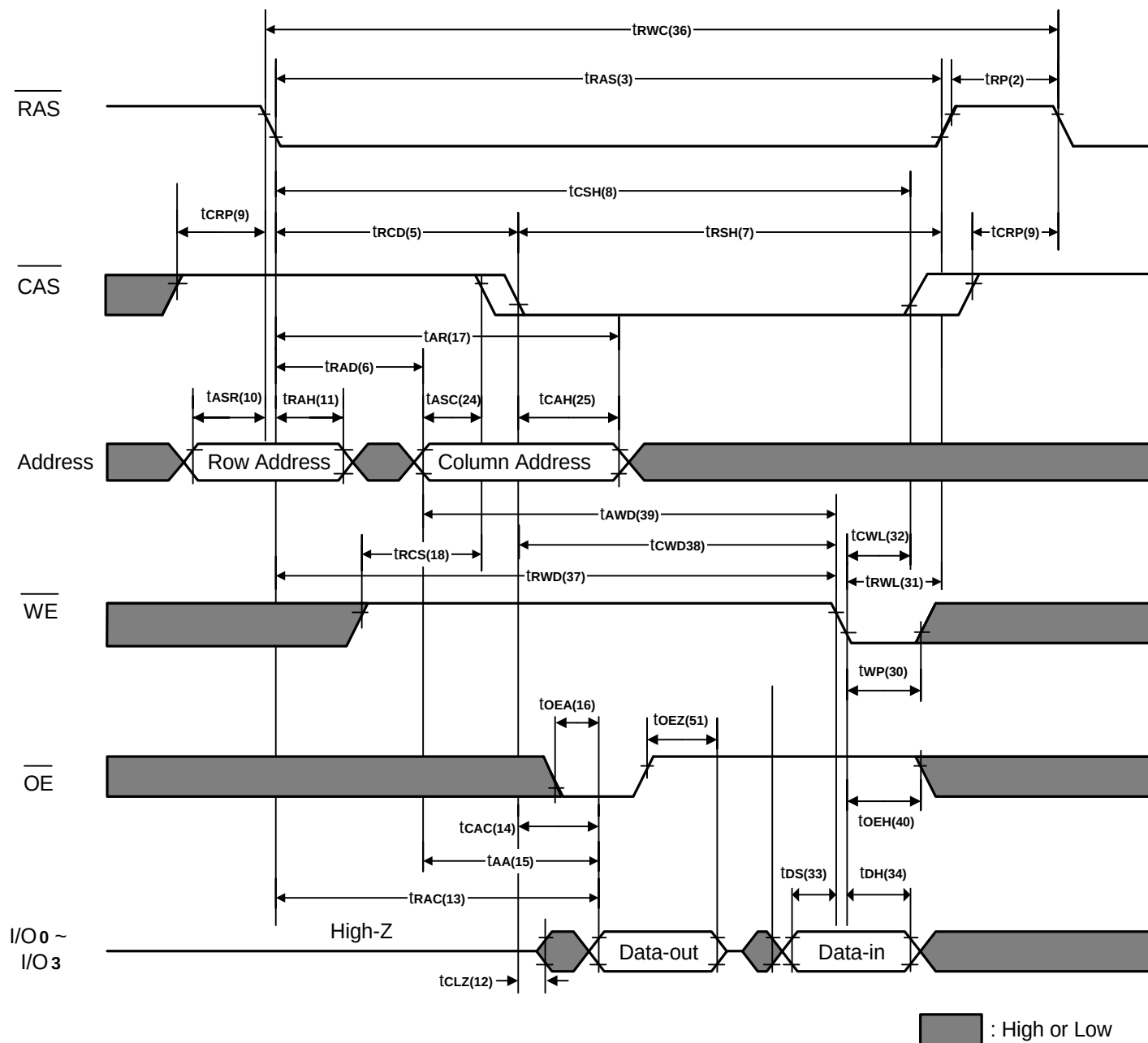
1. I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
3. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$ -before- $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks.
4. AC Characteristics assume $t_r = 2$ ns. All AC parameters are measured with a load equivalent to two TTL loads and 50pF, $V_{IL}(\text{min.}) \geq \text{GND}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
5. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
6. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled exclusively by t_{CAC} .
7. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled exclusively by t_{AA} .
8. Assumes three state test load (5pF and a 500 Ω Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
11. t_{WCS} , t_{WCH} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$ and $t_{WCH} \geq t_{WCH}(\text{min.})$, the cycle is an early write cycle and data-out pins will remain open circuit, high impedance, throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA} .
13. $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.

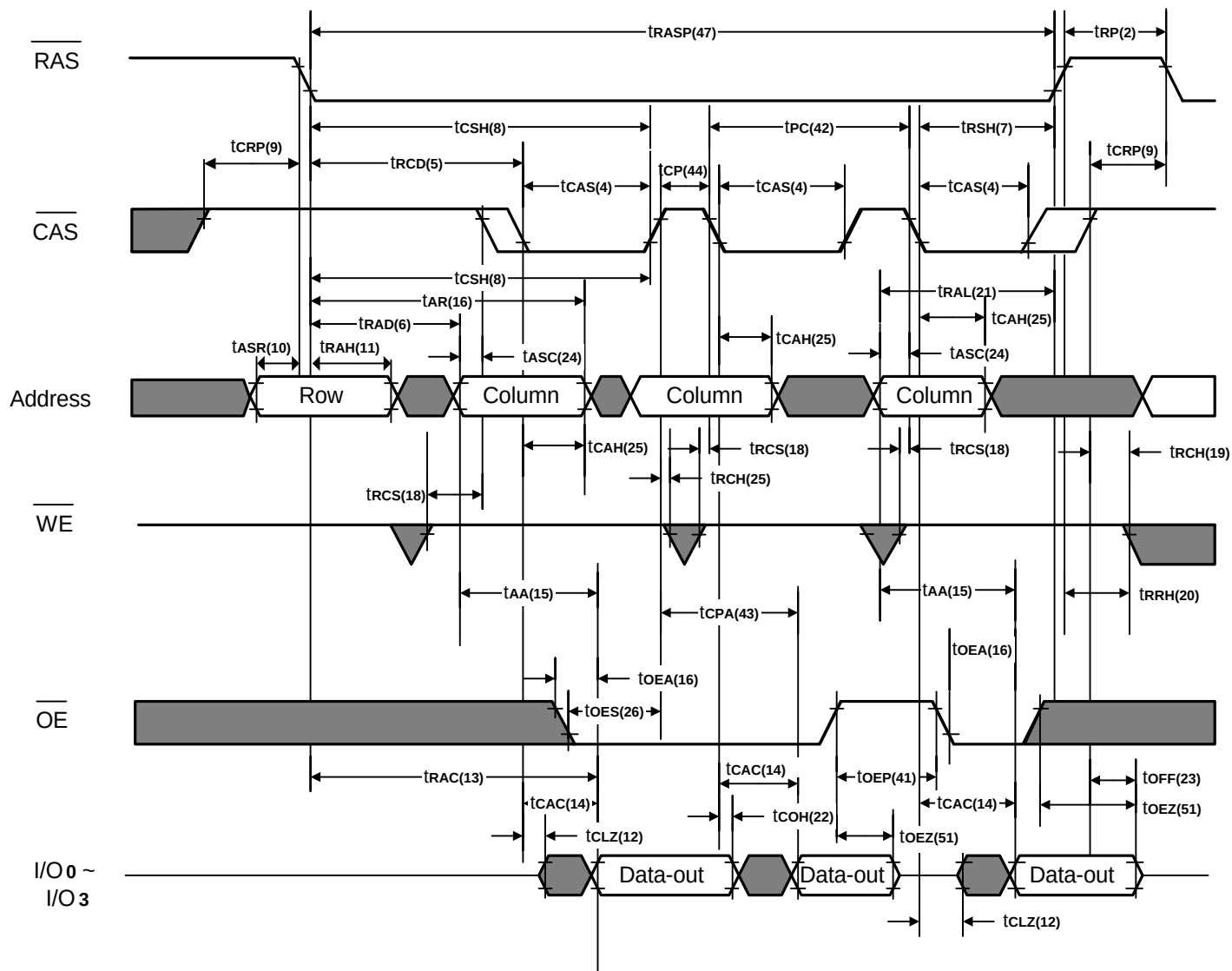
Word Read Cycle


Word Write Cycle (Early Write)


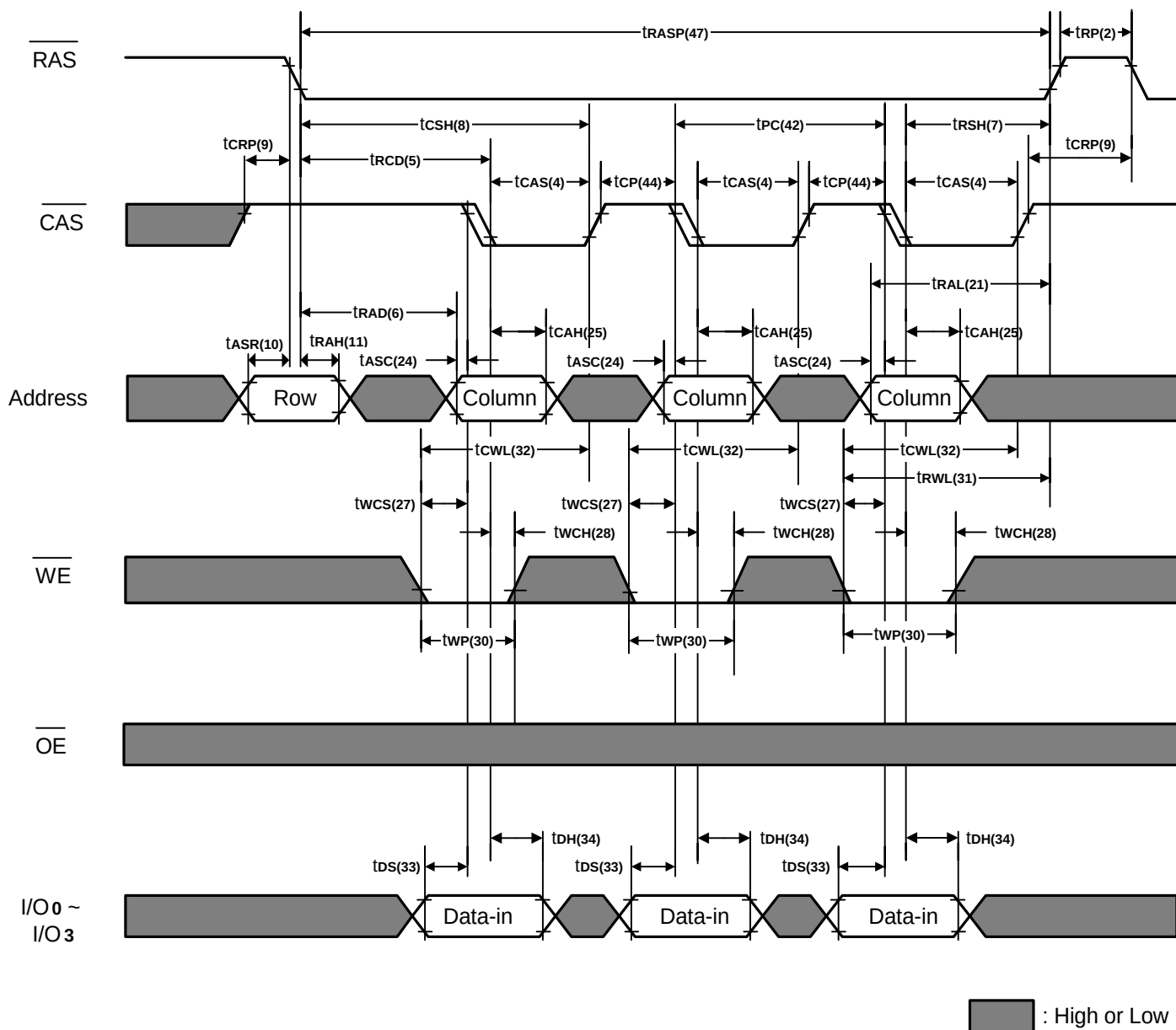
 : High or Low

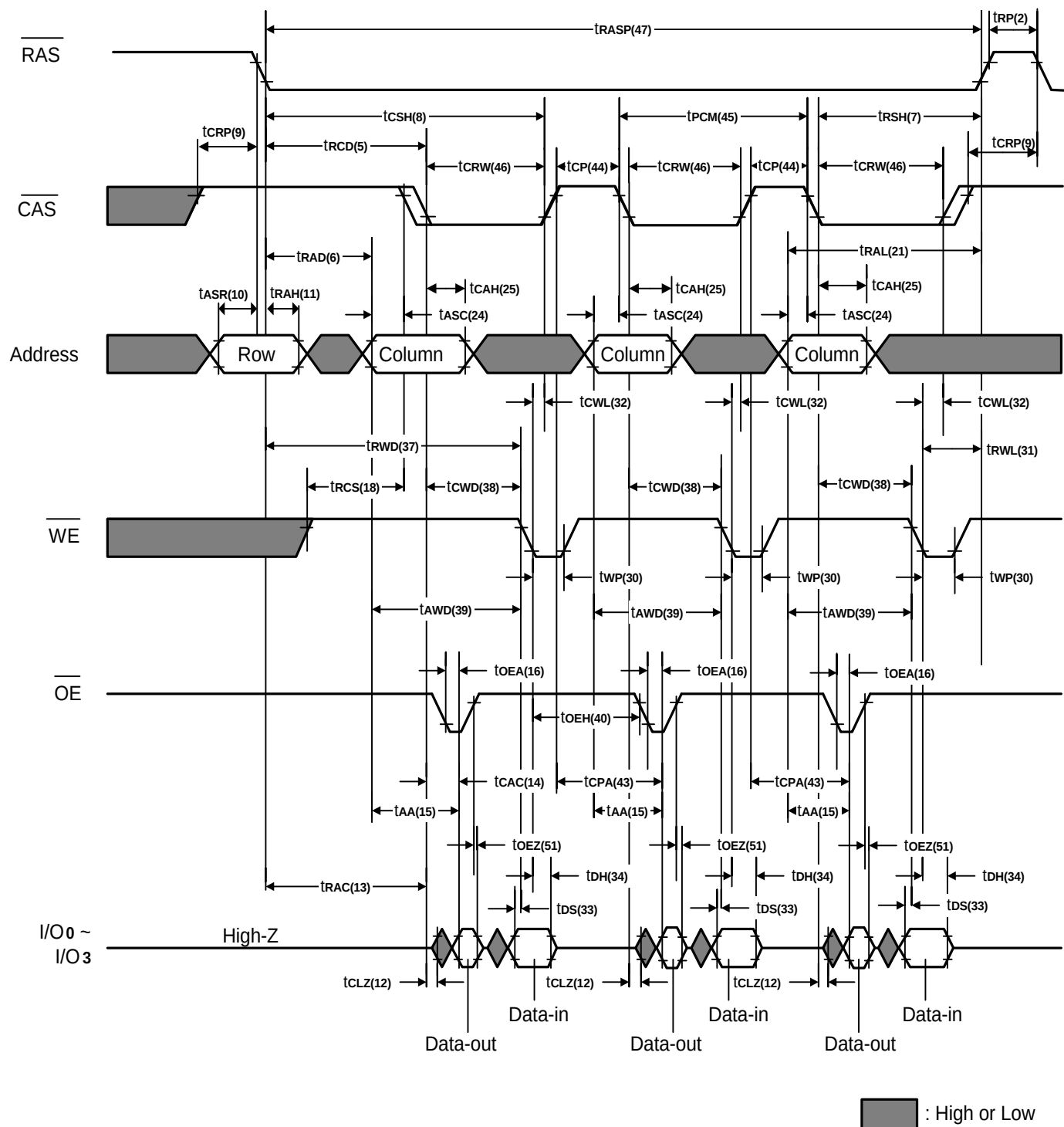
Word Write Cycle (Late Write)


Word Read-Modify-Write Cycle


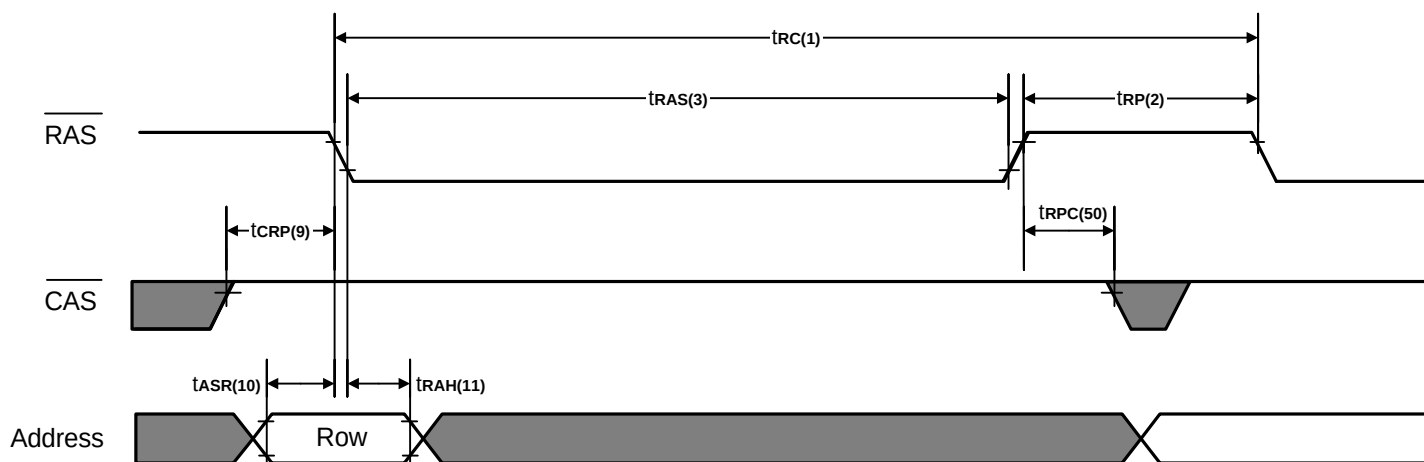
EDO Page Mode Word Read Cycle


■ : High or Low

EDO Page Mode Early Word Write Cycle


EDO Page Mode Word Read-Modify-Write Cycle


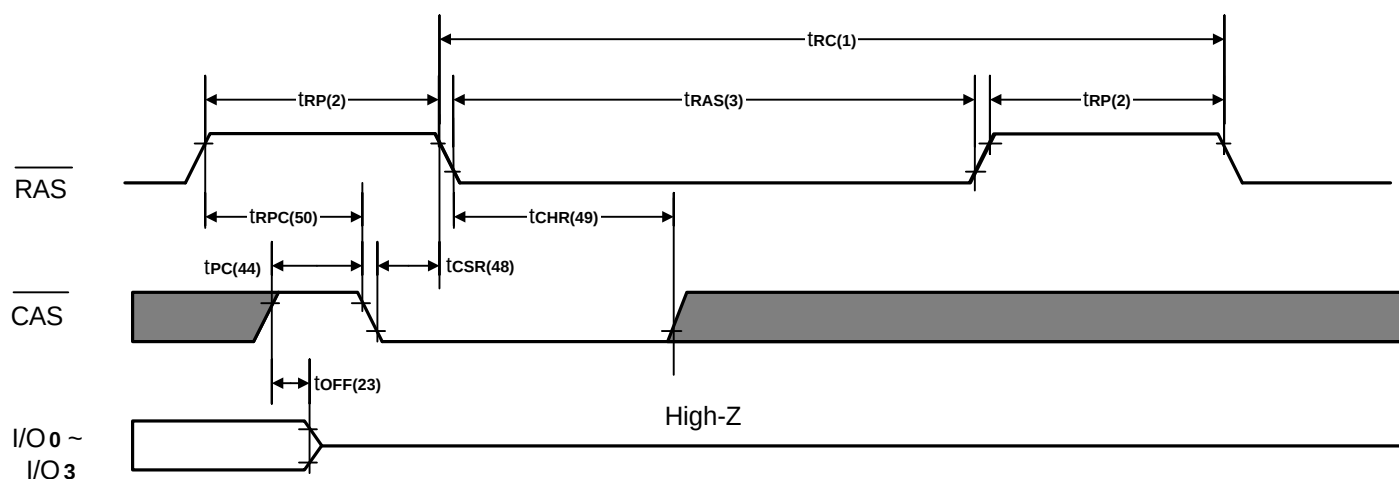
$\overline{\text{RAS}}$ Only Refresh Cycle



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care.

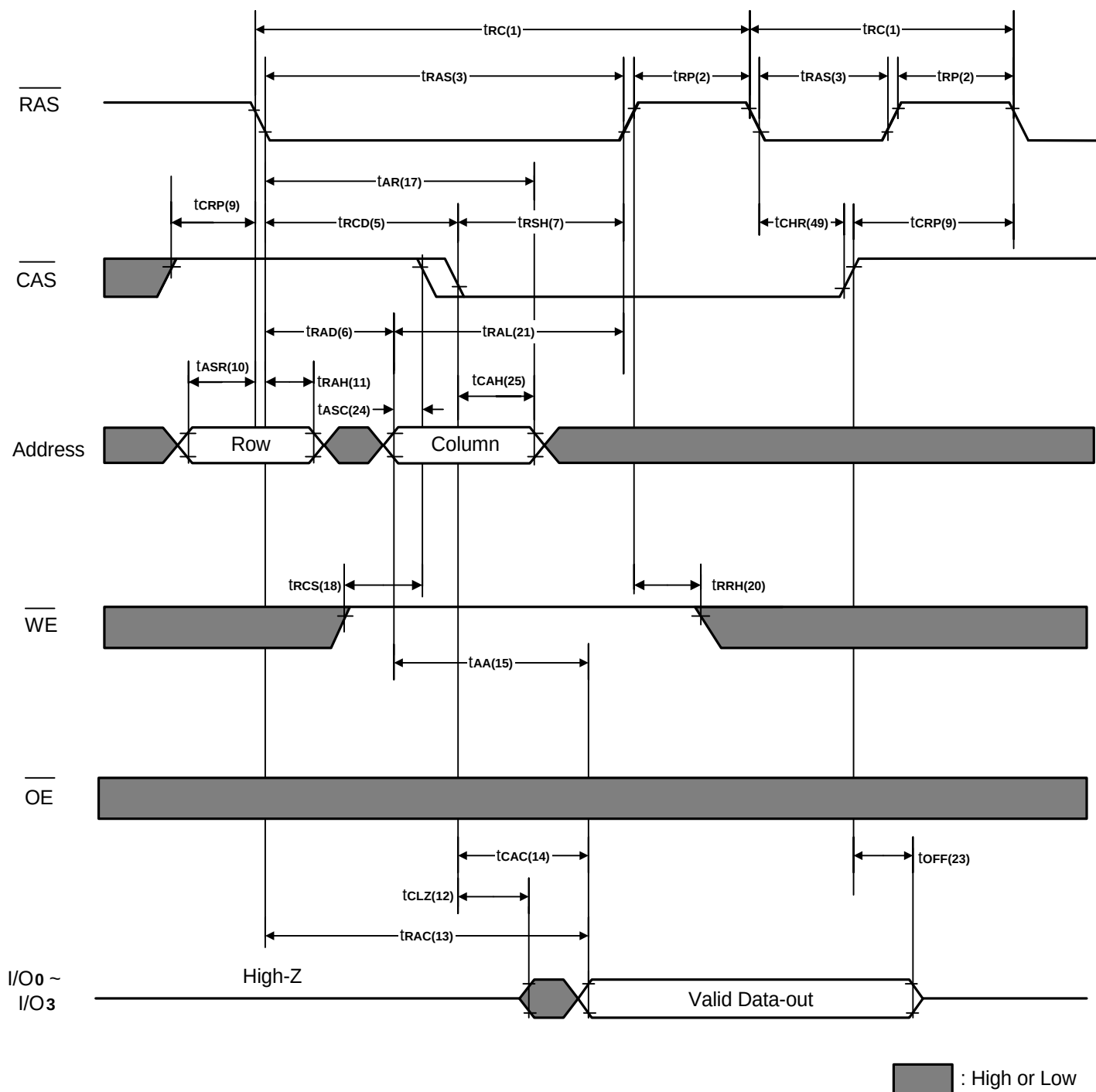
 : High or Low

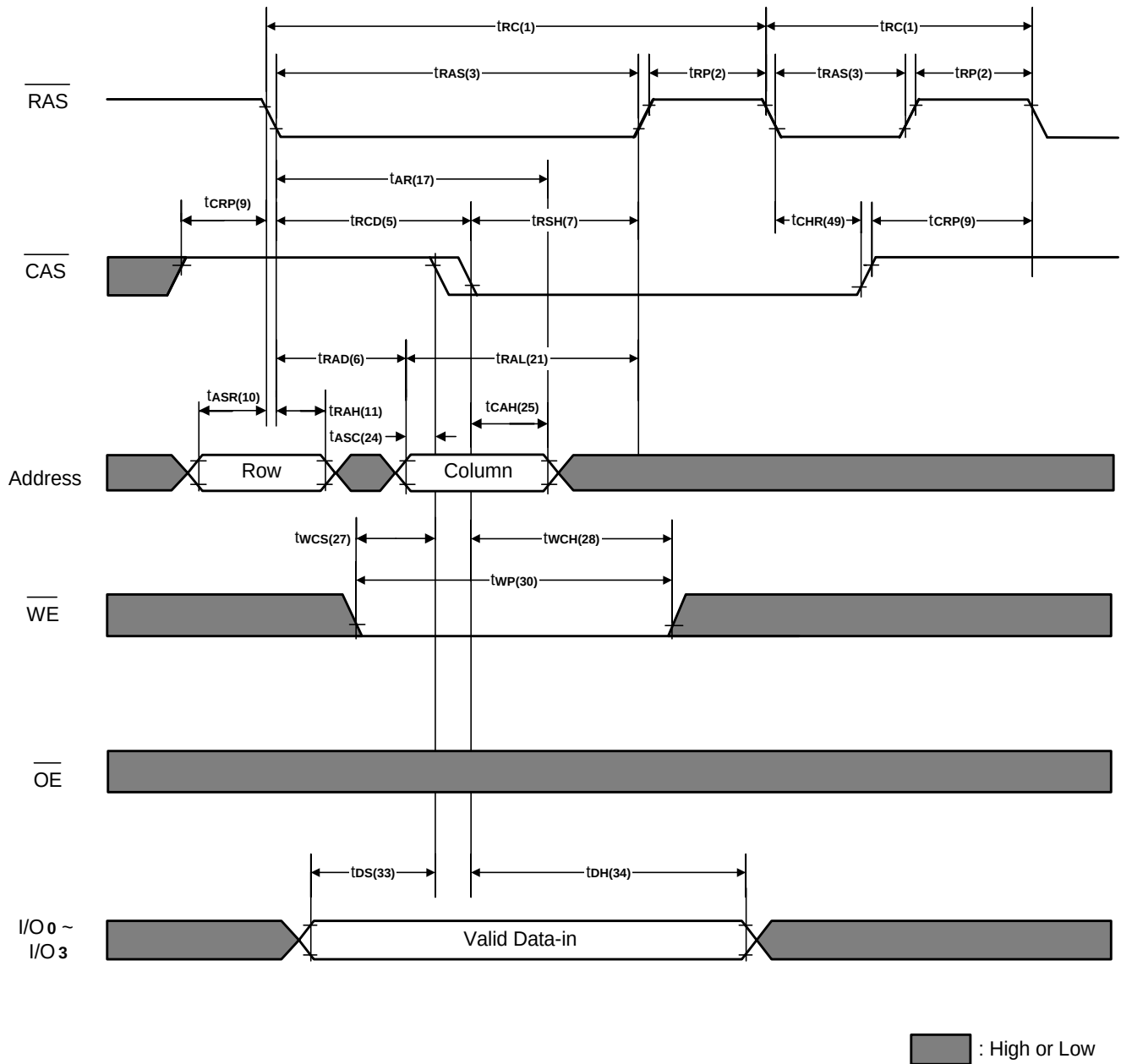
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, Address = Don't care.

 : High or Low

Hidden Refresh Cycle (Word Read)


Hidden Refresh Cycle (Early Word Write)


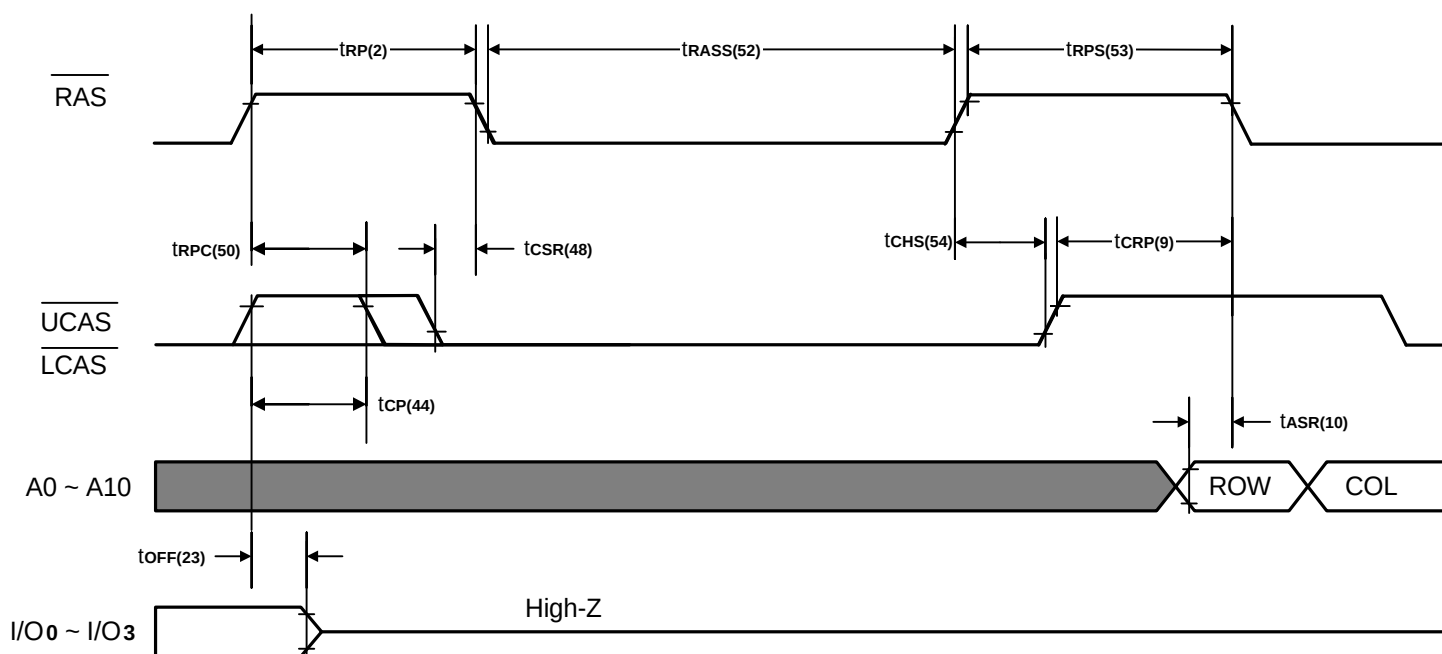


The diagram illustrates the timing relationships for a memory device. The signals shown are RAS, CAS, Address, WE, OE, and I/O0 ~ I/O3. The Address bus is divided into Row and Column segments. The Data bus is divided into Data-out and Data-in segments. The timing parameters are defined as follows:

- $t_{RASP}(47)$: RAS pulse width
- $t_{RSP}(2)$: RAS setup time
- $t_{CSH}(8)$: CAS setup time
- $t_{PC}(42)$: Precharge time
- $t_{RSH}(7)$: RAS hold time
- $t_{CRP}(9)$: CAS to RAS precharge time
- $t_{RCD}(5)$: RAS to CAS delay
- $t_{CAS}(4)$: CAS pulse width
- $t_{CP}(44)$: CAS to Precharge time
- $t_{ASR}(10)$: Address setup time
- $t_{RAH}(11)$: Row Address Hold time
- $t_{ASC}(24)$: Address to Column Select time
- $t_{CAH}(25)$: Column Address Hold time
- $t_{RCH}(19)$: Row to Column Select time
- $t_{RCS}(18)$: Row to Column Select time
- $t_{AA}(15)$: Address to Array Access time
- $t_{RAC}(13)$: Row to Array Access time
- $t_{CAC}(14)$: Column to Array Access time
- $t_{OEA}(16)$: Output Enable to Array Access time
- $t_{COH}(22)$: Column to Output Hold time
- $t_{DS}(33)$: Data Setup time
- $t_{DH}(34)$: Data Hold time
- $t_{WCS}(27)$: Write Command Setup time
- $t_{WCH}(28)$: Write Command Hold time

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Self Refresh Mode



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

 : High or Low

■ Self Refresh Mode.

a. Entering the Self Refresh Mode:

The A42L2604 Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal "low" longer than 100 μ s.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{RAS}$ "low" after entering the Self Refresh Mode.

It does not depend on $\overline{CAS}$ being "high" or "low" after entering the Self Refresh Mode continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The A42L2604 exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

Capacitance (f = 1MHz, Ta = Room Temperature, VCC = 3.3V ± 10%)

Symbol	Signals	Parameter	Max.	Unit	Test Conditions
C _{IN1}	A0 – A10	Input Capacitance	5	pF	V _{in} = 0V
C _{IN2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$		7	pF	V _{in} = 0V
C _{I/O}	I/O ₀ - I/O ₃	I/O Capacitance	7	pF	V _{in} = V _{out} = 0V

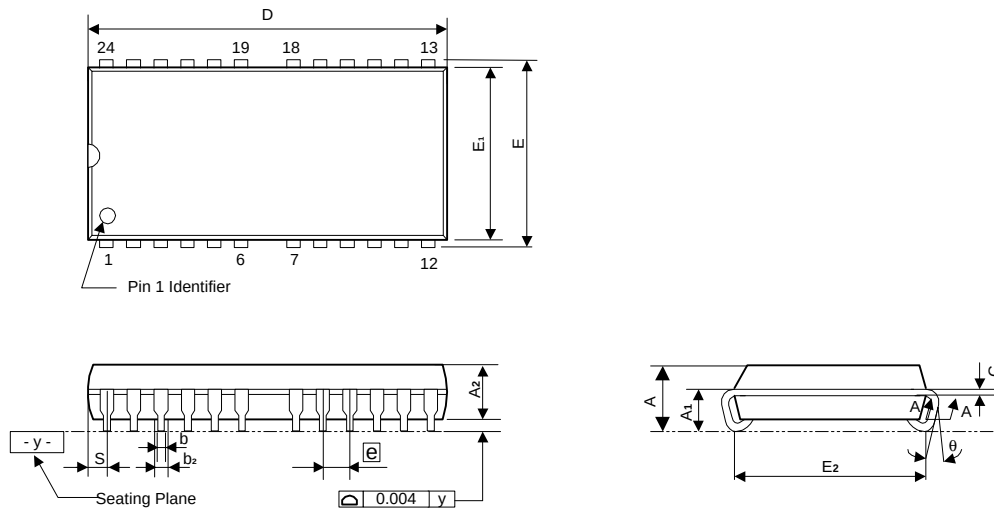
Ordering Codes

Package	$\overline{\text{RAS}}$ Access Time	45ns	50ns	Refresh Cycle	Self-Refresh
24/26L SOJ (300mil)		A42L2604S-45	A42L2604S-50	2K	No
24/26L TSOP type II (300mil)		A42L2604V-45	A42L2604V-50	2K	No
24/26L TSOP type II (300mil)		A42L2604V-45U	A42L2604V-50U	2K	No
24/26L SOJ (300mil)		A42L2604S-45L	A42L2604S-50L	2K	Yes
24/26L TSOP type II (300mil)		A42L2604V-45L	A42L2604V-50L	2K	Yes
24/26L TSOP type II (300mil)		A42L2604V-45LU	A42L2604V-50LU	2K	Yes

Note: -U is for industrial operating temperature range.

Package Information
SOJ 24L/26L (300mil) Outline Dimensions

unit: inches/mm



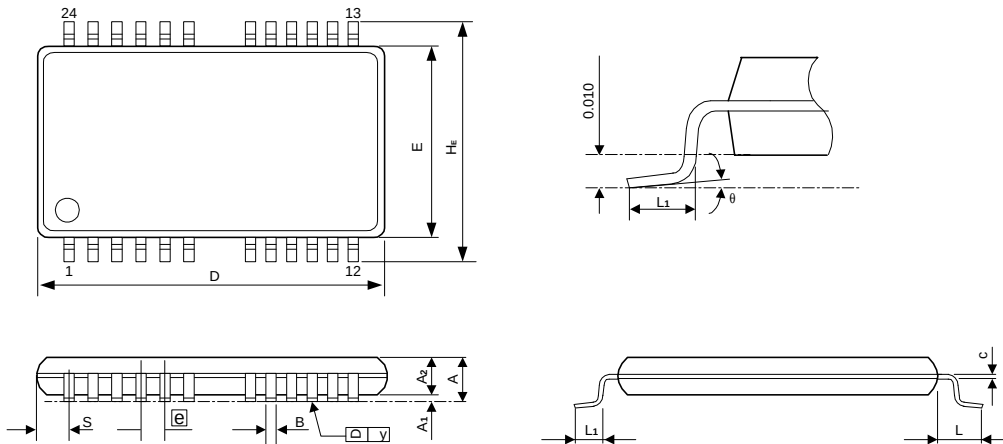
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.140	-	-	3.56
A ₁	0.070	0.080	0.090	1.78	2.03	2.29
A ₂	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.022	0.41	0.46	0.56
b ₂	0.026	0.028	0.032	0.66	0.71	0.81
C	0.008	0.010	0.014	0.20	0.25	0.36
D	-	0.675	0.686	-	17.15	17.42
E	0.327	0.337	0.347	8.31	8.56	8.81
E ₁	0.295	0.300	0.305	7.49	7.62	7.75
E ₂	0.245	0.265	0.285	6.22	6.73	7.24
$\overline{e}$	0.044	0.050	0.056	1.12	1.27	1.42
S	-	-	0.048	-	-	1.22
θ	0°	-	10°	0°	-	10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E₁ does not include resin fins.
3. Dimension E₂ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information
TSOP 24/26L (TYPE II) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.012	0.016	0.020	0.30	0.40	0.50
c	-	0.005	-	-	0.127	-
D	0.671	0.675	0.679	17.04	17.14	17.24
E	0.298	0.300	0.302	7.57	7.62	7.67
e	-	0.050	-	-	1.27	-
HE	0.355	0.363	0.371	9.02	9.22	9.42
L	-	0.031	-	-	0.80	-
L1	0.016	0.020	0.024	0.40	0.50	0.60
S	-	0.037	-	-	0.95	-
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes:

1. Dimension D&E do not included interlead flash.
2. Dimension B does not included dambar protrusion / intrusion.
3. Dimension S includes end flash.