

100364 Low Power 16-Input Multiplexer

General Description

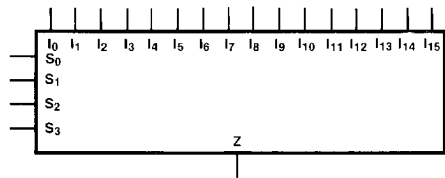
The 100364 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0 – S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data. All inputs have 50 k Ω pulldown resistors.

- 2000V ESD protection
- Pin/function compatible with 100164
- Voltage compensated operating range = –4.2V to –5.7V
- Available to industrial grade temperature range
- Standard Microcircuit Drawing (SMD) 5962-9459201

Features

- 35% power reduction of the 100164

Logic Symbol

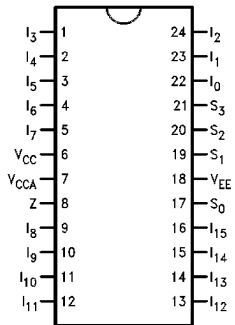


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Pin Names	Description
I_0 – I_{15}	Data Inputs
S_0 – S_3	Select Inputs
Z	Data Output

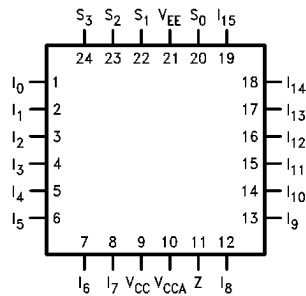
Connection Diagrams

24-Pin DIP



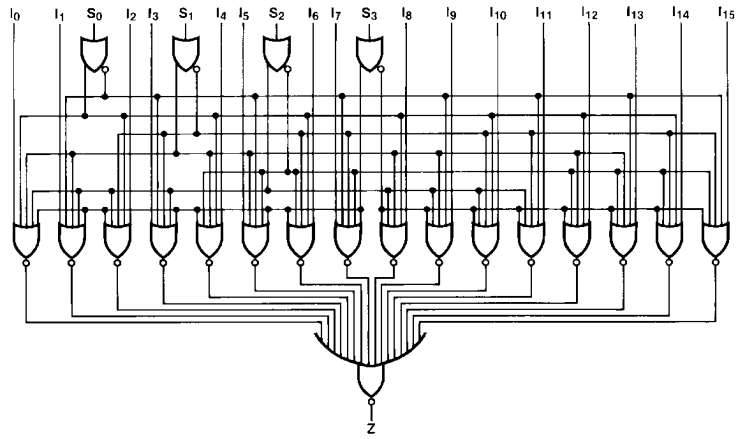
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24-Pin Quad Cerpak



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Logic Diagram



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Truth Table

Select Inputs				Output
S ₀	S ₁	S ₂	S ₃	Z
L	L	L	L	I ₀
H	L	L	L	I ₁
L	H	L	L	I ₂
H	H	L	L	I ₃
L	L	H	L	I ₄
H	L	H	L	I ₅
L	H	H	L	I ₆
H	H	H	L	I ₇
L	L	L	H	I ₈
H	L	L	H	I ₉
L	H	L	H	I ₁₀
H	H	L	H	I ₁₁
L	L	H	H	I ₁₂
H	L	H	H	I ₁₃
L	H	H	H	I ₁₄
H	H	H	H	I ₁₅

H = HIGH Voltage Level

L = LOW Voltage Level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired	
Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Pin Potential to	
Ground Pin (V_{EE})	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V

Output Current	
(DC Output HIGH)	-50 mA
ESD (Note 2)	≥ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	-55°C to +125°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55°C$ to $+125°C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085	-870	mV	-55°C			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C			
		-1830	-1555	mV	-55°C			
V_{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085		mV	-55°C			
V_{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C			
			-1555	mV	-55°C			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(Notes 3, 4, 5, 6)	
V_{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Notes 3, 4, 5, 6)	
I_{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)	(Notes 3, 4, 5)	
I_{IH}	Input HIGH Current		300	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	(Notes 3, 4, 5)	
			450	μA	-55°C			
I_{EE}	Power Supply Current	-95	-35	mA	-55°C to +125°C	Inputs Open	(Notes 3, 4, 5)	

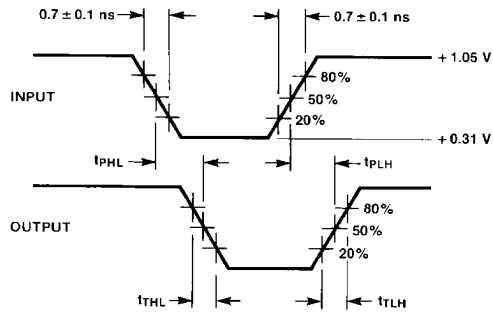
Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7 and 8.

Note 5: Sampled tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Switching Waveforms



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Note 11: $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

Note 12: L1 and L2 = Equal length 50Ω impedance lines

Note 13: $R_T = 50\Omega$ terminator internal to scope

Note 14: Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}

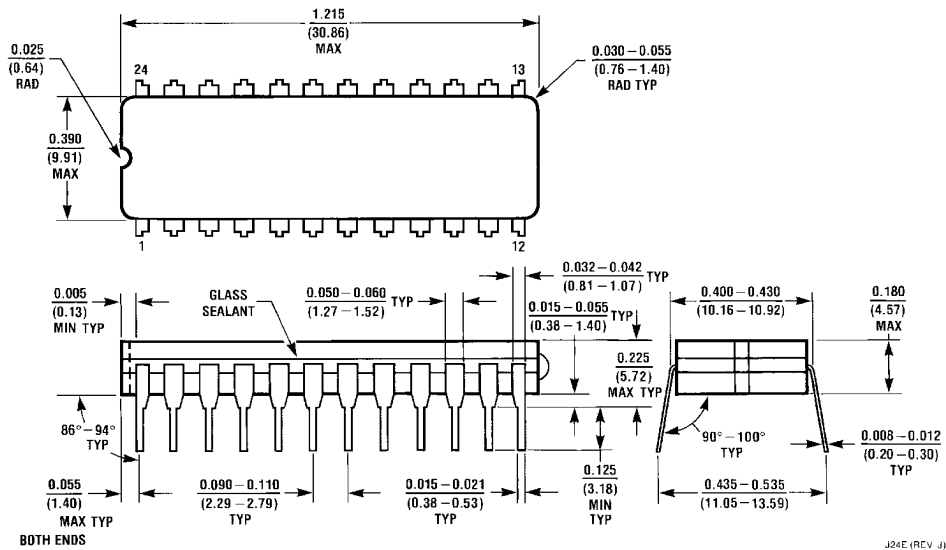
Note 15: All unused outputs are loaded with 50Ω to GND

Note 16: C_L = Fixture and stray capacitance $\leq 3 \text{ pF}$

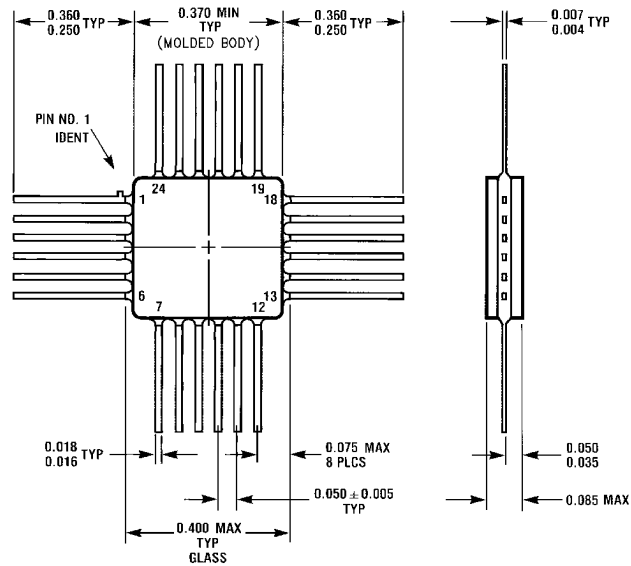
Note 17: Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B