PLESSEY
Semiconductors

T-51-09-08

ZN558

8-BIT LATCHED INPUT MONOLITHIC D-A CONVERTER

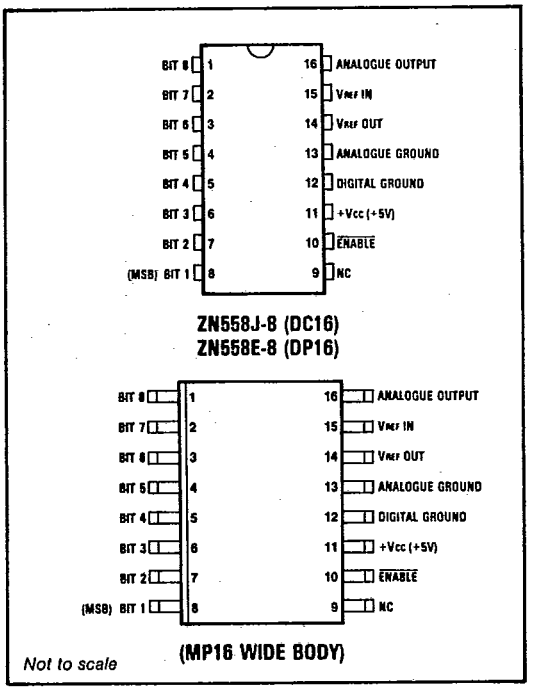
The ZN558 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The ZN558 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

FEATURES

- Contains DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Single +5V Supply
- Microprocessor Compatible
- TTL and 5V CMOS Compatible
- 800ns Settling Time
- Complementary to ZN447 A-D Series
- Commercial and Military Temperature Ranges
- Available in Miniature Plastic Surface Mount Package (MP16)

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN558D	0°C to +70°C	MP16
ZN558E-8	0°C to +70°C	DP16
ZN558J-8	-55°C to +125°C	DC16



Pin connections - top view

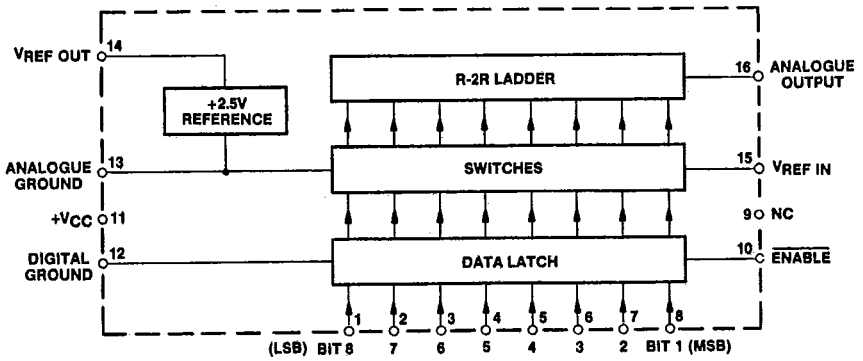


Fig.1 System diagram

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ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	+7.0V
Max. voltage, logic and V_{REF} input	+Vcc
Operating temperature range	0°C to +70°C (ZN558E-8, ZN558D) -55°C to +125°C (ZN558J-8)
Storage temperature range	-55°C to +125°C
Analogue ground to digital ground	±200mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal voltage reference					
Output voltage	2.475	2.550	2.625	V	R_{REF} = 390Ω, C_{REF} = 1μF
Slope resistance		0.5	2	Ω	
$V_{REF\ OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D-A converter					
Linearity error			±0.5	LSB	2.0V ≤ $V_{REF\ IN}$ ≤ 3.0V
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage		±6		μV/°C	
Full scale output	2.545	2.550	2.555		External reference $V_{REF\ IN}$ = 2.560V, all bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	V	
Settling time to 0.5 LSB		800		ns	1 LSB major transition (note 2)
		1.25		μs	All bits ON to OFF or OFF to ON (note 2)
Operating temperature range:					
ZN558E-8/D	0		70	C	
ZN558J-8	-55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	V	

Note 1 See REFERENCE, page 1-88.
Note 2 R_L = 10MΩ, C_L = 10pF.

ELECTRICAL CHARACTERISTICS (Cont.) T-51-09-08

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range)					
High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	μA	$V_{IN}=5.5V$, $V_{CC}=$Max.
			20	μA	$V_{IN}=2.4V$, $V_{CC}=$Max.
Low level input current			−5	μA	$V_{IN}=0.4V$, $V_{CC}=$Max.
Input clamp diode voltage		−1.5		V	$I_{IN}=-8mA$
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH ($V_{IH}=3.5V$).
Note 4 Set up time before $\overline{\text{enable}}$ goes high.
Note 5 Hold time after $\overline{\text{enable}}$ goes high.

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\,IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

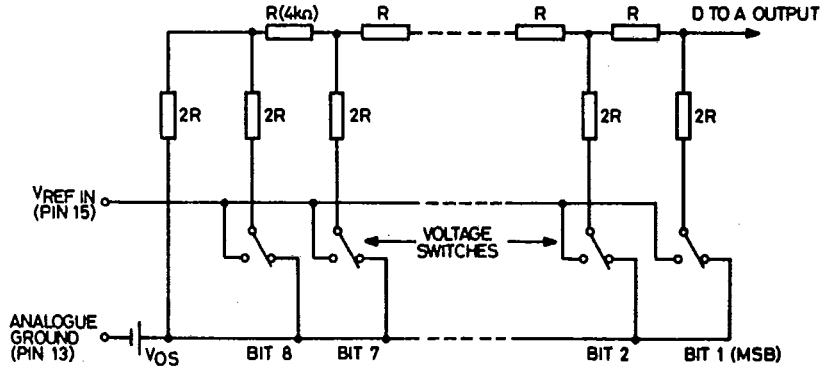

Fig. 2 The R-2R ladder network

Analogue output = $\frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

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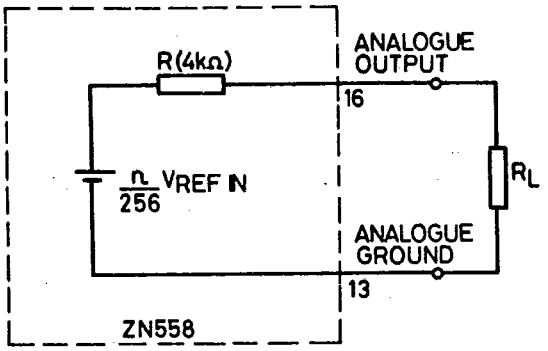

Fig. 3 Analogue output equivalent circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

R_L should be chosen to be as large as possible to make the gain drift small. As an example if R_L = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN558 can be buffered by an amplifier (see Operating Notes).

REFERENCE

(a) Internal reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 11) and pin 14. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF} = 1\mu F$ is required between pins 14 and 13 for internal reference option, $V_{REF\ OUT}$ (pin 14) being connected to $V_{REF\ IN}$ (pin 15).

Up to five ZN558's may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

(b) External reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN558 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

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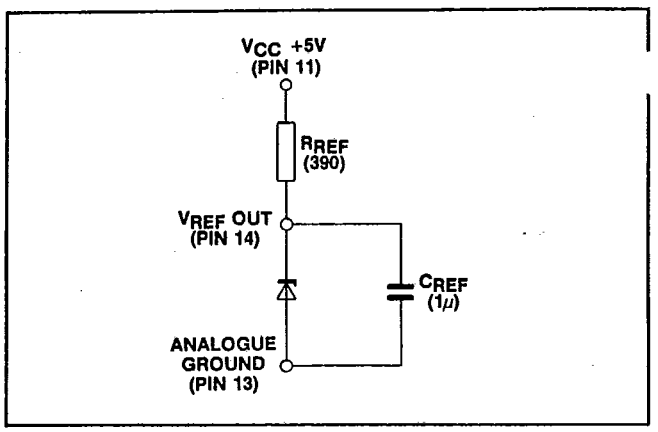

Fig.4 Internal voltage reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D-A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig.5.

The ZN558 is provided with seperate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

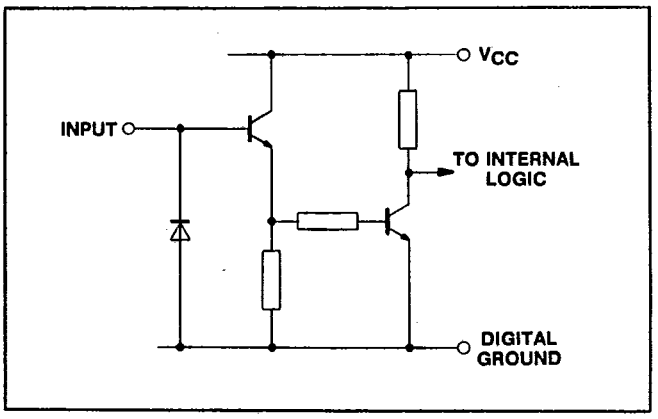

Fig. 5 Equivalent circuit of all inputs

OPERATING NOTES

(1) Unipolar D-A converter

The nominal output range of the ZN558 is 0 to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R1 and R2 are given by $R1 = 4GkΩ$ and $R_2 = 4G/(G-1)kΩ$.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Output range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig. 7. Settling time for a major transistion is 1.5μs typical.

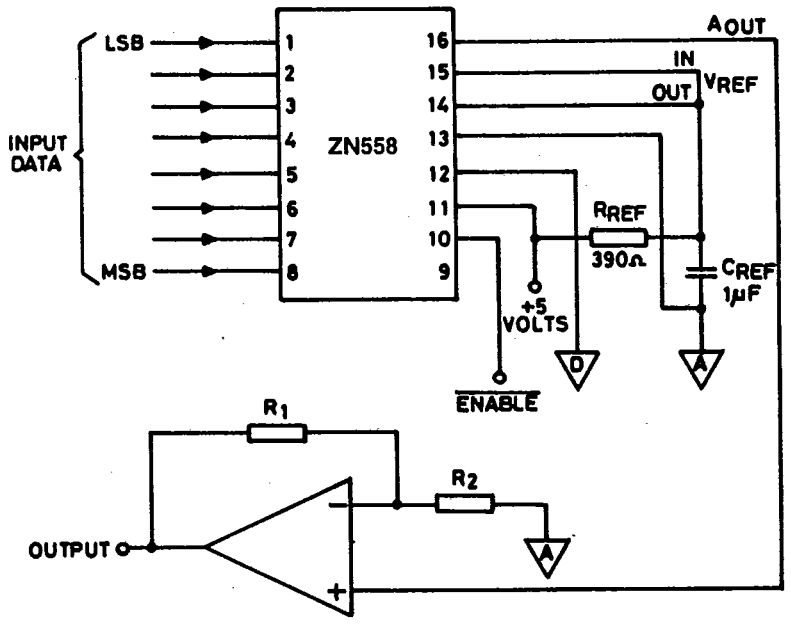

Fig. 6 Unipolar operation - basic circuit

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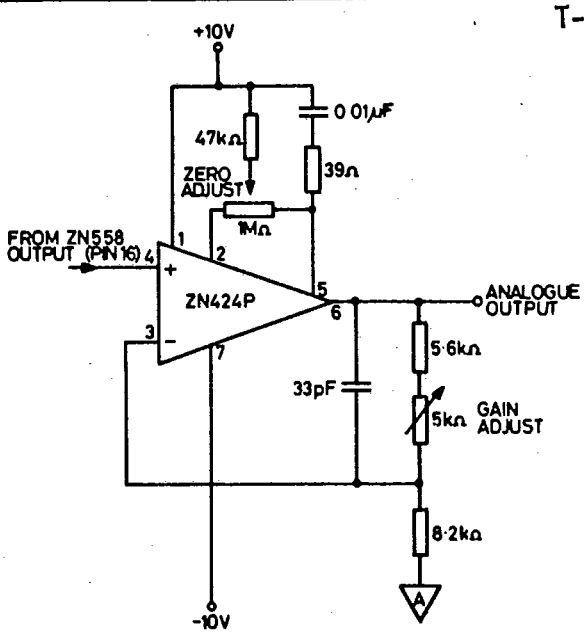
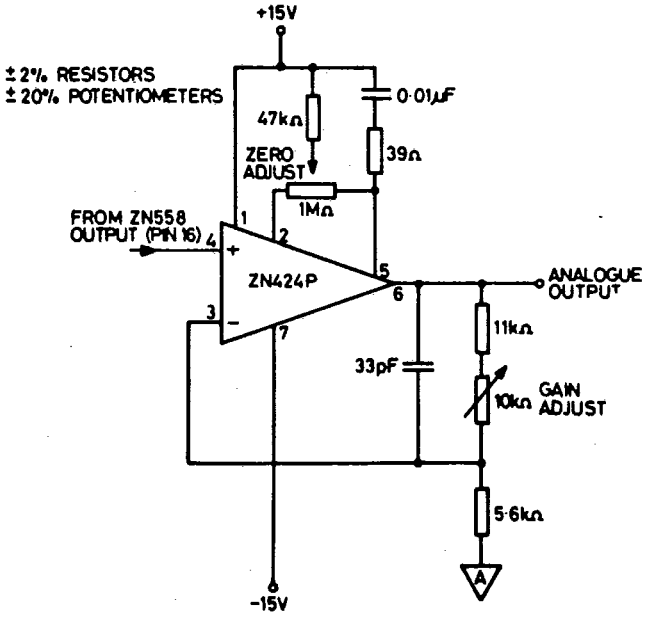


+5 VOLTS FULL SCALE



+10 VOLTS FULL SCALE

Fig. 7 Unipolar operation - component values

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UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.
(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

UNIPOLAR SETTING UP POINTS

Output range, +FS	LSB	FS - 1LSB
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input code (Binary)	Analogue output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	¾ FS
10000001	½FS + 1LSB
10000000	½FS
01111111	½FS - 1LSB
01000000	¼FS
00000001	1LSB
00000000	0

(2) Bipolar D-A converter

For bipolar operation the output from the ZN558 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

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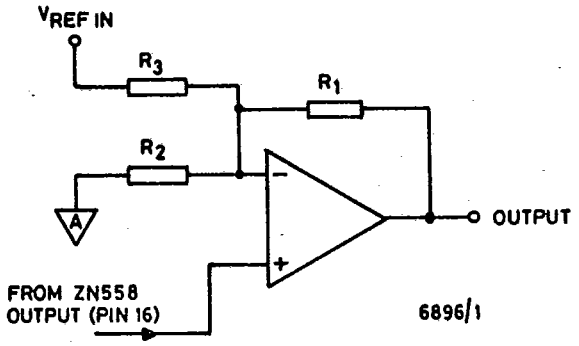

Fig. 8 Bipolar operation - basic circuit

When the digital input to the ZN558 is zero the analogue output is zero and the amplifier output should be −full scale. An input of all ones to the D-A will give a ZN558 output of $V_{REF\ IN}$ and the amplifier output required is +full scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

Output range	G	R_1	R_2	R_3
±5V	2	16kΩ	16kΩ	8kΩ
±10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 9.

Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5μs typical.

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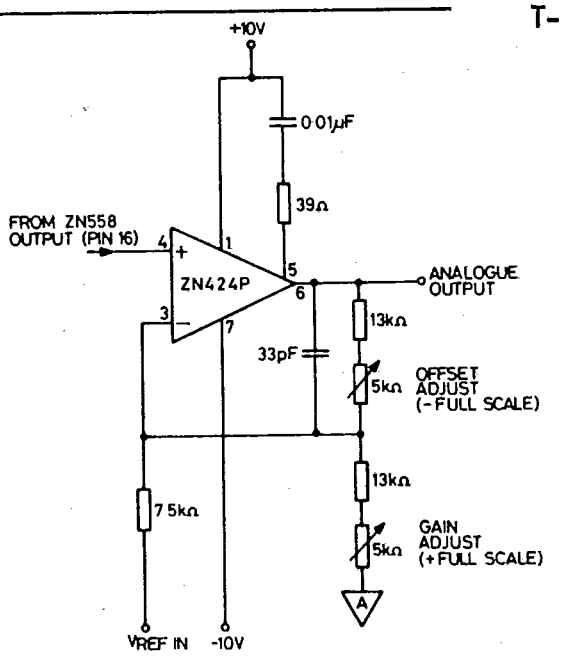

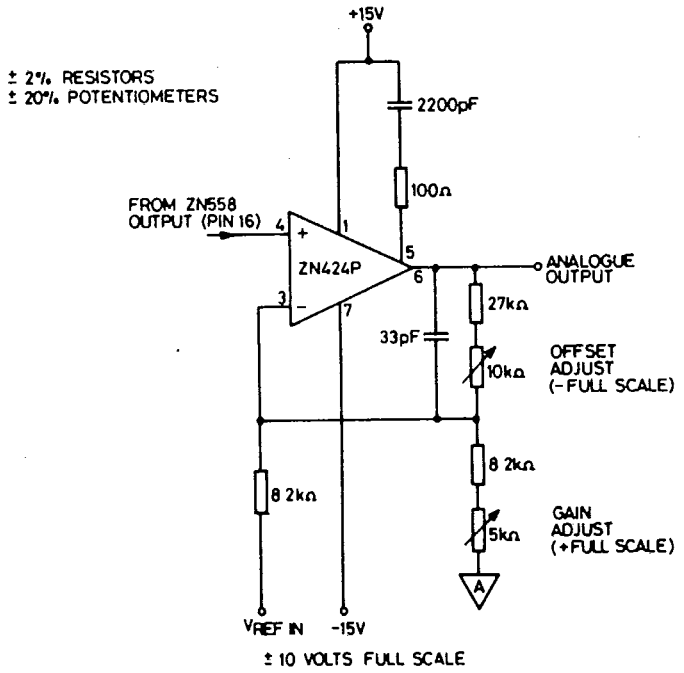

Fig. 9 Bipolar operation - component values

Bipolar Adjustment Procedure

(1) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads −full scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads +(full scale - 1LSB).

BIPOLAR SETTING UP POINTS

Input range, ±FS	LSB	−FS	+(FS - 1LSB)
±5V	39.1mV	−5.0000V	+4.9609V
±10V	78.1mV	−10.0000V	+9.9219V

$$1LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Input code (Offset binary)	Analogue output (Nominal value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	−1LSB
01000000	−½FS
00000001	−(FS - 1LSB)
00000000	−FS