STL60N32N3LL

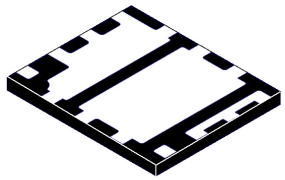
Dual N-channel 30 V, 0.006 Ω, 15 A PowerFLAT™5x6 asymmetrical double island, STripFET™ Power MOSFET

Target specification

Features

Type		V_{DSS}	$R_{DS(on)}$	I_D
STL60N32N3LL	Q_1	30 V	< 0.012 Ω	12 A
	Q_2	30 V	< 0.008 Ω	15 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



PowerFLAT™5x6 asymmetrical double island

Application

- Switching applications

Description

This product utilizes latest generations of design rules of ST's proprietary STripFET™ V and STripFET™ VI DeepGATE technology. The lowest available $R_{DS(on)}$*Q_g, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

Figure 1. Internal schematic diagram

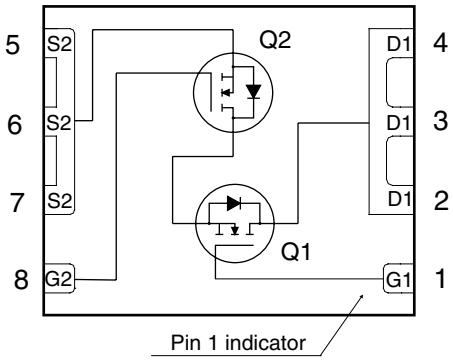


Table 1. Device summary

Order code	Marking	Package	Packaging
STL60N32N3LL	60N32N3LL	PowerFLAT™5x6 asymmetrical double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Type	Value	Unit
V_{DS}	Drain-source voltage (v_{GS} = 0)	Q_1 Q_2	30 30	V V
V_{GS}	Gate- source voltage	Q_1 Q_2	± 22 ± 20	V V
I_D(1)	Drain current (continuous) at T_C = 25°C	Q_1 Q_2	32 60	A A
I_D(1)	Drain current (continuous) at T_C = 100°C	Q_1 Q_2	20 37	A A
I_D(2)	Drain current (continuous) at T_C = 25°C	Q_1 Q_2	12 15	A A
I_D(2)	Drain current (continuous) at T_C = 100°C	Q_1 Q_2	7.5 9	A A
I_{DM} (3)	Drain current (pulsed)	Q_1 Q_2	48 60	A A
P_{TOT}(1)	Total dissipation at T_C = 25°C	Q_1 Q_2	23 50	W W
P_{TOT}(2)	Total dissipation at T_C = 25°C	Q_1 Q_2	3.12 3.12	W W
E_{AS}(4)	Single pulse avalanche energy		TBD	mJ

1. This value is accordingly $R_{thj\text{-}c}$
2. This value is accordingly $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area
4. Starting T_J = 25 °C, I_D = 7.5 A

Table 3. Thermal data

Symbol	Parameter	Type	Value	Unit
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-ambient max		40	°C/W
$R_{thj\text{-}c}$	Thermal resistance junction-case	Q_1 Q_2	5.5 2.5	°C/W
T_j	Thermal operating junction-ambient		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	Q_1 Q_2	30 30			V V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating	Q_1 Q_2			1 1	µA µA
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} =Max rating @125°C	Q_1 Q_2			10 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 22 V	Q_1 Q_2			±100 ±100	nA nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	Q_1 Q_2	1 1			V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 6 A V_{GS} = 10 V, I_D = 7.5 A	Q_1 Q_2		0.01 0.006	0.12 0.008	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 4.5 V, I_D = 6 A V_{GS} = 4.5 V, I_D = 7.5 A	Q_1 Q_2		0.0115 0.009	0.014 0.011	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	Q_1 Q_2	-	1020 1690	-	pF pF
C_{oss}	Output capacitance		Q_1 Q_2	-	200 291	-	pF pF
C_{rss}	Reverse transfer capacitance		Q_1 Q_2	-	26 176	-	pF pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 15 A, V_{GS} = 4.5 V *(see Figure 3)*	Q_1 Q_2	-	7 17	-	nC nC
Q_{gs}	Gate-source charge		Q_1 Q_2	-	TBD TBD	-	nC nC
Q_{gd}	Gate-drain charge		Q_1 Q_2	-	TBD TBD	-	nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=15 V, I_D=7.5 A, R_G=4.7 Ω, V_{GS}= 4.5 V *(see Figure 7)*	Q_1 Q_2 Q_1 Q_2	-	TBD	-	ns ns ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=15 V, I_D=7.5 A, R_G=4.7 Ω, V_{GS}= 4.5V *(see Figure 7)*	Q_1 Q_2 Q_1 Q_2	-	TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	V_{DD}=15 V, I_D=7.5 A R_G=4.7 Ω, V_{GS}=4.5 V	Q_1 Q_2	-		12 15	A A
I_{SDM} (1)	Source-drain current (pulsed)	V_{DD}=15 V, I_D= 7.5 A R_G=4.7 Ω, V_{GS}=4.5 V	Q_1 Q_2	-		48 60	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0	Q_1 Q_2	-		1.1 1.1	V V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 15 A, V_{DD} = 15 V di/dt = 100 A/µs, T_j = 150°C *(see Figure 7)*	Q_1 Q_2 Q_1 Q_2 Q_1 Q_2	-	TBD TBD TBD TBD TBD TBD		ns ns nC nC A A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

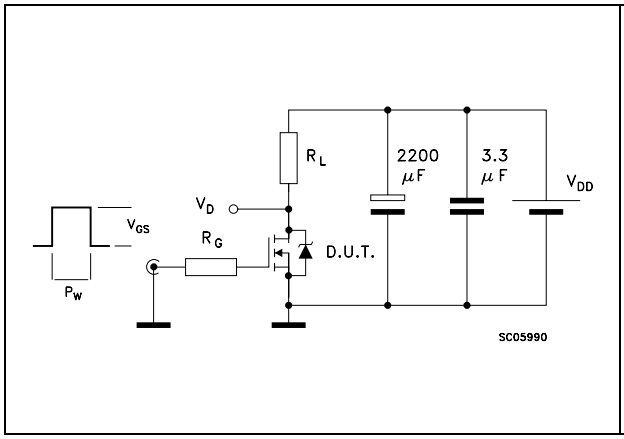


Figure 3. Gate charge test circuit

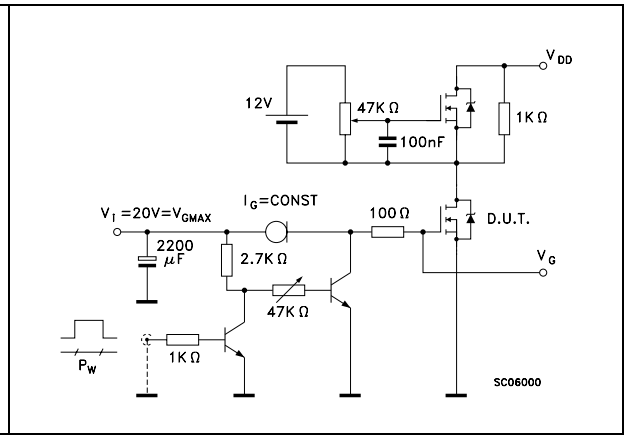


Figure 4. Test circuit for inductive load switching and diode recovery times

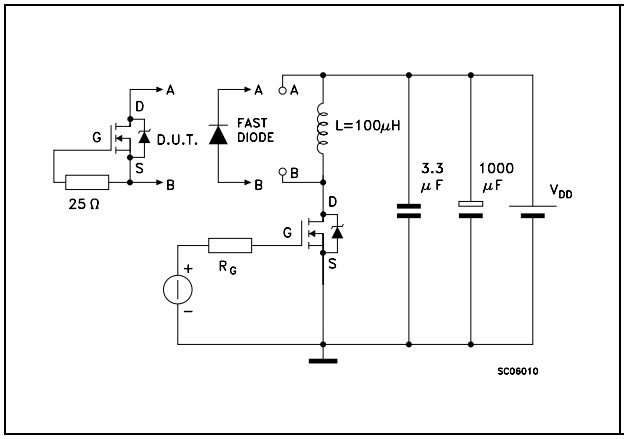


Figure 5. Unclamped inductive load test circuit

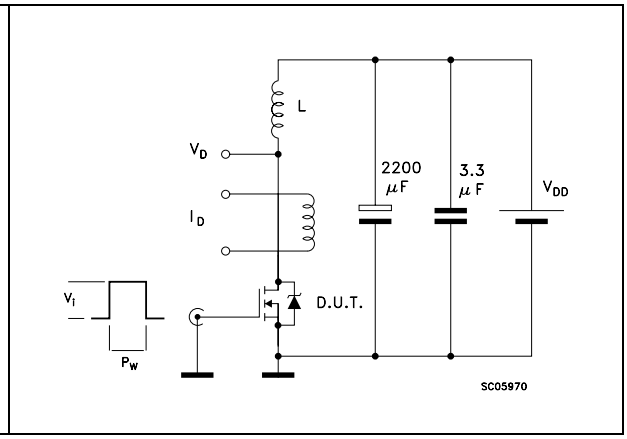


Figure 6. Unclamped inductive waveform

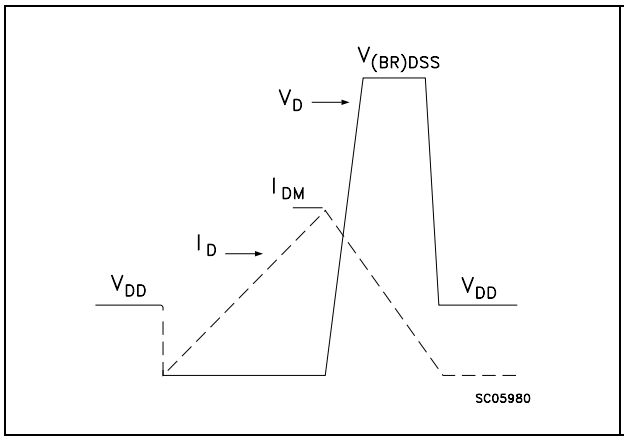
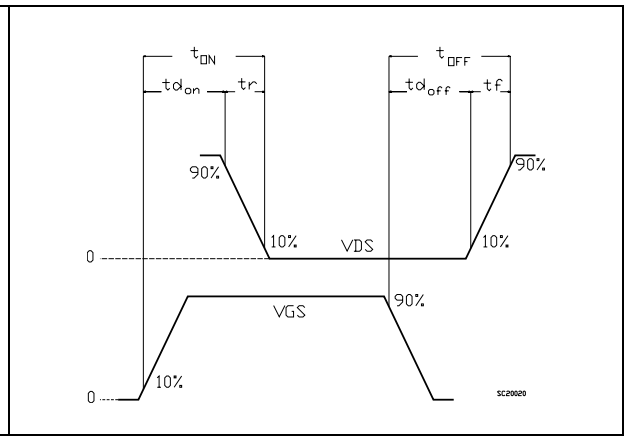


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 asymmetrical double island dimentions

Dim.	mm		
	Min.	Typ.	Max.
A	0.77		0.97
A1			0.03
b	0.42		0.52
D	4.90	5.00‘	5.10
D2	2.40		2.60
E	5.90	6.00	6.10
E2	2.90		3.10
e		1.27	
L	0.40		0.60

Figure 8. Package drawing

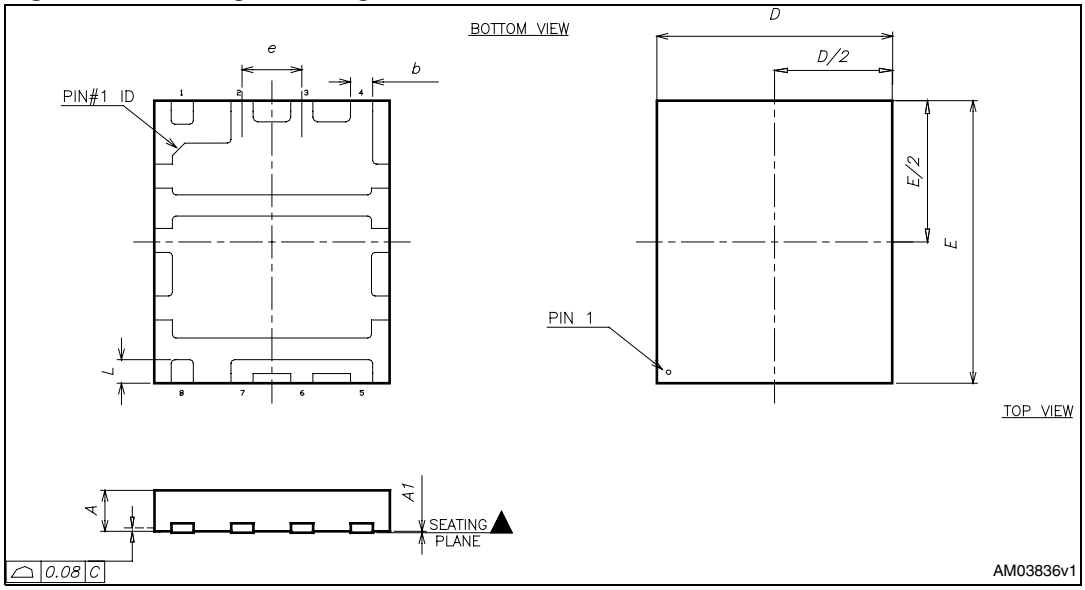
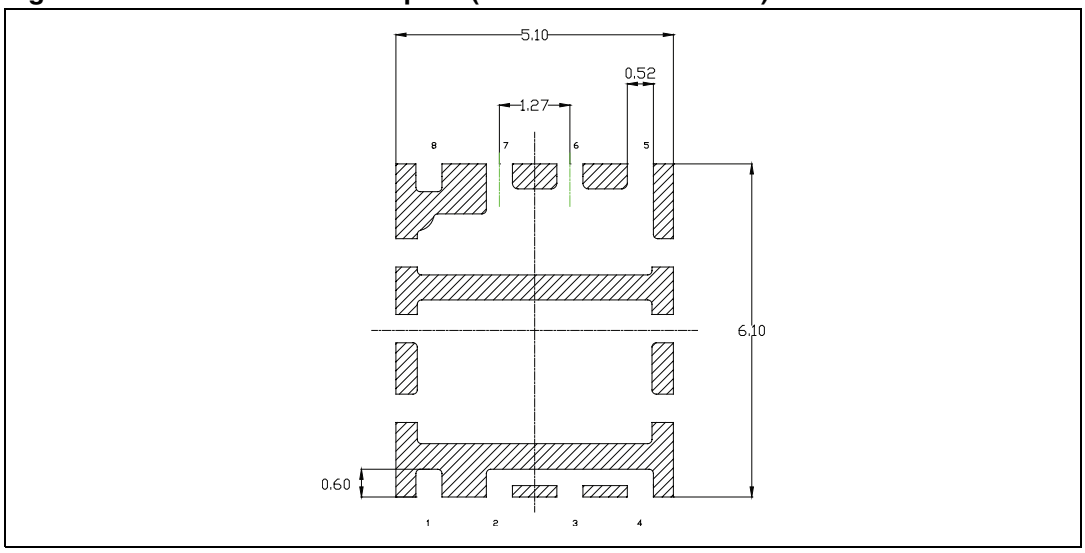


Figure 9. Recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Mar-2010	1	First release

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