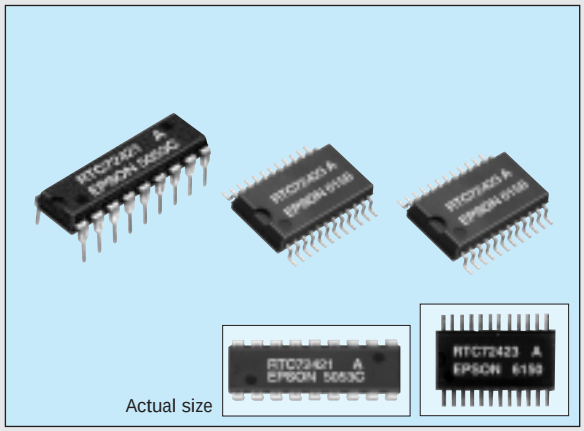
4-bit REAL TIME CLOCK MODULE

RTC-72421/72423

- Builtin crystal unit allows adjustment-free efficient operation.
- ALE input terminal available for 8048, 8051, and 8085 series.
- 12/24H clock switchover function and automatic leap year setting.
- Interrupt masking.
- 30 second adjustment function.
- Low current consumption and features a backup function.



Specifications (characteristics)

Absolute Max. rating

Item	Symbol	Condition	Specifications	Unit
Power source voltage	V_{DD}	Ta=25°C	-0.3 to 7.0	V
Input and output voltage	$V_{I/O}$	Ta=25°C	GND -0.3 to V_{DD}+0.3	
Storage temperature	T_{STG}	RTC-72421	-55 to +85	°C
		RTC-72423	-55 to +125	
Soldering condition	T_{SOL}	RTC-72421	Under 260°C within 10 sec. (lead part) (package should be less than 150°C)	
		RTC-72423	Twice at under 260°C within 10 sec. or under 230°C within 3 min.	

Operating range

Item	Symbol	Condition	Specifications	Unit
Operating voltage	V_{DD}		4.5 to 5.5	V
Operating temperature	T_{OPR}	RTC-72421	-10 to 70	°C
		RTC-72423	-40 to 85	
Data holding voltage	V_{DH}		2.0 to 5.5	V
CSI data holding time	t_{CDR}	Refer to the data holding timing	2.0 min.	µs
Operation restoring time	t_R			

Frequency characteristics and current consumption characteristics

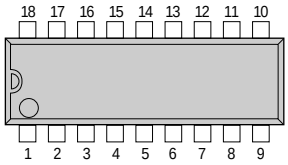
Item	Symbol	Condition		Specifications	Unit
Frequency tolerance	Δf/fo	Ta=25°C V_{DD}=5V	72421 A	±10	ppm
			72421 B	±50	
			72423 A	±20	
			72423	±50	
Frequency temperature characteristics		-10 to +70°C (25°C reference temperature)		+10/-120	
Aging	fa	V_{DD}=5V, Ta=25°C, first year		±5 max.	ppm/Y
Shock resistance	S.R.	Three drops on a hard board from 75 cm or 3000G x 0.3ms x 1/2 sine wave x 3 directions		±10 max.	ppm
Current consumption	I_{DD1}	CS_1=0V Exclude input/output current	V_{DD}=5V	10 max.	µA
	I_{DD2}		V_{DD}=2V	5 max.	

Electrical characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable terminal
"H" input voltage (1)	V_{IH1}	—	2.2	—	—	V	All inputs other than CS_1
"L" input voltage (1)	V_{IL1}		—		0.8		
Input leak current (1)	I_{LK1}	V_I=V_{DD}/0V	—	—	±1	µA	Input other than D_0 to D_3
Input leak current (2)	I_{LK2}				±10		D_0 to D_3
"L" output voltage (1)	V_{OL1}	I_{OL}=2.5mA			0.4	V	
"H" output voltage	V_{OH}	I_{OH}=-400µA	2.4		—		
"L" output voltage (2)	V_{OL2}	I_{OL}=2.5mA	—		0.4		STD.P
Off leak current	I_{OFFLK}	V_I=V_{DD}/0V			10	µA	
Input capacity	C_I	Input frequency 1 MHz		10	—	pF	Input other than D_0 to D_3
				20			D_0 to D_3
"H" input voltage (2)	V_{IH2}	V_{DD}=2 to 5.5V	4/5 V_{DD}	—	—	V	CS_1
"L" input voltage (2)	V_{IL2}		—		1/5 V_{DD}		

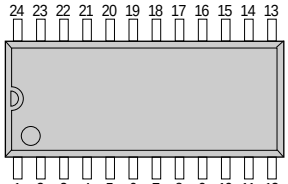
Terminal connection

RTC-72421



No.	72421	No.	72423
1	STD. P	1	STD. P
2	$\overline{CS_0}$	2	$\overline{CS_0}$
3	ALE	3	NC
4	A_0	4	ALE
5	A_1	5	A_0
6	A_2	6	NC
7	A_3	7	A_1
8	RD	8	NC
9	GND	9	A_2
10	$\overline{WR}$	10	A_3
11	D_3	11	RD
12	D_2	12	GND
13	D_1	13	$\overline{WR}$
14	D_0	14	D_3
15	CS_1	15	D_2
16	(V_{DD})	16	D_1
17	(V_{DD})	17	NC
18	V_{DD}	18	NC
		19	D_0
		20	CS_1
		21	NC
		22	(V_{DD})
		23	(V_{DD})
		24	V_{DD}

RTC-72423

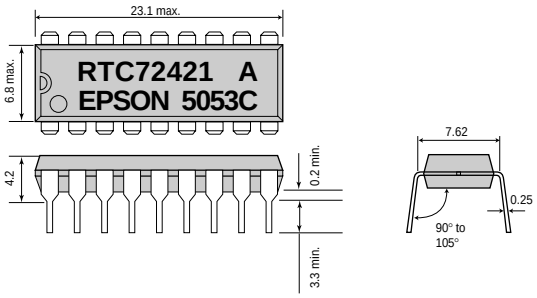


- (V_{DD}) and V_{DD} are to have the same level of voltage. Do not connect it to any external terminals.
- NC is not connected internally.

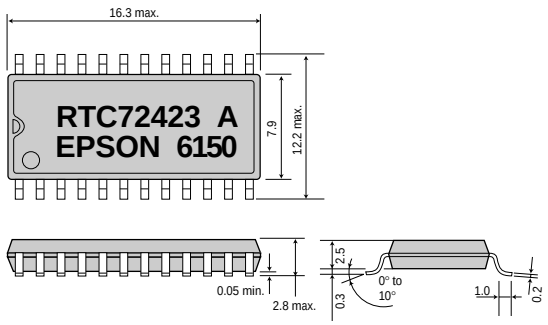
External dimensions

(Unit: mm)

RTC-72421



RTC-72423



Register table

Address	A3	A2	A1	A0	Register	Data D3	Data D2	Data D1	Data D0	Count Value	Remarks
0	0	0	0	0	S1	s8	s4	s2	s1	0 to 9	1- second digit register
1	0	0	0	1	S10	*	s40	s20	s10	0 to 5	10- second digit register
2	0	0	1	0	MI 1	mi8	mi4	mi2	mi1	0 to 9	1- minute digit register
3	0	0	1	1	MI10	*	mi40	mi20	mi10	0 to 5	10- minute digit register
4	0	1	0	0	H 1	h8	h4	h2	h1	0 to 9	1- hour digit register
5	0	1	0	1	H10	*	PM/AM	h20	h10	0 to 2 or 0 to 1	PM/AM,10- hours digit register
6	0	1	1	0	D1	d8	d4	d2	d1	0 to 9	1- day digit register
7	0	1	1	1	D10	*	*	d20	d10	0 to 3	10 -day digit register
8	1	0	0	0	MO1	mo8	mo4	mo2	mo1	0 to 9	1- month digit register
9	1	0	0	1	MO10	*	*	*	mo10	0 to 1	10- month digit register
A	1	0	1	0	Y1	y8	y4	y2	y1	0 to 9	1- year digit register
B	1	0	1	1	Y10	y80	y40	y20	y10		10- year digit register
C	1	1	0	0	W	*	w4	w2	w1	0 to 6	Week register
D	1	1	0	1	RegD	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	—	Control Register D
E	1	1	1	0	RegE	t1	t0	ITRPT /STND	MASK		Control Register E
F	1	1	1	1	RegF	TEST	24/12	STOP	REST		Control Register F

0="L" level,1="H" level, REST = RESET ITRPT/ STND=INTERRUPT/STANDARD

1) Bit * does not exist.
2) Please mask AM/PM bit with 10's of hours operations.
3) Busy is read only. IRQ can only. IRQ can only be set low ("O").
4)

Data Bit	PM/AM	ITRPT/STND	24/12
1	PM	ITRPT	24
0	AM	STND	12

5) TEST bit should be "O".

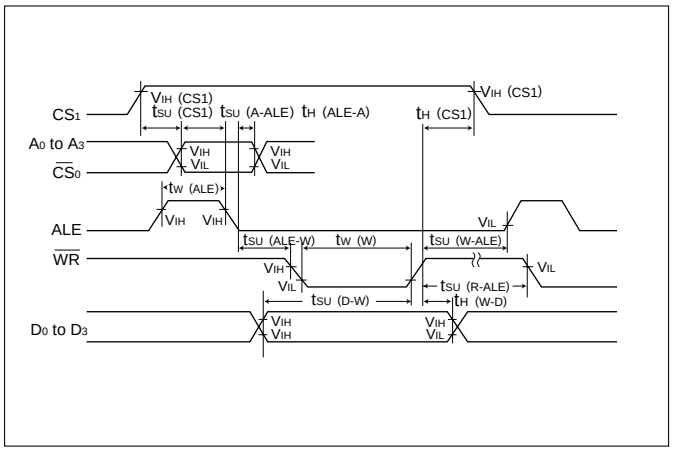
Switching characteristics (with ALE)

(Please connect ALE to V_{DD} if the microprocessor does not have an ALE output.)

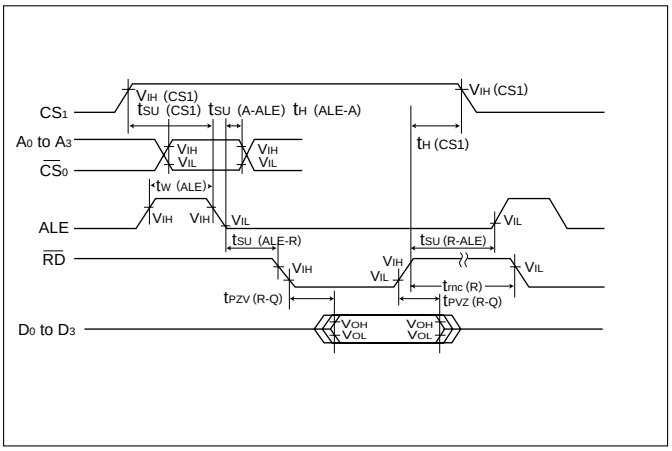
Item	Symbol	Condition	Min.	Max.	Unit
CS1 setup time	$t_{SU\ (CS1)}$		1000	—	ns
Address setup time before ALE	$t_{SU\ (A-ALE)}$		50		
Address hold time after ALE	$t_{H\ (ALE-A)}$		50		
ALE pulse width	$t_{W\ (ALE)}$		80		
ALE setup time before WRITE	$t_{SU\ (ALE-W)}$		0		
ALE setup time before READ	$t_{SU\ (ALE-R)}$		0		
ALE setup time after WRITE	$t_{SU\ (W-ALE)}$		50		
ALE setup time after READ	$t_{SU\ (R-ALE)}$		50		
WRITE pulse width	$t_{W\ (W)}$		120		
DATA delay time after READ	$t_{PZV\ (R-Q)}$	C_L=150pF	—	120	
DATA Hold time after READ	$t_{PVZ\ (R-Q)}$		0	70	
DATA setup time before WRITE	$t_{SU\ (D-W)}$		80	—	
DATA hold time after WRITE	$t_{H\ (W-D)}$		10		
CS1 hold time	$t_{H\ (CS1)}$		1000		
READ/WRITE recovery time	$t_{REC\ (R/W)}$		200		

(V_{DD} = 5V ± 0.5V)

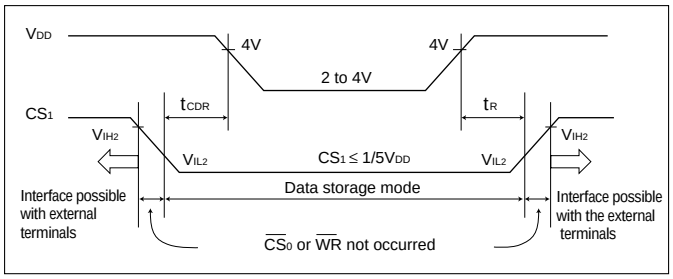
Write mode (with ALE)



Read mode (with ALE)



Data holding timing



Block diagram