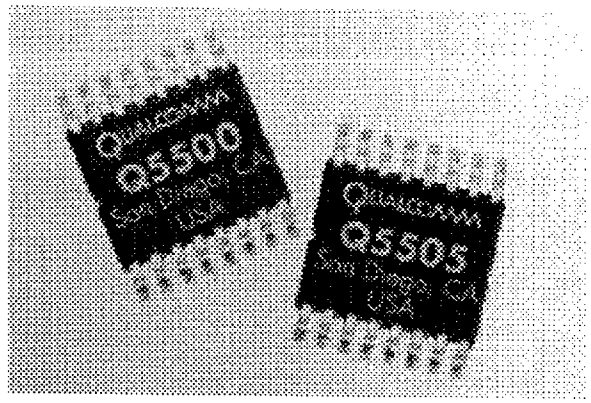
Q5500 IF RECEIVE AGC AMPLIFIER/

Q5505 IF TRANSMIT AGC AMPLIFIER



FEATURES

Q5500 FEATURES

- Supports Dual Mode Operation
- Single +3.6 V Power Supply
- Enhanced Performance over Temperature and Supply Voltage
- -45 to +45 dB Gain Control Range
- 10 MHz to 300 MHz Operation
- Low Power Consumption
- Silicon BiCMOS Process

Q5505 FEATURES

- Supports Dual Mode Operation
- Single +3.6 V Power Supply
- Enhanced Performance over Temperature and Supply Voltage
- -45 to +40 dB Gain Control Range
- 10 MHz to 250 MHz Operation
- Silicon BiCMOS Process

APPLICATIONS

- Digital Cellular Systems (dual-mode CDMA/FDM or TDMA/FDM)
- Analog Cellular Systems (AMPS, TACS)
- Analog and Digital Cordless Telephones
- Wireless Data Systems (WAN/LAN)
- Personal Communicators
- Specialized Mobile Radios (SMR)
- General Purpose Voltage-variable Linear IF Amplifier/Attenuator

GENERAL DESCRIPTION

The Q5500 Receive (Rx) and Q5505 Transmit (Tx) Variable Gain Amplifiers (VGA) are designed specifically for the receive and transmit section, respectively, of dual-mode CDMA/FM cellular applications. They provide variable gain control to IF signals with extremely wide dynamic range requirements. Noise Figure (NF), Third Order Intercept (IP3) and other specifications are designed to be compatible with the IS-95 Standard for CDMA cellular communications and remain remarkably consistent over temperature and supply voltage fluctuation. In such a dual-mode system, the Rx and Tx VGAs handle a narrowband frequency range for the IF signal processing. The Q5500 and Q5505, however, are also quite suitable for variable gain operation across a broadband frequency range. These devices can provide linear gain control for IF frequencies up to 300 MHz in general purpose Automatic Gain Control (AGC) amplifier loops. The VGAs maintain consistent NF and IP3 performance in an AGC system because these parameters exhibit low sensitivity to temperature variation. A generic system implementation for the Q5500 and Q5505 VGAs are shown in Figure 1. The differential inputs and outputs of the Q5500 and Q5505 allow a direct connection to differential downconverters/upconverters and discrete or SAW bandpass filters. Differential signals in these circuit elements reduce the effects of common-mode noise. The Q5500 and Q5505 are fabricated using a silicon BiCMOS process, operate from a single +3.6 VDC supply and come packaged in a standard 16-pin Shrink Small Outline Package (SSOP).

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Figure 1a. Generic Receive AGC Block Diagram with Q5500

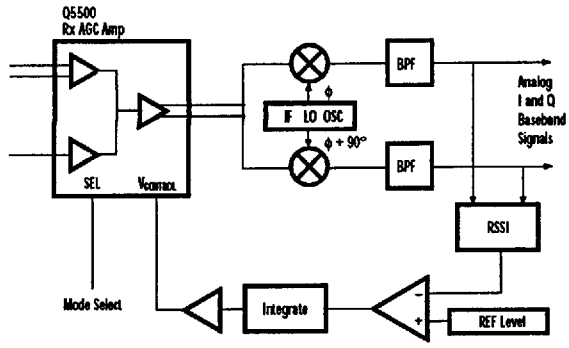
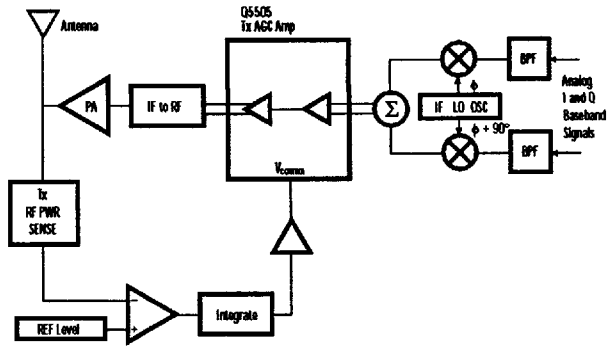


Figure 1b. Generic Transmit AGC Block Diagram with Q5505



Q5500 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent and functional damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond the min/max ranges indicated in the operational sections of this specification is not implied. Exposure exceeding absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Q5500 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T_{STO}	-55	+150	°C	
Junction Temperature	T_J	-55	+150	°C	
Supply Voltage (Relative to GND)	V_{CC}		+7.0	V	
Continuous RF Input Power			-10	dBm	
DC Voltage on any Non RF Input Pin (Relative to GND)	V_{IN}	-0.5	V_{CC} + 0.5	V	
Latchup Insensitivity	I_{TRIG}	±200		mA	1
ESD Protection	V_{ESD}	±500		V	2

NOTES:

1. Method meets the intent of JEDEC STD 17 Publication and is the maximum allowable current flow through the input and output protection diodes.
2. Method meets the intent of MIL-STD-883. Method 3015.

Table 2 Q5500 Operating Range

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature (Case)	T_C	-30	+80	°C
Operating Voltage (Relative to GND)	V_{CC}	+3.42	+3.78	V

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Table 3. Q5500 DC Electrical Parameters

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Select Input High Input Voltage	I_{CC}	3.4		V	
Select Input Low Input Voltage	V_{IL}		0.5	V	
Select Input High Input Current	V_{IH}		+100	µA	5
Select Input Low Input Current	I_{IL}	-50		µA	6
Supply Current (CDMA Mode)	I_{CC}		15	mA	
Supply Current (FM Mode)	I_{CC}		15	mA	

Table 4. Q5500 AC Electrical Parameters

PARAMETER		VALUE	NOTES
RX AGC Frequency		85.38 MHz and 210.38 MHz	
Gain Flatness (± 630 kHz)		±0.25 dB	
Gain		$V_{CONTROL}$ = 0.1 V, G< -45 dB $V_{CONTROL}$ = 3.0 V, G> 45 dB	1, 3, 6
Gain Slope		60 dB/V Maximum 20 dB/V Minimum	1, 3, 8
Gain Slope Linearity (Over any 6 dB Gain Segment)		± 3.0 dB/V	8
Gain Control Pin Input Current		< 0.1 mA @ $V_{CONTROL}$ = (0.1 - 3.0) V < 50 pF Capacitive	
NF For CDMA and FM		Figure 7a - 7f, Table 5	1, 3, 7
IIP3 For CDMA and FM		Figures 8a and 8b Respectively	1, 2, 3, 7,9
Desense (Change in Small Signal Gain)	Max Gain (G=45 dB) Input Jammer Power = -57 dBm Jammer Offset 900 kHz	FM Mode Δ G < 0.45 dB	
		CDMA Mode Δ G < 0.75 dB	
P_{1dB}	CDMA Input Min Gain (G=-45 dB)	-15.5 dBm ≤ P_{1dB}	
	FM Input (G < -27 dB)	-22.0 dBm ≤ P_{1dB}	
Isolation AGC-1 Between AGC-2		30 dB	1
CDMA Input Impedance (Differential)		1K Ω ± 15%, < 1 pF Capacitive	3
FM Input Impedance (Single Ended)		865 Ω ± 15%, < 1.5 pF Capacitive	3
Output Impedance		> 5 kΩ, < 1 pF Capacitive	3
Stability		Over Full AGC Range With Source and Load VSWR 10:1 All Angles Spurious < -70dBm	

NOTES:

1. $Z_S = Z_L = 250\ \Omega$. Manufacturer to recommend Z_S and Z_L.
2. IIP3 = IMR3/2 + P_{IN}, where IIP3 is the input third order intercept, in dBm, IMR3 is the third order intermodulation product rejection in dB, and P_{IN} is the sum power of the two input tones.
3. See Figures 2a, 2b and 2c.
4. $V_{IH} = V_{CC} = 3.78V$.
5. $V_{IL} = 0V$, $V_{CC} = 3.78$ V.
6. P_{OUT} = -57 dBm, or $P_{IN\ MAX}$ = -12 dBm if in compression.
7. Over Specified Gain Range of -45 dB to +45 dB.
8. In Linear Operating Range.
9. P_{IN} total maximum = -23 dBm, and P_{OUT} total maximum = -57 dBm.

Figure 2a. Definition of FM Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5500

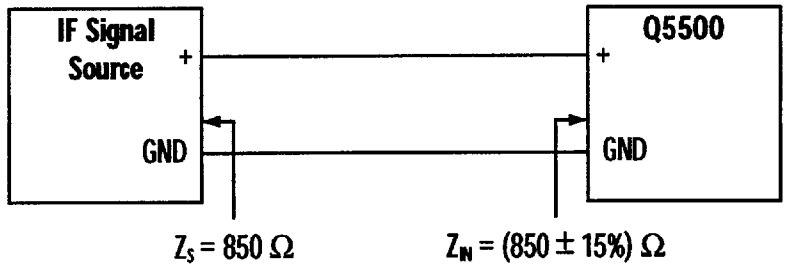


Figure 2b. Definition of CDMA Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5500

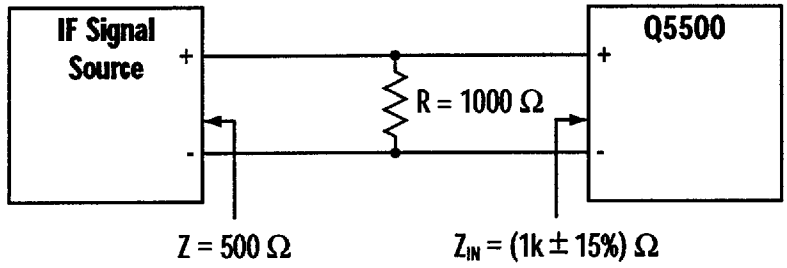
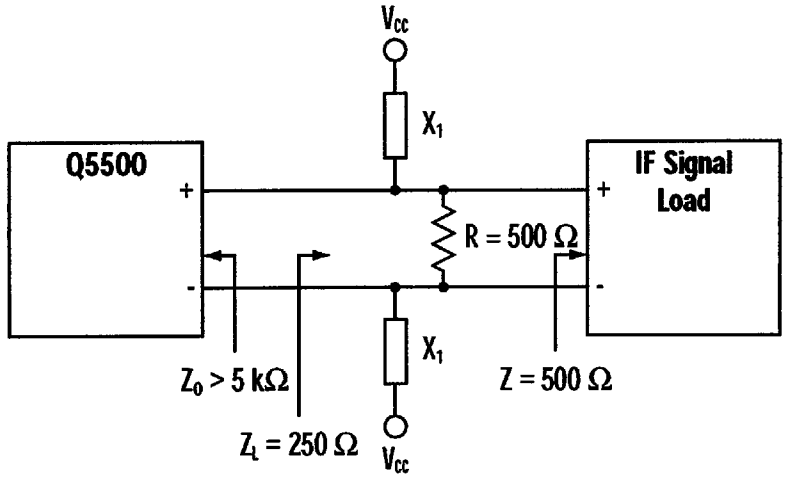


Figure 2c. Definition of Load Impedance, Z_L, and Output Impedance, Z_O, for Q5500



Note: X_1 can be a resistor or an inductor.
If it is a resistor, X_1 = 250 Ω and the 500 Ω resistor will not be used.
If it is an inductor, L = 2.7 µH.

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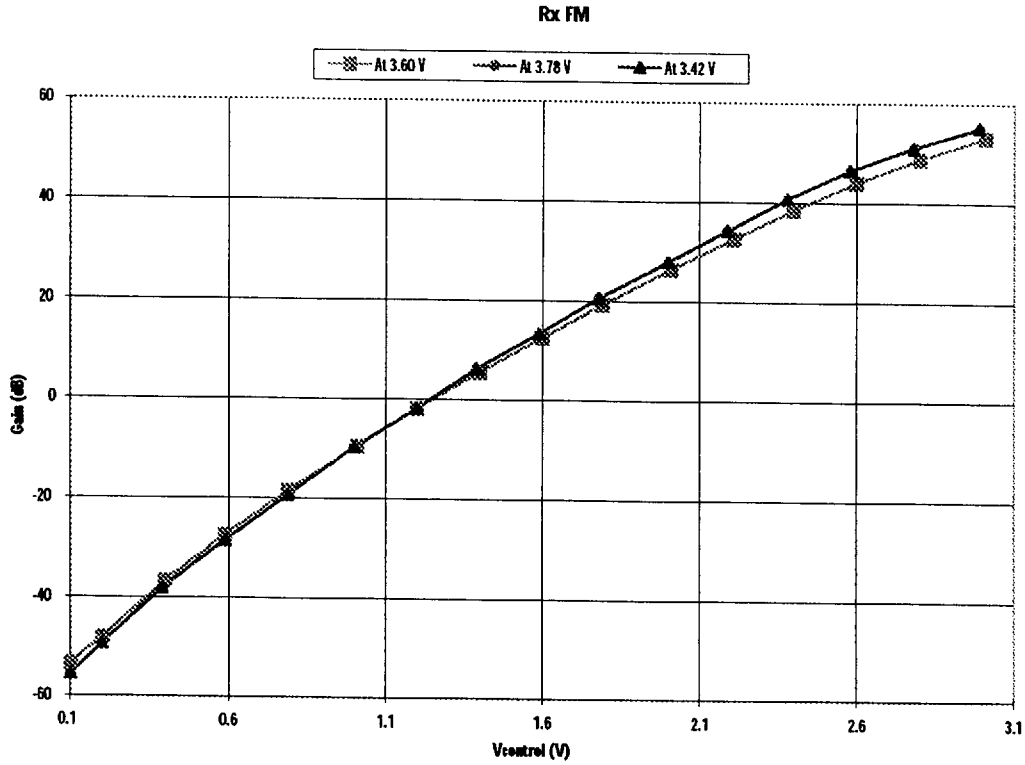
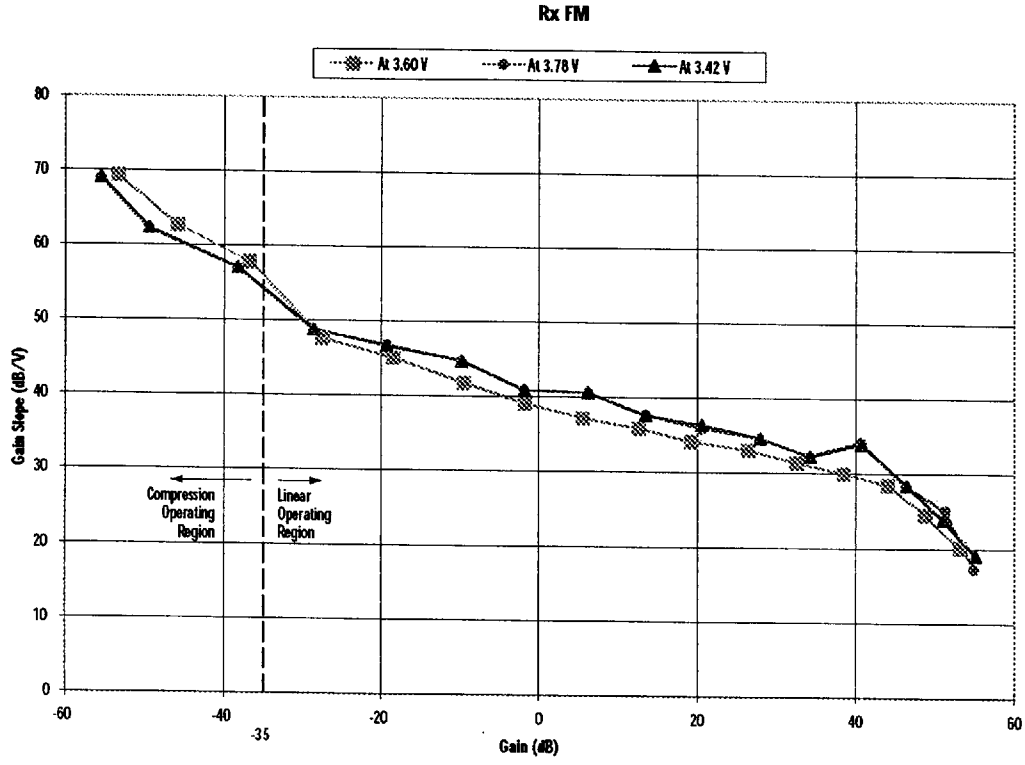
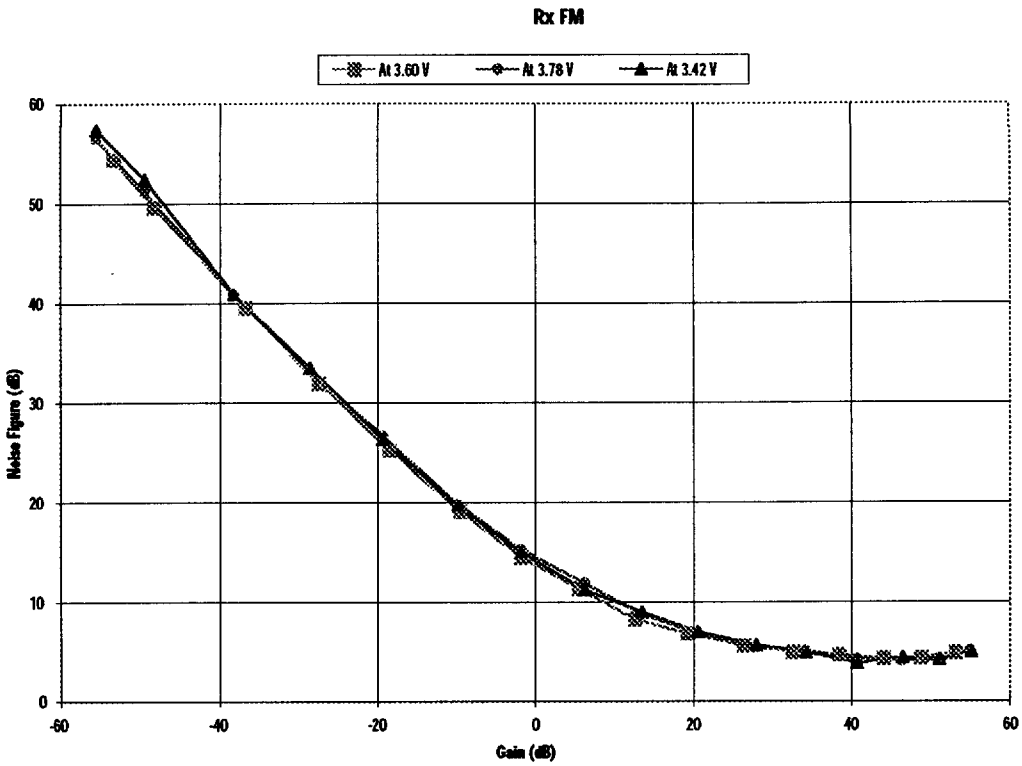
Figure 3a-e. Typical Q5500 Performance Characteristics Over Supply Voltage Range, FM Mode



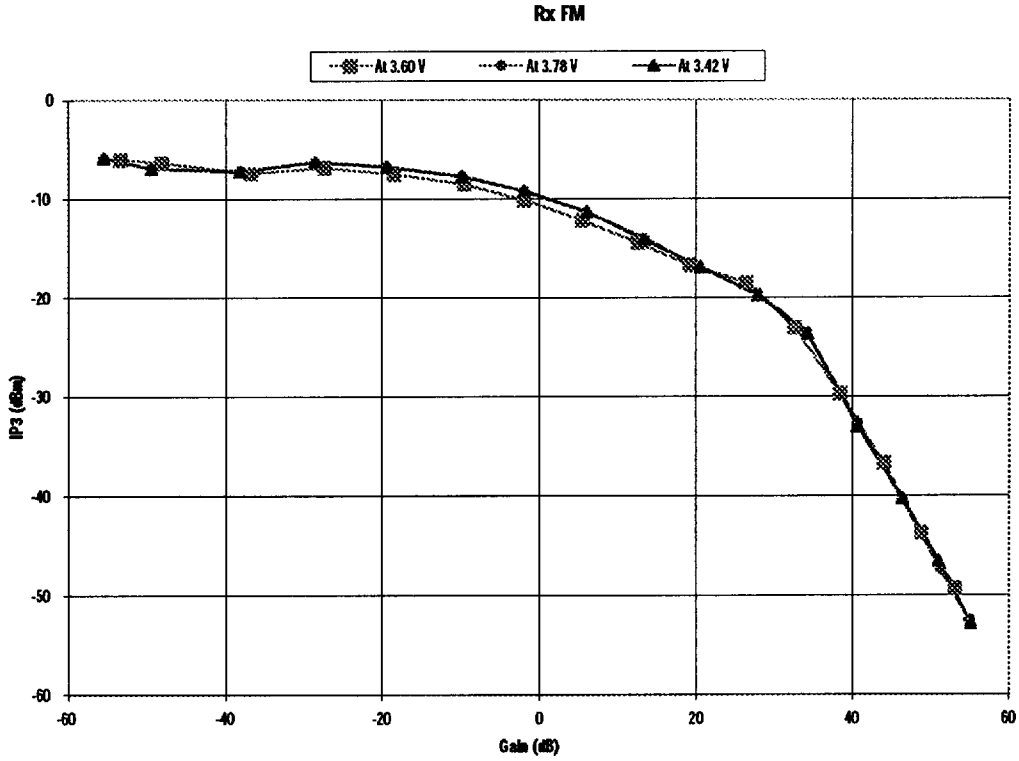
a. Gain vs. Control Voltage



b. Gain Slope vs. Gain



c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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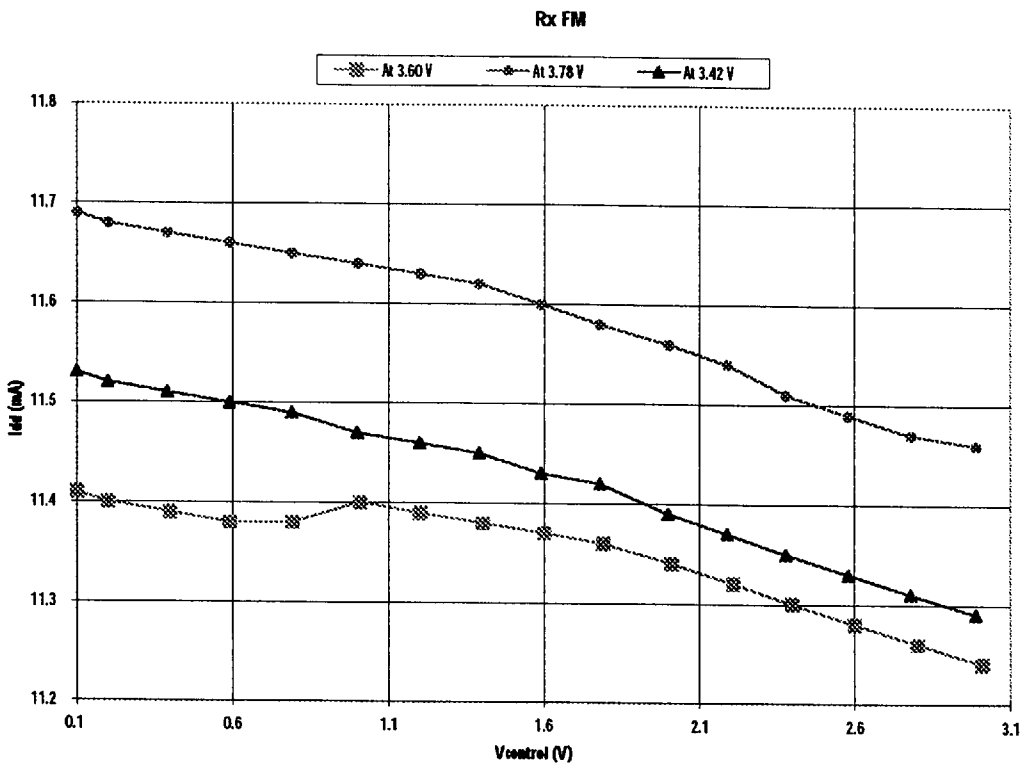
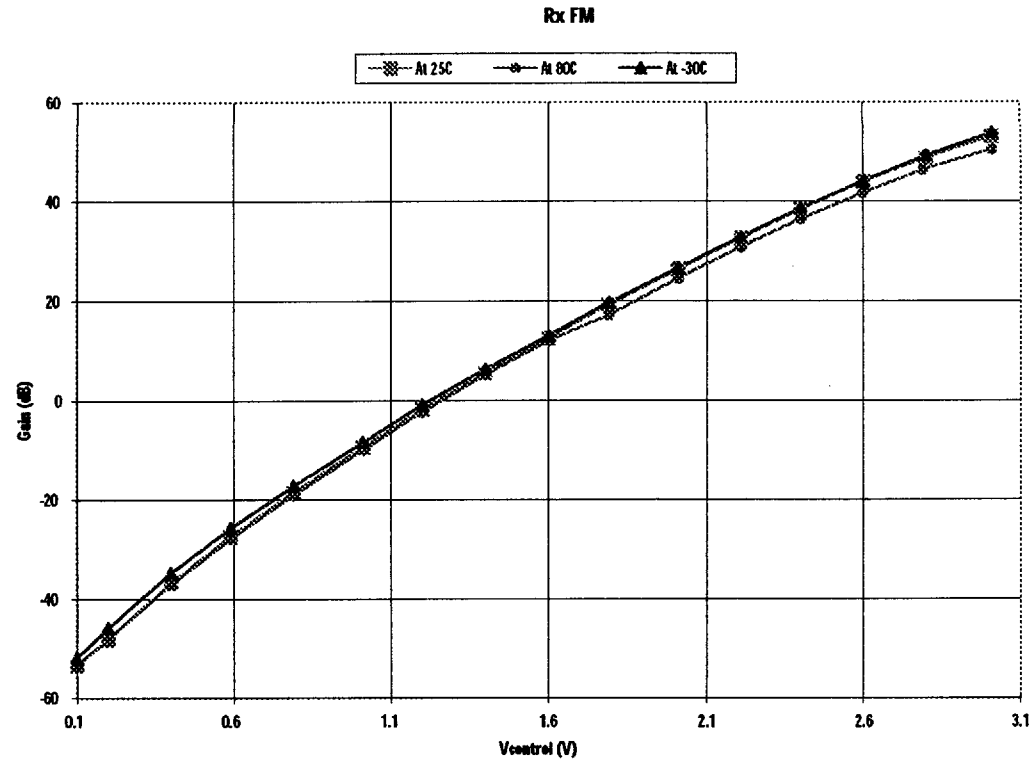
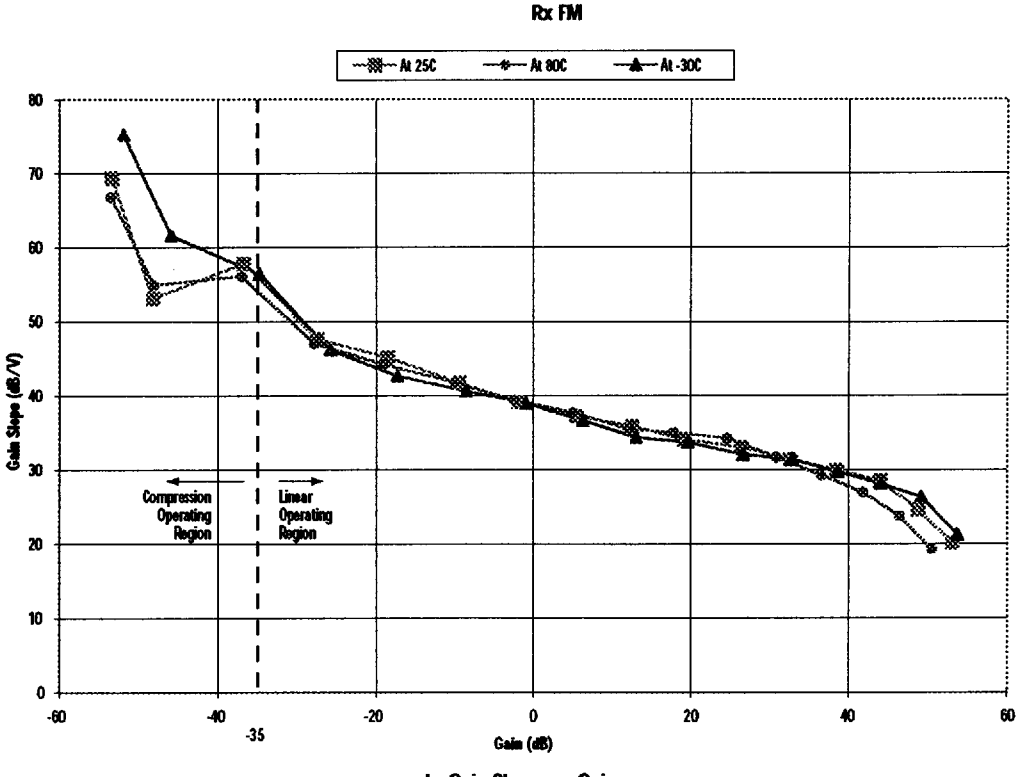


e. Supply Current vs. Control Voltage

Figure 4a-e. Typical Q5500 Performance Characteristics Over Operating Temperature Range, FM Mode



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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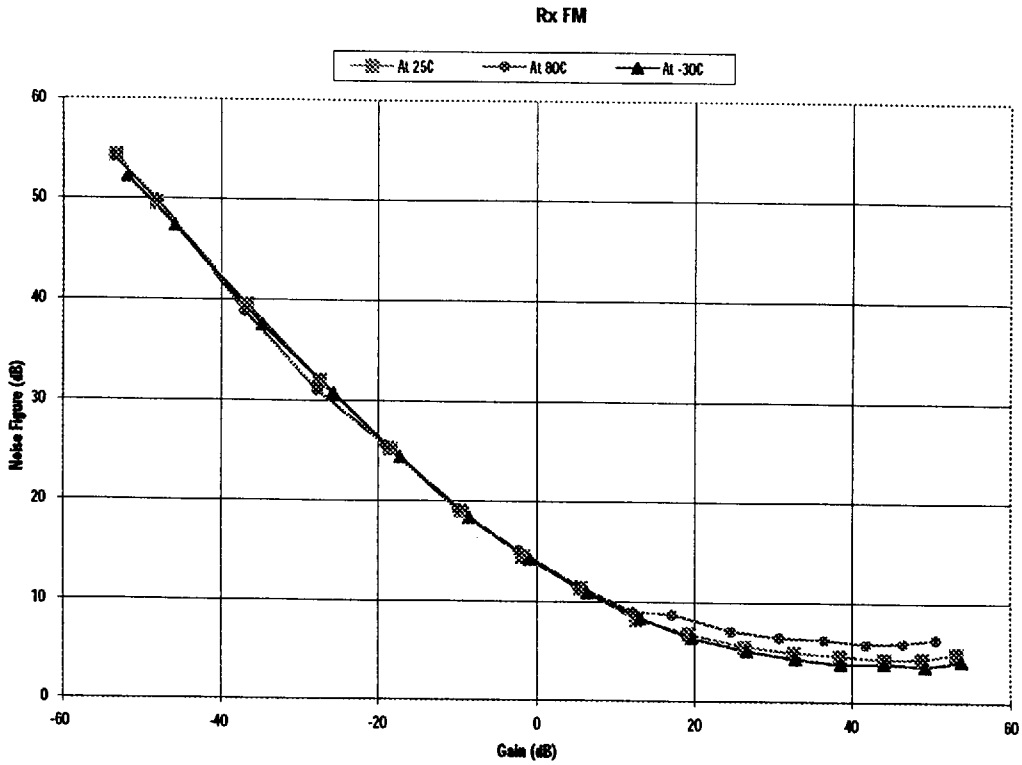
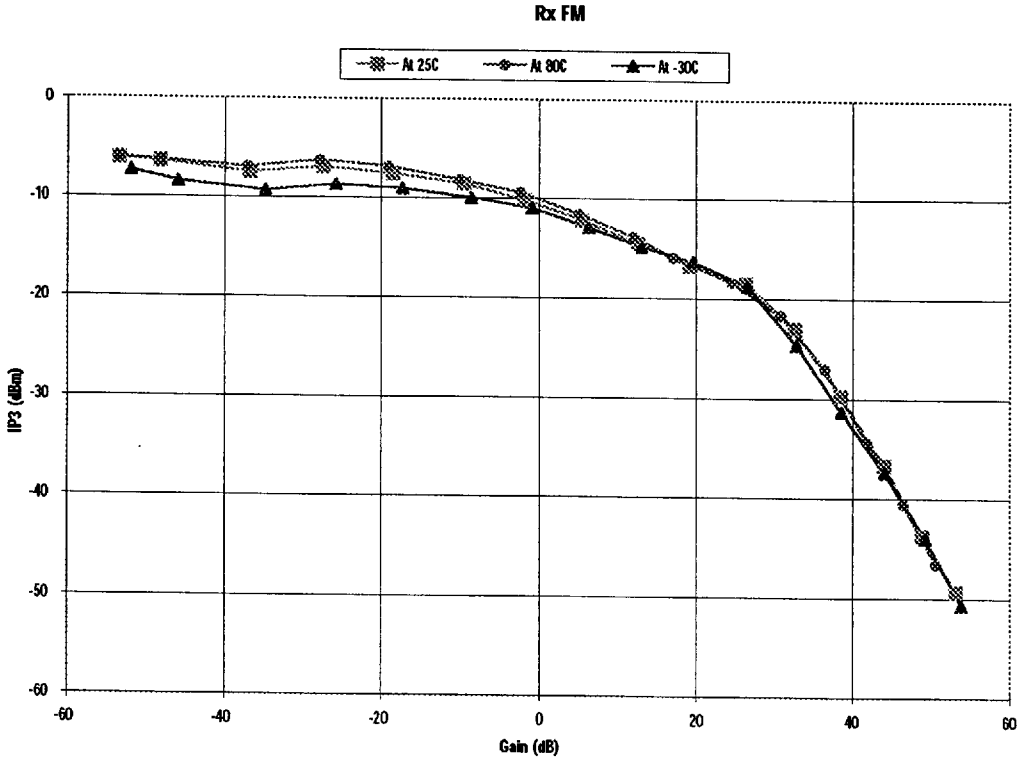
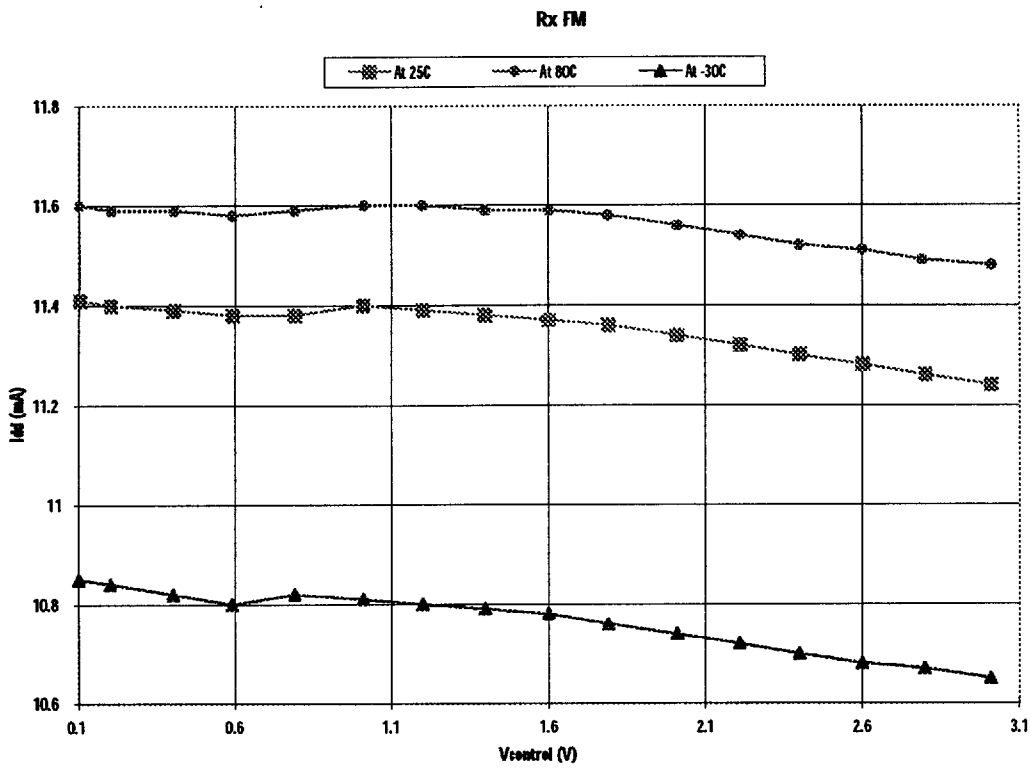


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain



e. Supply Current vs. Control Voltage

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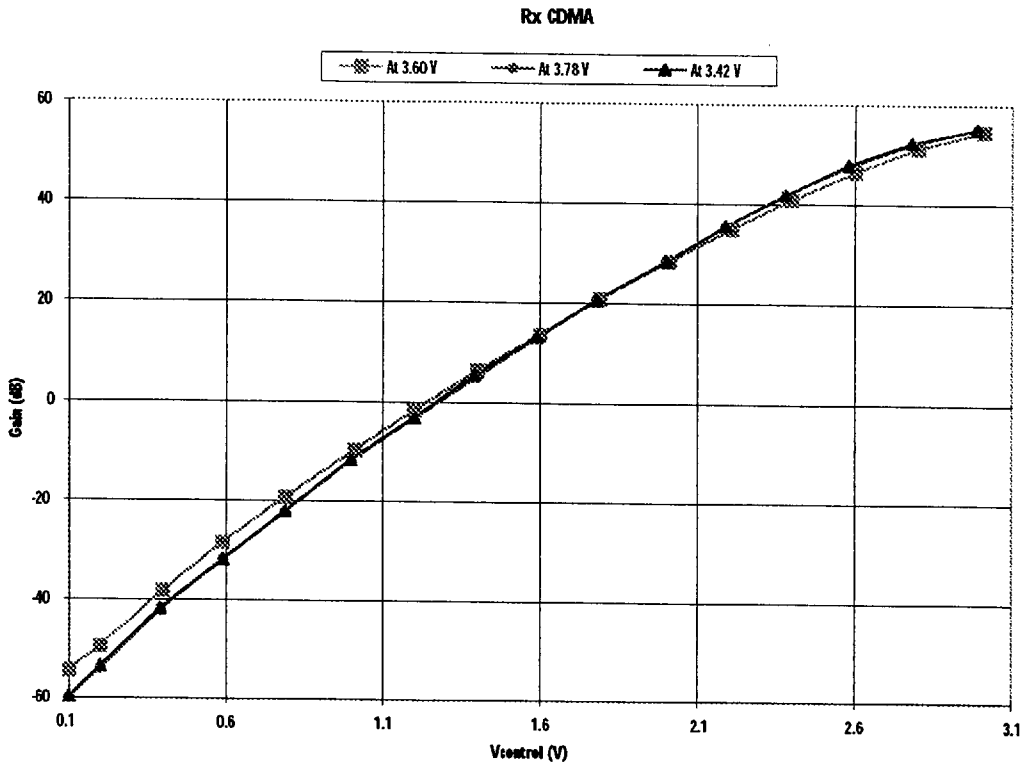
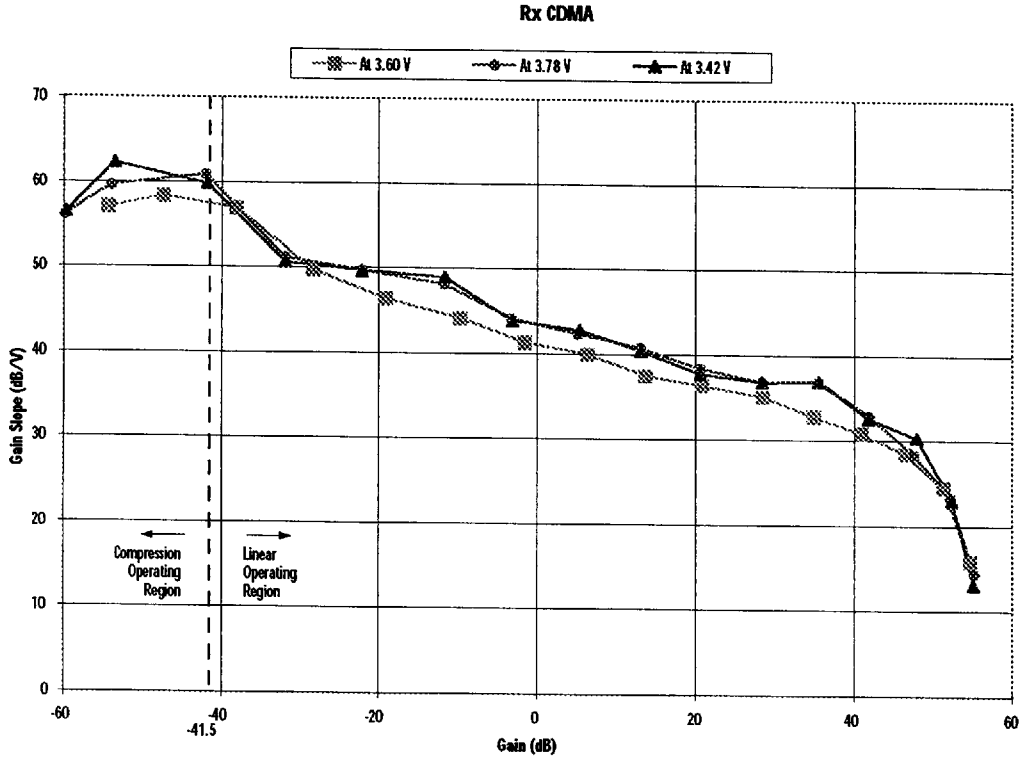
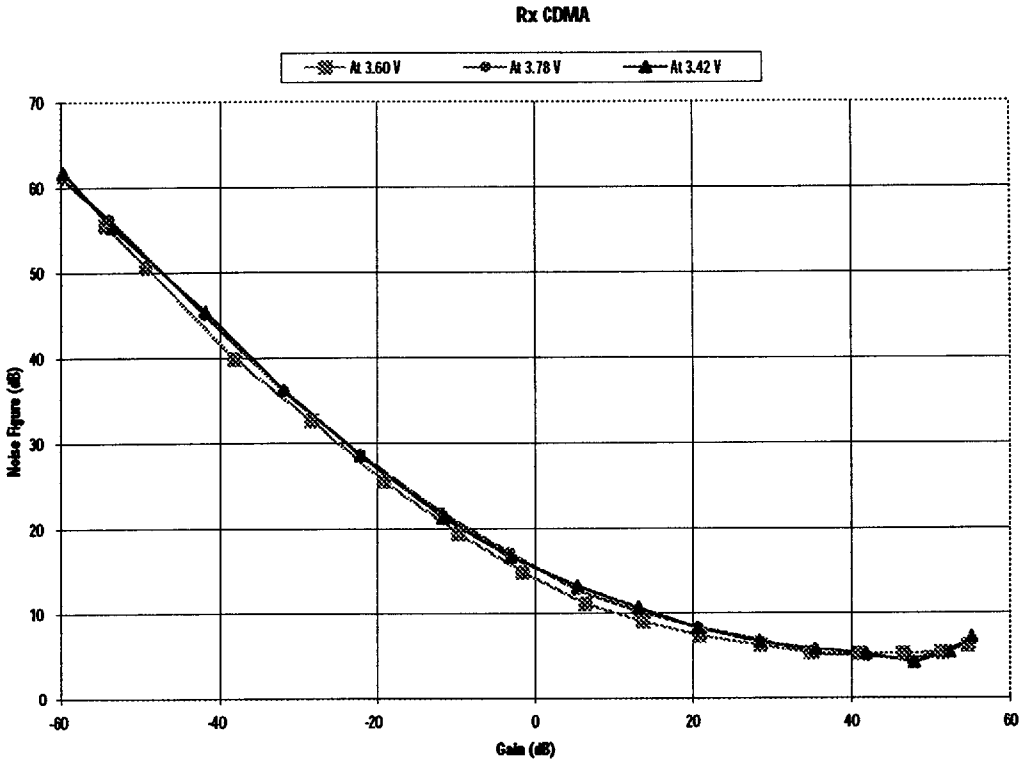
Figure 5a-e. Typical Q5500 Performance Characteristics Over Supply Voltage Range, CDMA Mode



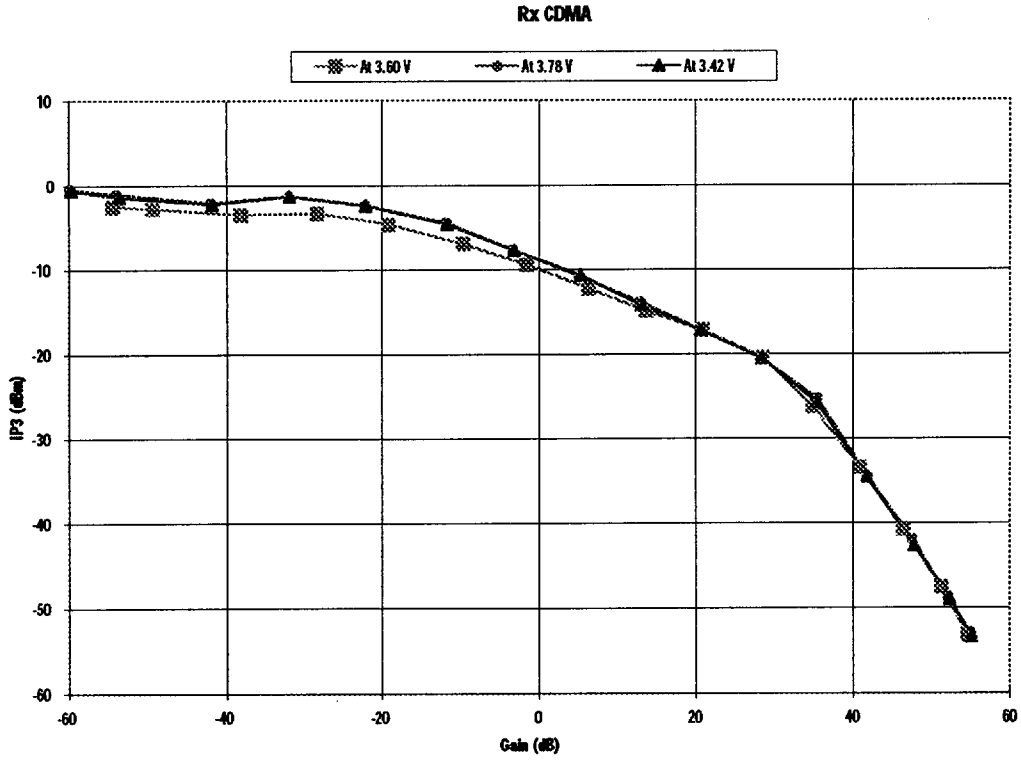
a. Gain vs. Control Voltage



b. Gain Slope vs. Gain



c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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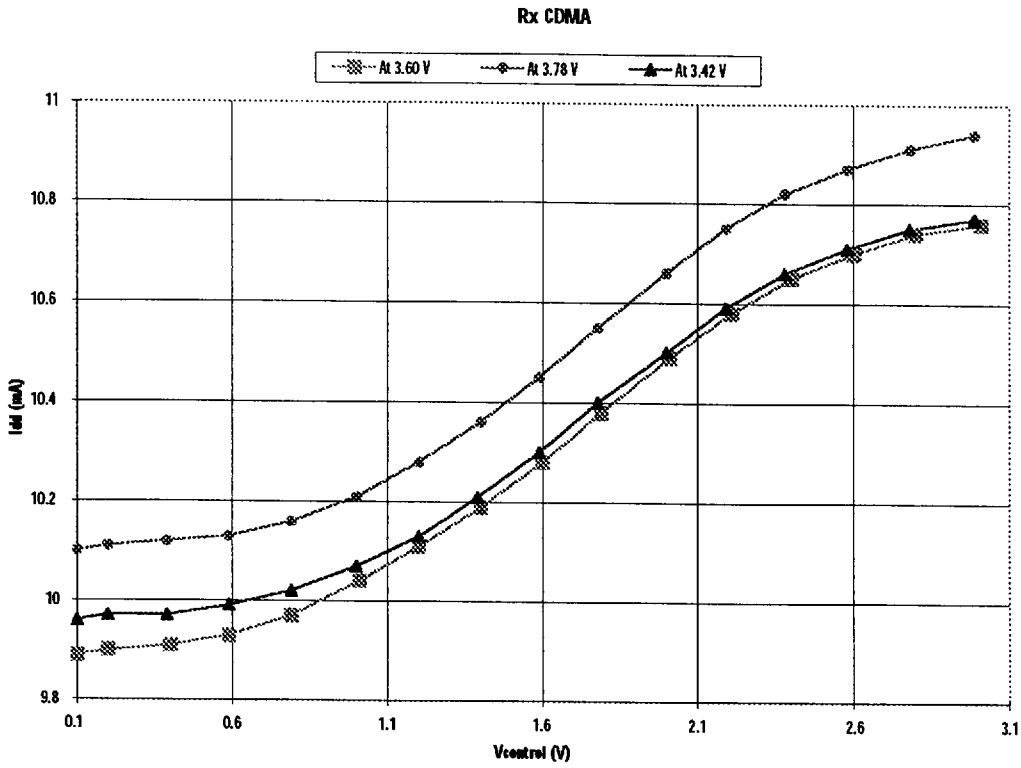
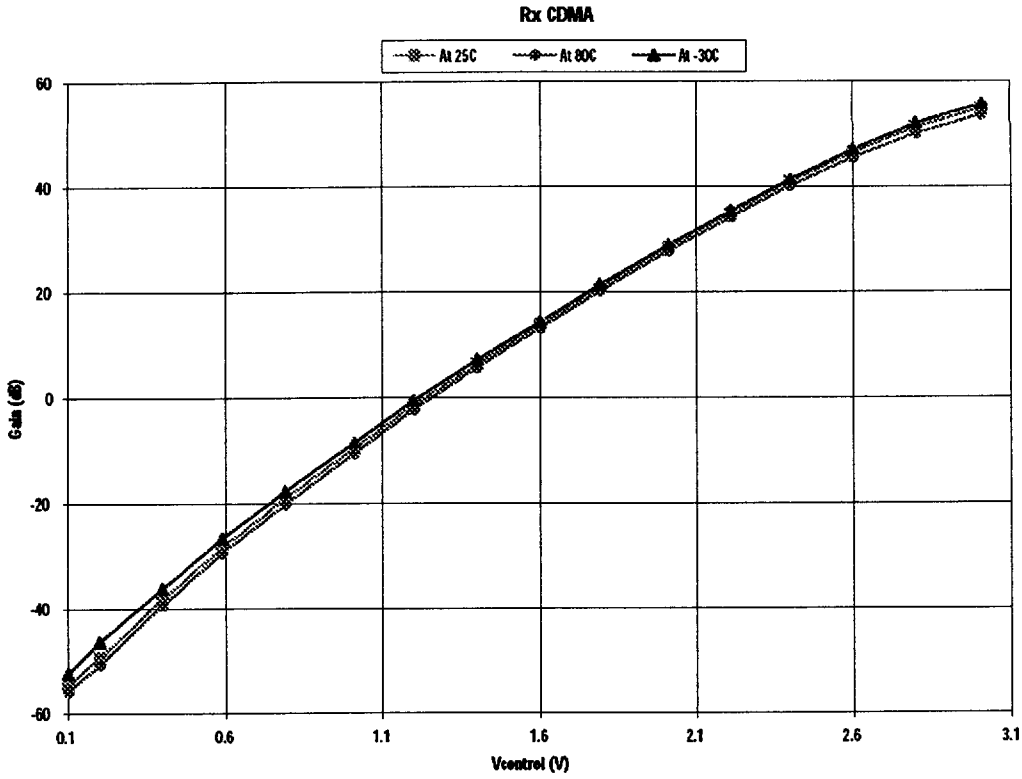
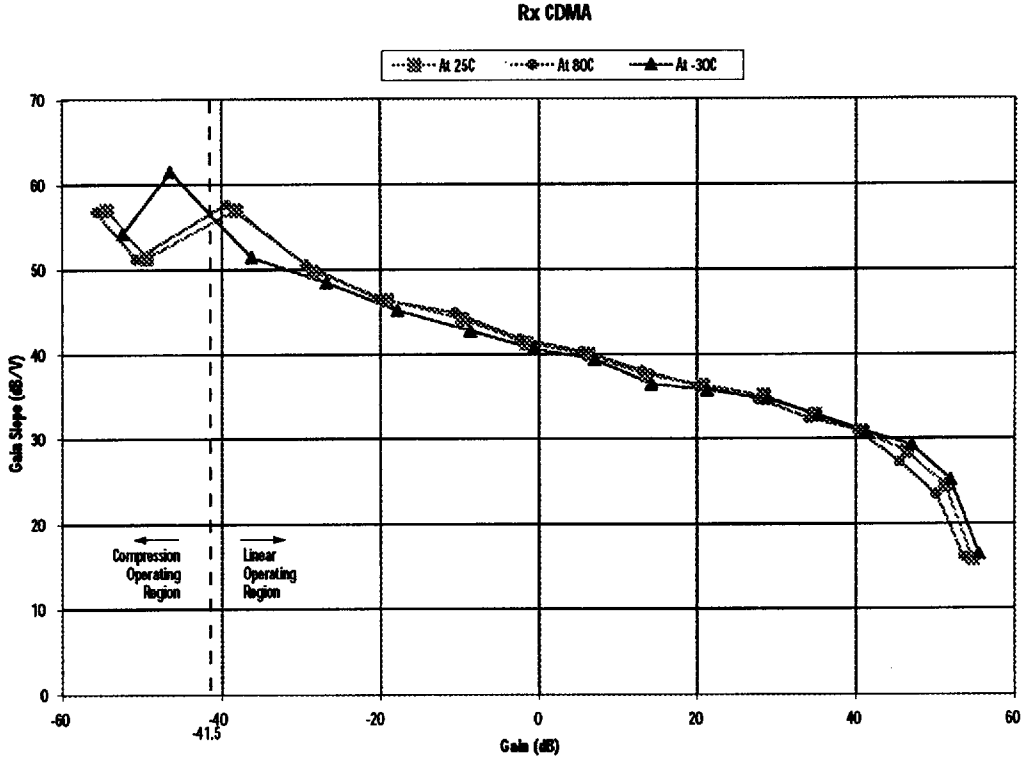


e. Supply Current vs. Control Voltage

Figure 6a-e. Typical Q5500 Performance Characteristics Over Operating Temperature Range, CDMA Mode



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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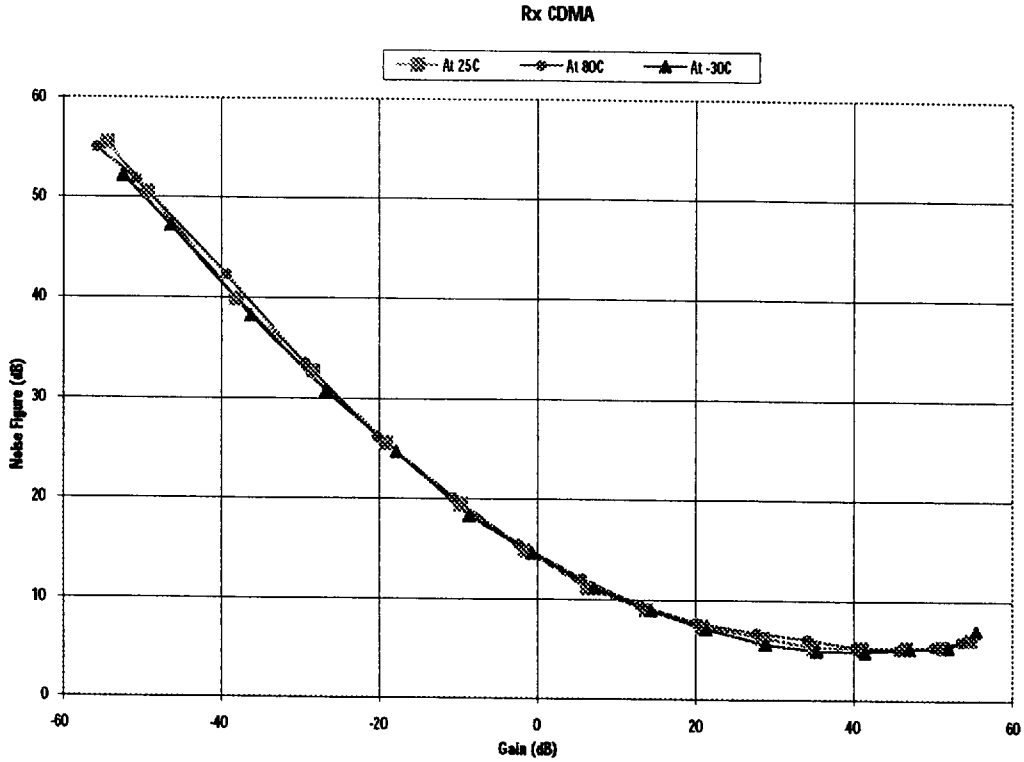
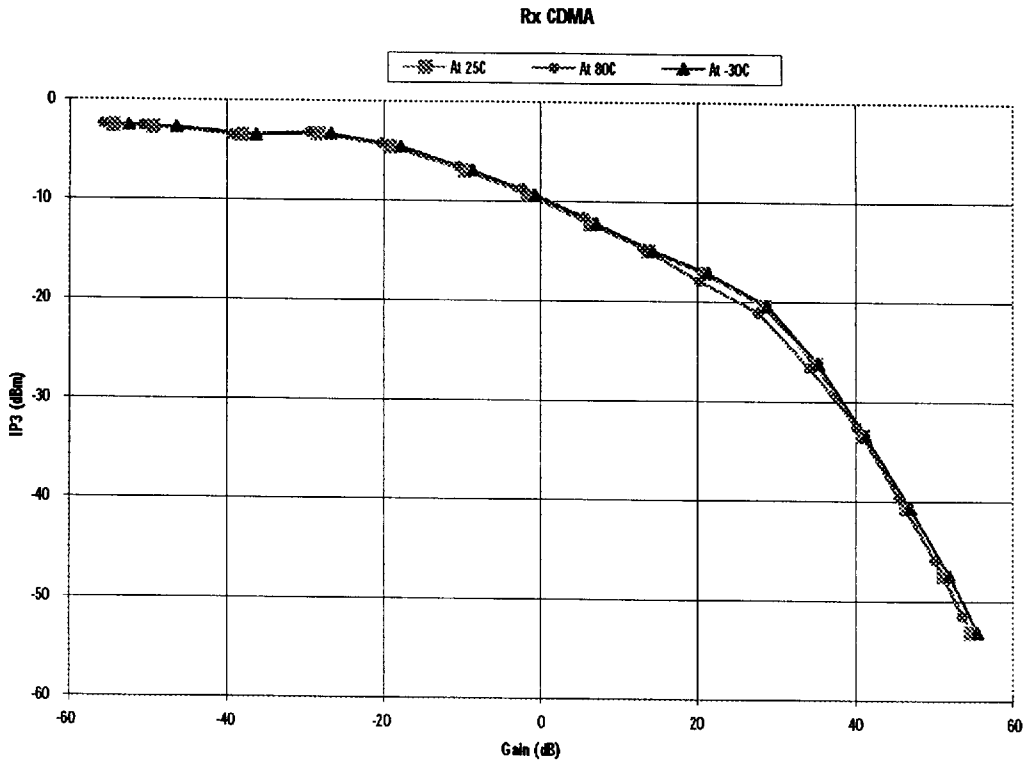
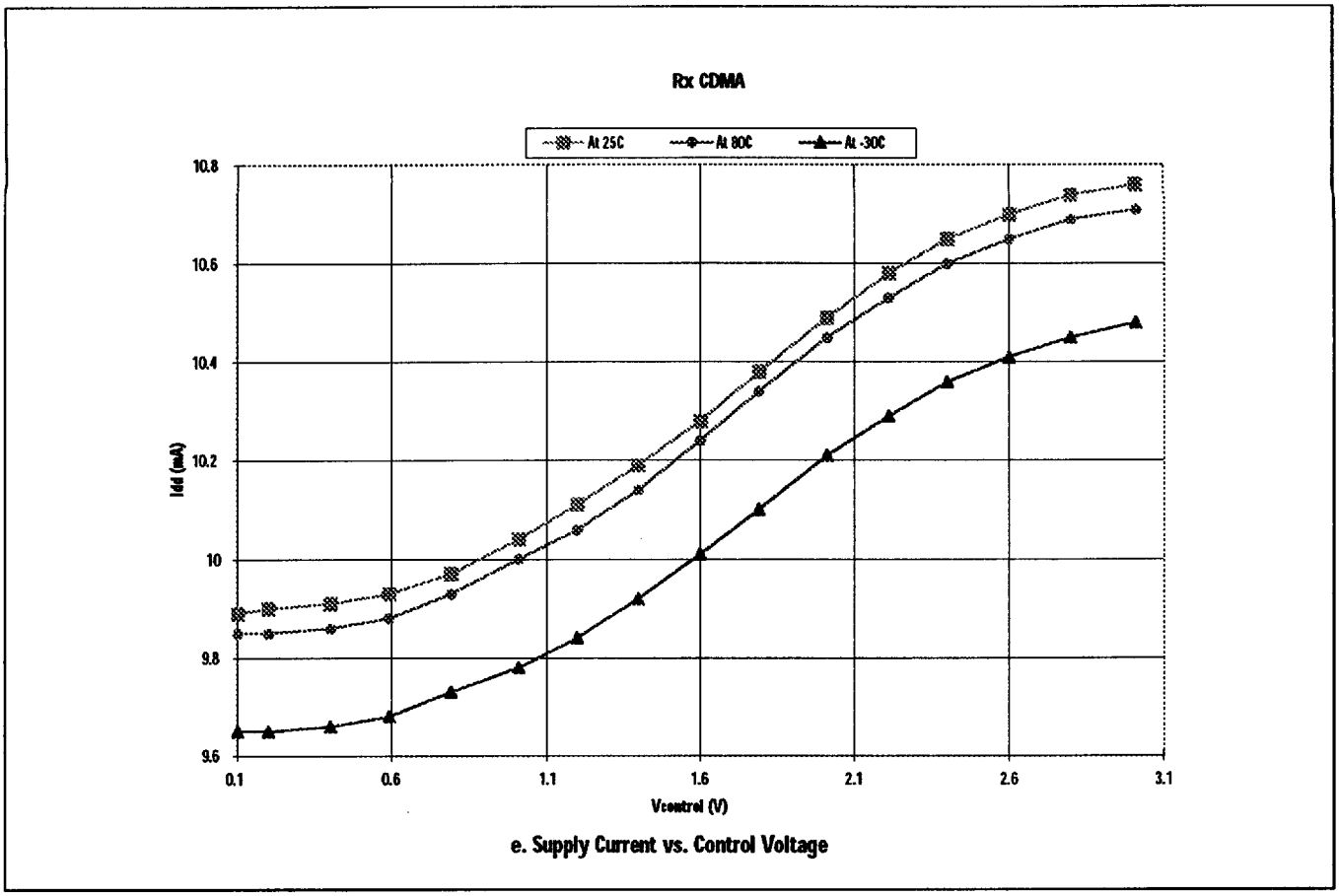


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain



e. Supply Current vs. Control Voltage

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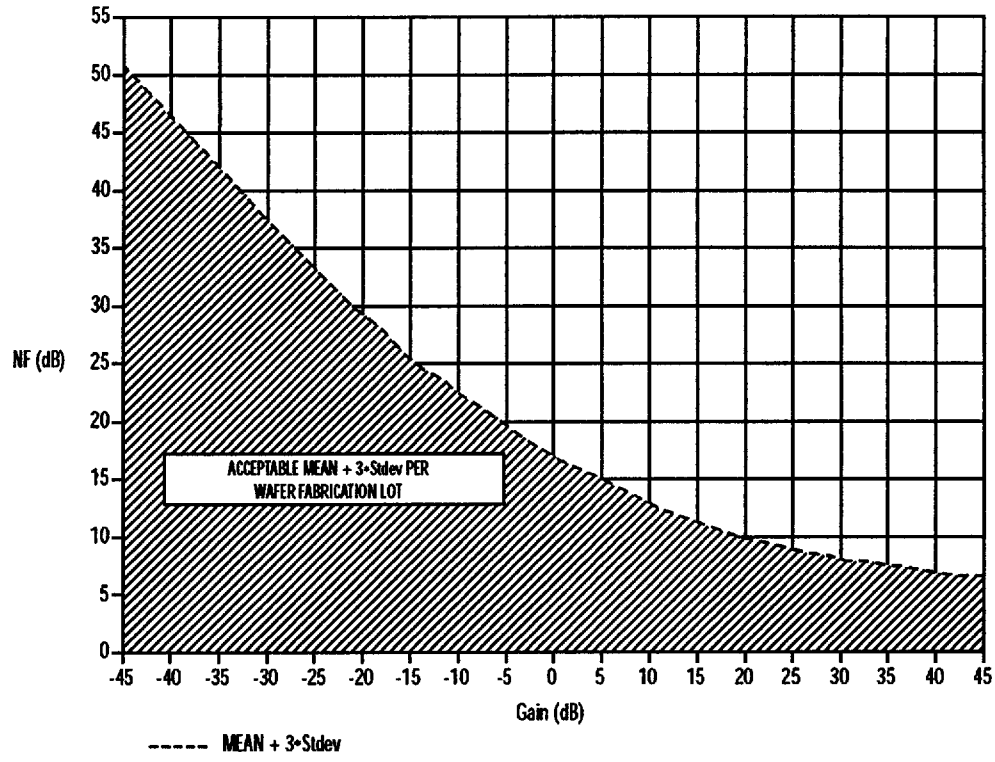
Table 5. Q5500 Noise Figure Standard Deviation X3

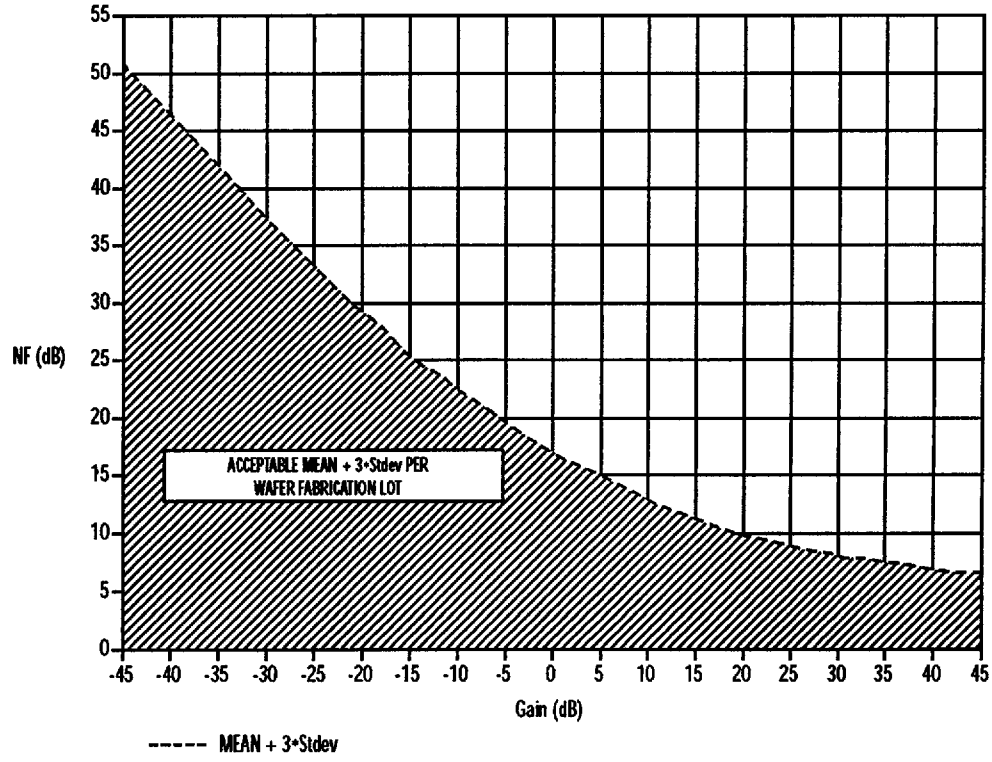
Gain (dB)	FM Mode Standard Deviation X3	CDMA Mode Standard Deviation X3
-45	2.85	3
-40	2.55	2.6
-35	2.55	2.6
-30	2	2.1
-25	2	2.1
-20	1.5	1.6
-15	1.5	1.6
-10	1.3	1.5
-5	1.3	1.5
0	1.2	1.3
5	1.2	1.3
10	1.2	1.1
15	1.2	1.1
20	0.9	0.8
25	0.9	0.8
30	0.55	0.55
35	0.55	0.55
40	0.4	0.4
45	0.3	0.3

Figure 7a. Q5500 CDMA Mode Noise Figure Mean + 3•Stdev@ -30C



NF Typical = -4.039092 e - 09•G^5 - 4.164094e-07•G^4 + 7.80438e-06•G^3 + 6.321204e-03•G^2 - 0.466927•G + 15.7323

Figure 7b. Q5500 CDMA Mode Noise Figure Mean + 3•Stdev@ 25C



NF Typical = -1.499369e-09•G^5 - 4.456002e-07•G^4 + 1.677515e-06•G^3 + 6.355075e-03•G^2 - 0.454722•G +15.8378

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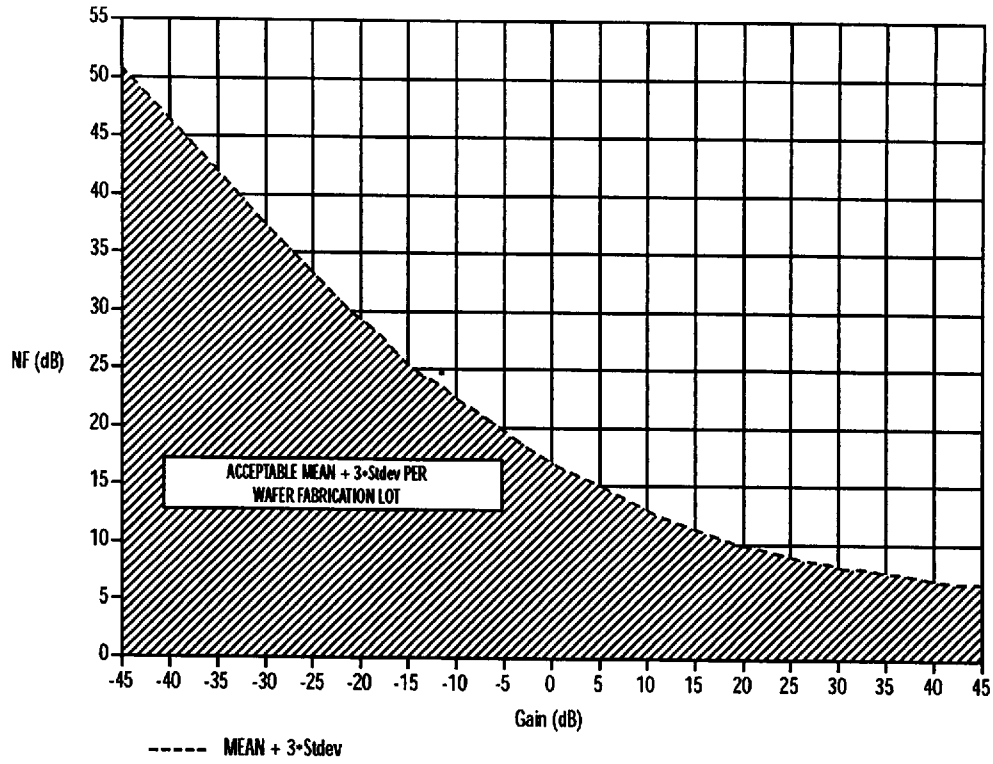
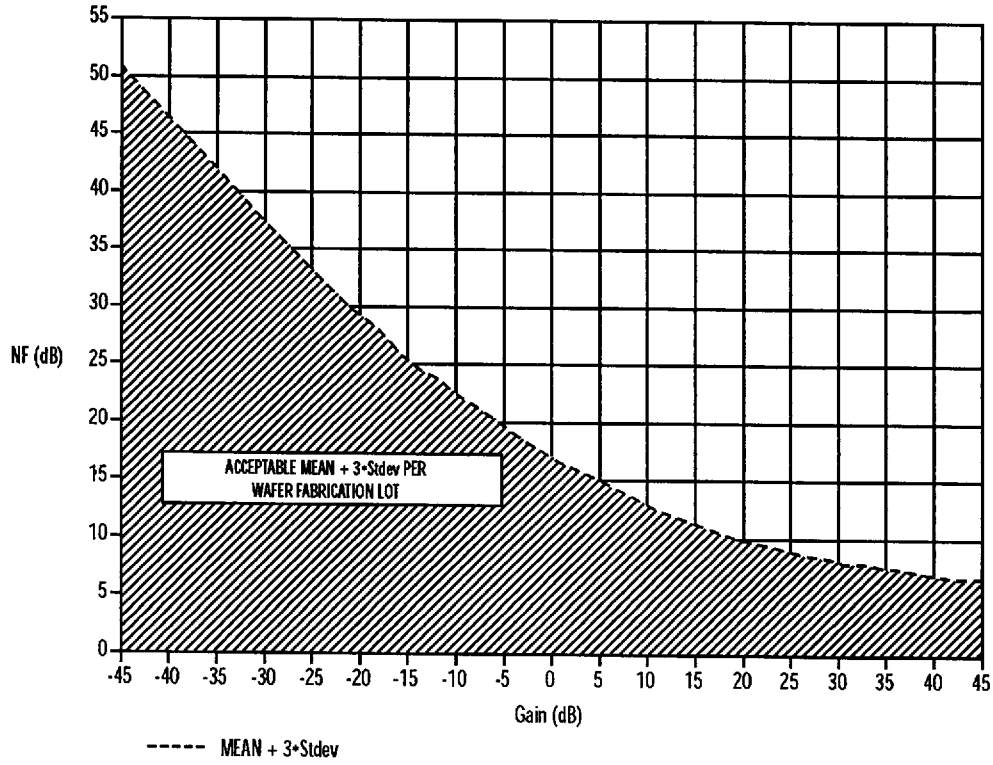
Figure 7c. Q5500 CDMA Mode Noise Figure Mean + 3•Stdev@ 80C



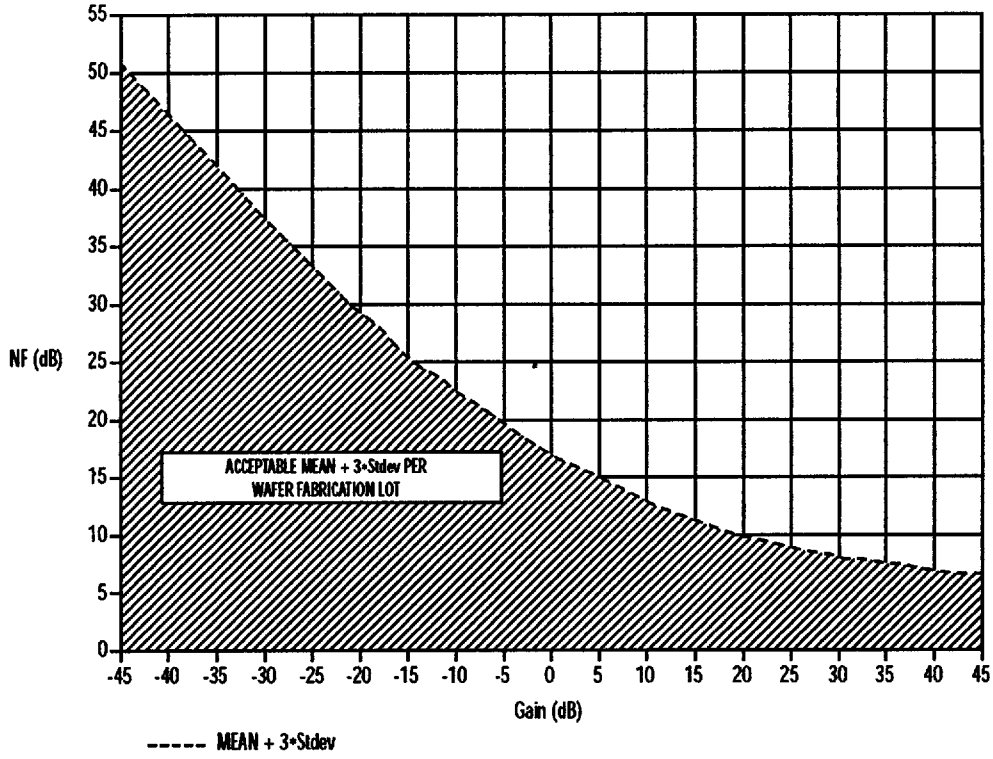
NF Typical = $4.211023e\text{-}10 \cdot G^5 - 6.676453e\text{-}07 \cdot G^4 - 7.945305e\text{-}06 \cdot G^3 + 7.236486e\text{-}03 \cdot G^2 - 0.448823 \cdot G + 16.0300$

Figure 7d. Q5500 FM Mode Noise Figure Mean + 3•Stdev@ -30C



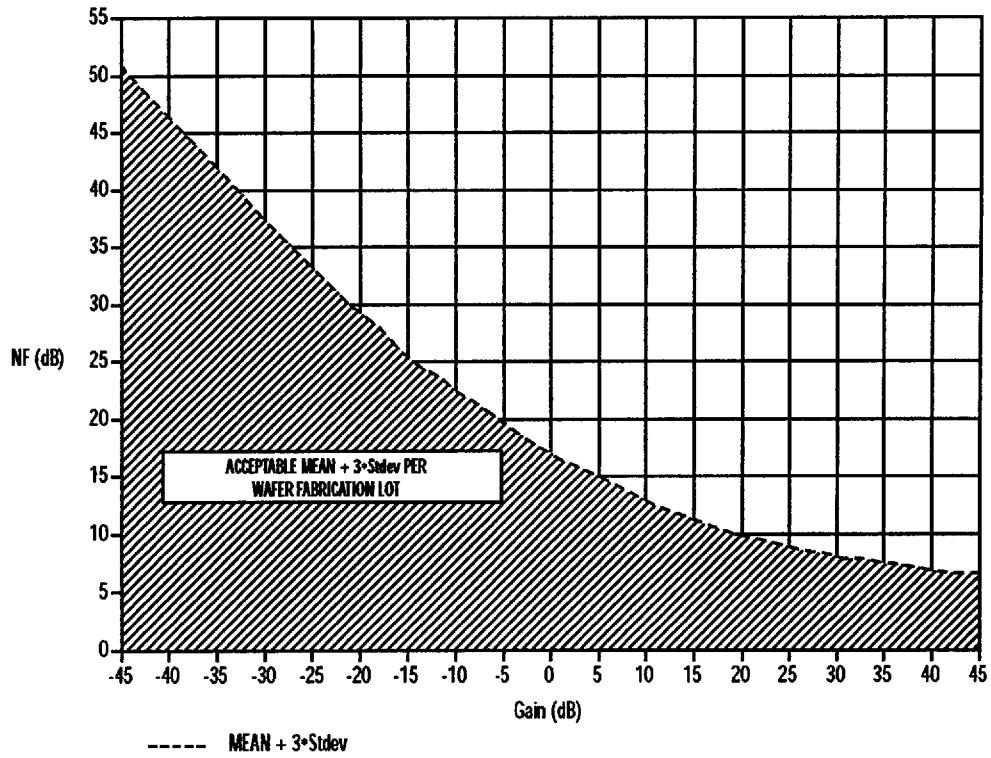
NF Typical = $-1.765908e\text{-}08 \cdot G^5 - 1.538293e\text{-}07 \cdot G^4 + 5.645998e\text{-}05 \cdot G^3 + 5.891888e\text{-}03 \cdot G^2 - 0.518637 \cdot G + 15.3817$

Figure 7e. Q5500 FM Mode Noise Figure Mean + 3•Stdev@ 25C



NF Typical = $-1.194405e\text{-}08 \cdot G^5 - 2.862301e\text{-}07 \cdot G^4 + 3.824693e\text{-}05 \cdot G^3 + 6.253457e\text{-}03 \cdot G^2 - 0.493354 \cdot G + 15.2345$

Figure 7f. Q5500 FM Mode Noise Figure Mean + 3•Stdev@ 80C



NF Typical = $-1.099614e\text{-}08 \cdot G^5 - 3.403353e\text{-}07 \cdot G^4 + 3.183561e\text{-}05 \cdot G^3 + 6.640703e\text{-}03 \cdot G^2 - 0.489305 \cdot G + 15.4513$

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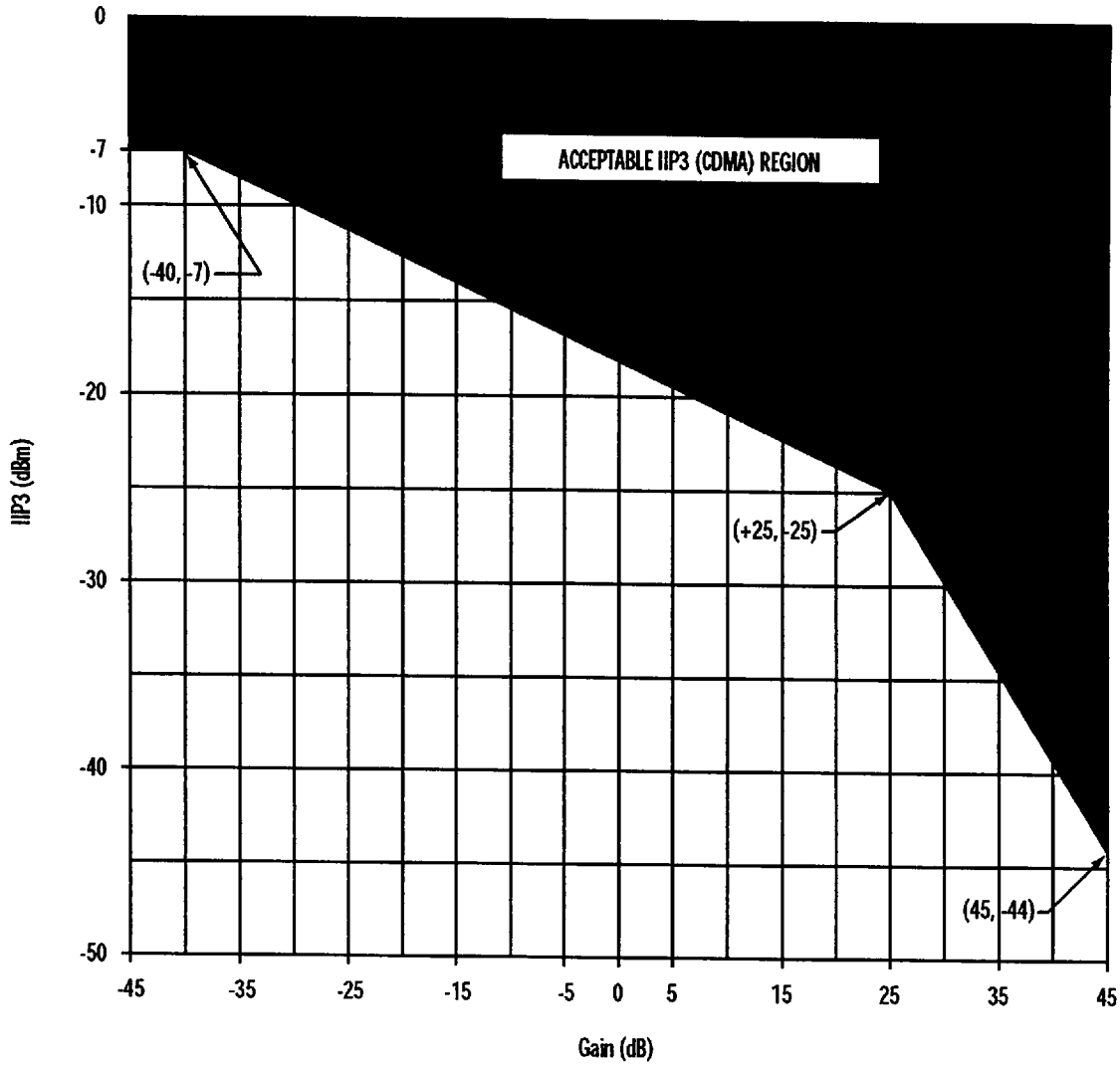
Figure 8a. Q5500 IIP3 (CDMA Mode)

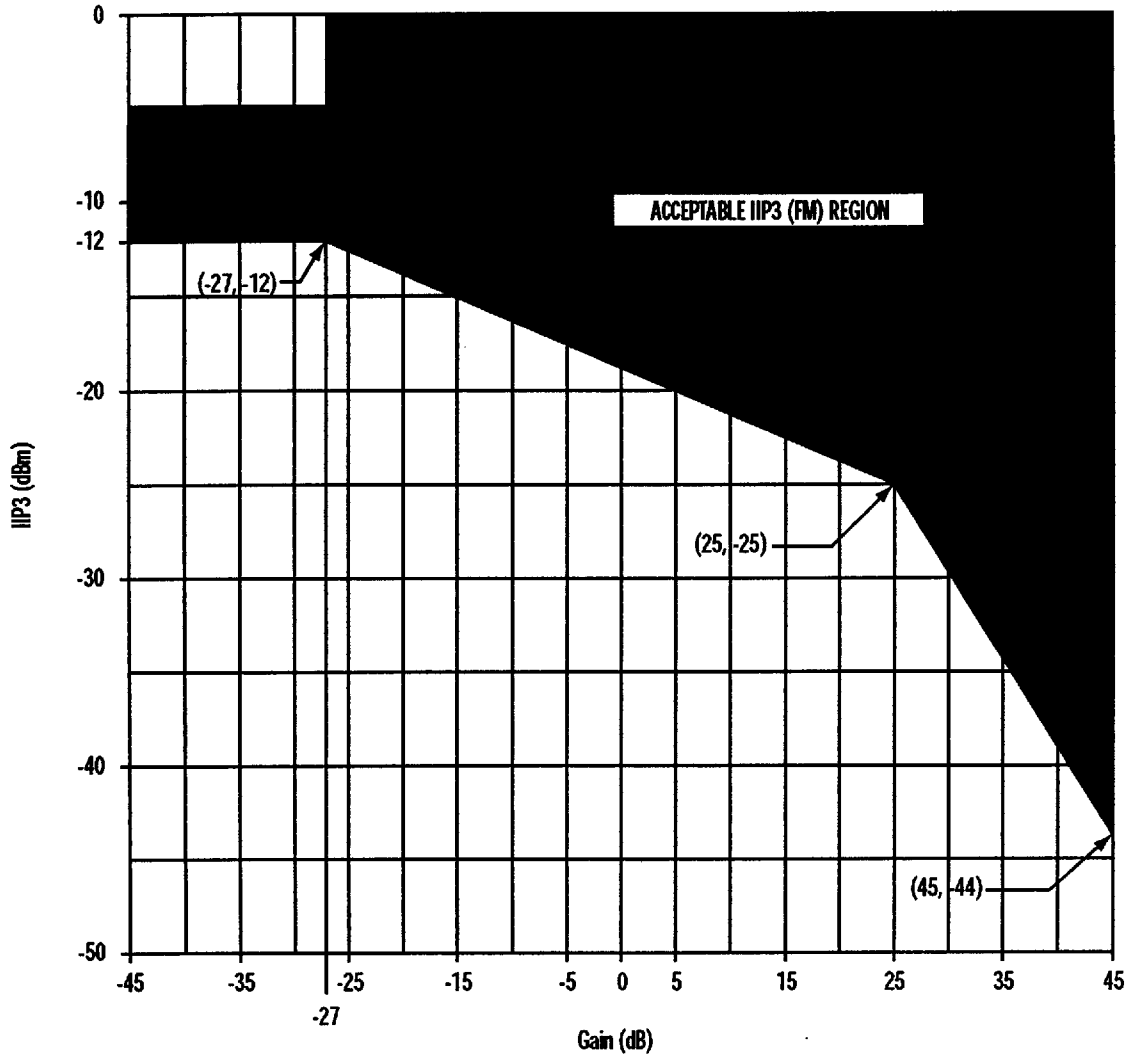


$IIP3 \geq -7$ dBm ($-45 \leq Gain \leq -40$ dB)

$IIP3 \geq -0.276923 * Gain - 18.07692$ dBm ($-40 \leq Gain \leq 25$ dB)

$IIP3 \geq -0.95 * Gain - 1.25$ dBm ($25 \leq Gain \leq 45$ dB)

Figure 8b. Q5500 IIP3 (FM Mode)



$-12 \leq -5$ dBm ($-45 \leq$ Gain ≤ -27 dB)

IIP3 $\geq -0.25 *$ Gain -18.75 dBm ($-27 <$ Gain ≤ 25 dB)

IIP3 $\geq -0.95 *$ Gain $- 1.25$ dBm ($25 <$ Gain ≤ 45 dB)

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Table 6a-g. Description of Q5500 Pin Functions

a. Hi-Gain Digital Mode Differential Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
IN +	1	Differential Input	Positive Differential Input
IN –	2	Differential Input	Negative Differential Input

b. Low-Gain Analog Mode Single Ended Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
FM IN +	4	Single Ended AC Input	Single Ended Analog Input

c. Analog Gain Control Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
$V_{CONTROL}$	16	DC Input	$V_{CONTROL}$ – Analog Gain Control Input $V_{CONTROL}$ = 0.1 V, Low Gain Rail, $V_{CONTROL}$ = 3.0 V, High Gain Rail

d. Analog/Digital Mode Select Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
SEL	7	CMOS Input	$V_{SELECT} \geq$ + 3.4 V, Digital Mode Select $V_{SELECT} \leq$ + 0.5 V, Analog Mode Select

e. Analog Differential Output Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
OUT +	10	Differential Output	Analog Positive Differential Output
OUT –	9	Differential Output	Analog Negative Differential Output

f. Unconnected Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
–	8	N/C	Unconnected Pin

g. Voltage Supply Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
V_{CC}	13, 14, 15	Power	V_{CC} Power Supply
GND	3, 6, 11, 12	Ground	Ground Connection
AC GND	5	AC Ground	Analog Ground Connection

Figure 9. Q5500 Functional Block Diagram

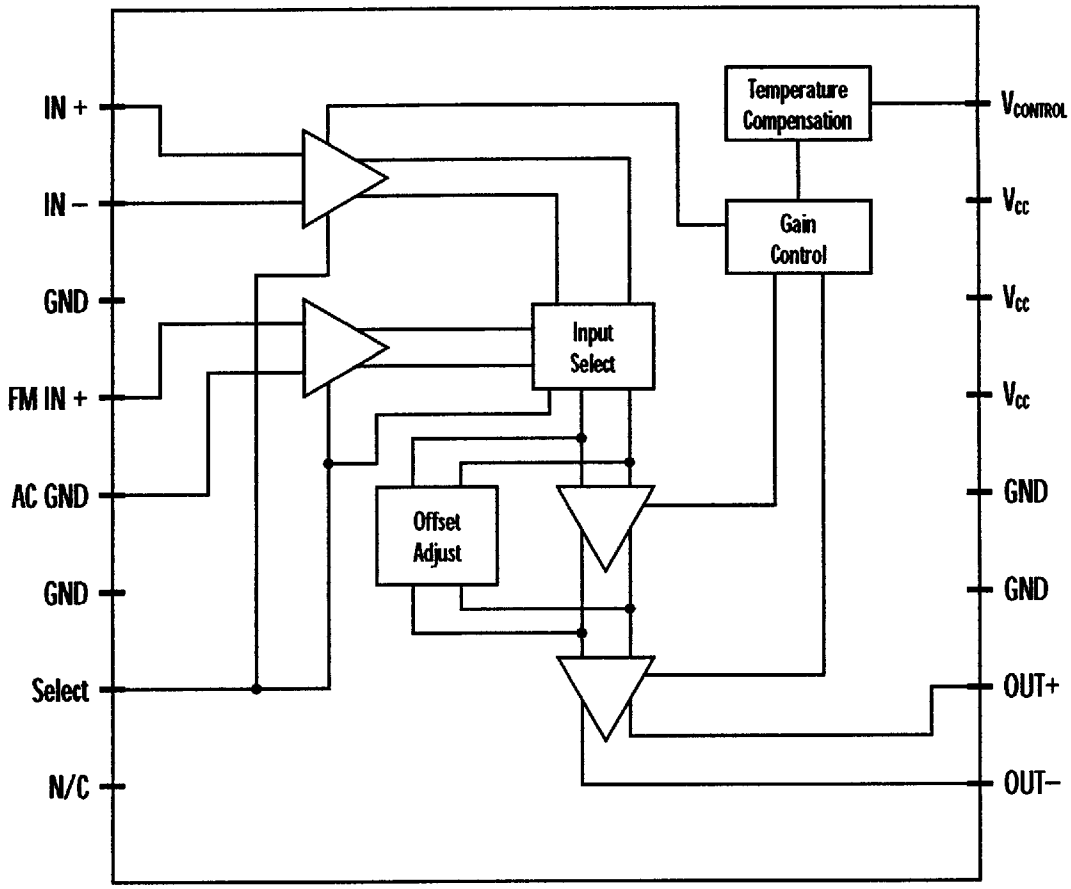

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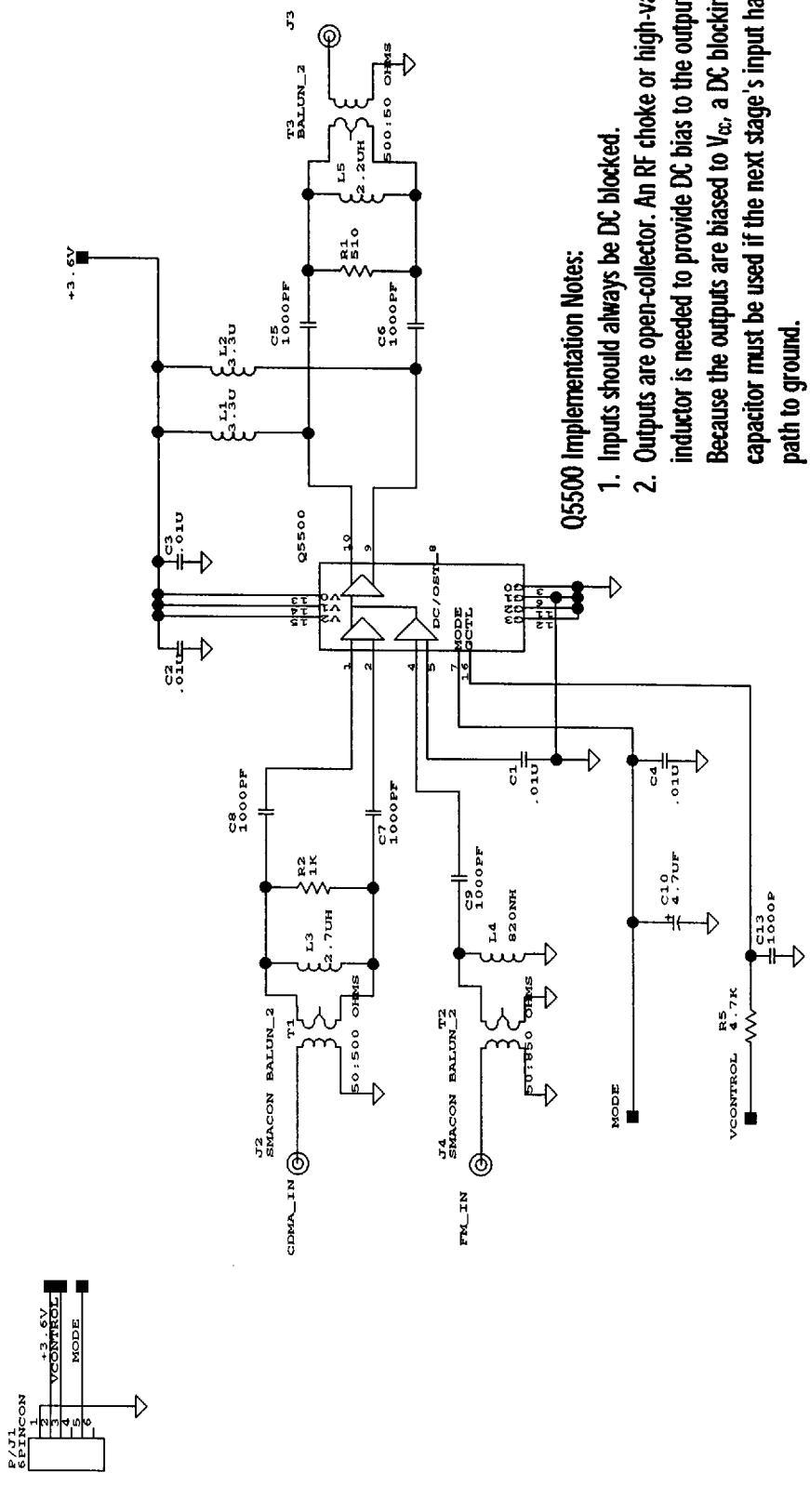
Figure 10. Q5500 Test Schematic



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Q5505 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent and functional damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond the min/max ranges indicated in the operational sections of this specification is not implied. Exposure exceeding absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Q5505 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T_{STO}	-30	+125	°C	
Junction Temperature	T_J	-30	+125	°C	
Supply Voltage (Relative to GND)	V_{CC}		+8.5	V	
Continuous RF Input Power			-15	dBm	
DC Voltage on any Non RF Input Pin (Relative to GND)	V_{IN}	-0.5	V_{CC} + 0.5	V	
Latchup Insensitivity	I_{TRIG}	±200		mA	1
ESD Protection	V_{ESD}	±250		V	2

NOTES:

1. Method meets the intent of JEDEC STD 17 Publication and is the maximum allowable current flow through the input and output protection diodes.
2. Method meets the intent of MIL-STD-883. Method 3015.

Table 8. Q5505 Operating Range

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature (Case)	T_C	-30	+80	°C
Operating Voltage (Relative to GND)	V_{CC}	+3.42	+3.78	V

Table 9. Q5505 DC Electrical Parameter

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Current	I_{CC}		25	mA	

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Table 10. Q5505 Electrical Characteristics

PARAMETER	VALUE	NOTES
TX AGC Frequency	130.38 MHz	
Gain Flatness (± 630 kHz)	±0.25 dB	
TX Power Gain	$V_{CONTROL}$ = 0.1 V, G< -45 dB $V_{CONTROL}$ = 3.0 V, G> 40 dB	1, 4 3, 5
Power Gain Slope	70 dB/V Maximum Over Specified Gain Region (-45 to +40 dB) 0 dB/V Minimum Over Specified Gain Region (-45 to +40 dB)	1, 4, 3
Power Gain Slope Linearity (Over and 6 dB Gain Segment)	± 3.0 dB/V	
NF for AGC Input	Figure 14	1
IIP3	Figure 15	1, 2, 3
IF Input Impedance (Differential)	1k ± 15%, < 1 pF Capacitive	4
IF Output Impedance	> 10 k Ω, < 1 pF Capacitive	4
Gain Control Pin Input Impedance	> 30 kΩ, < 50 pF Capacitive	
Stability	Over Full AGC Range With Source and Load VSWR 10:1 All Angles Spurious < -70 dBc	

NOTES:

1. Z_S = 1 kΩ, $Z_{L_{eff}}$ = 500 Ω, Z_L = 1 kΩ (see Figures 11a and 11b).
2. IIP3 = IMR3/2 + P_{IN} dBm, where IIP3 is the input third order intercept in dBm, IMR3 is the third order intermodulation product rejection in dB, and P_{IN} is the total power of the two input tones in dBm.
3. Input Power level = -38 dBm.
4. See Figures 11a and 11b.
5. $V_{CONTROL}$ Source Impedance must be 3.3 k ± 5%.

Figure 11a. Definition of Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5505

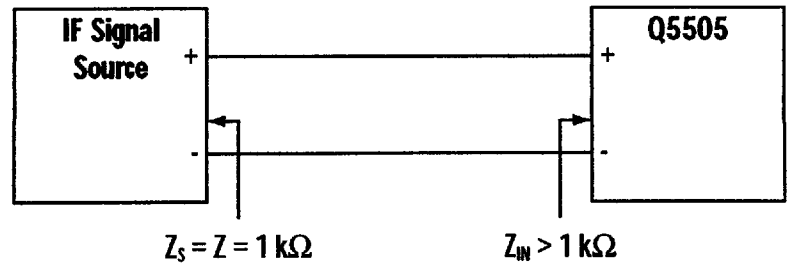

Figure 11b. Definition of Load Impedance, Z_L, and Output Impedance, Z_O, for Q5505

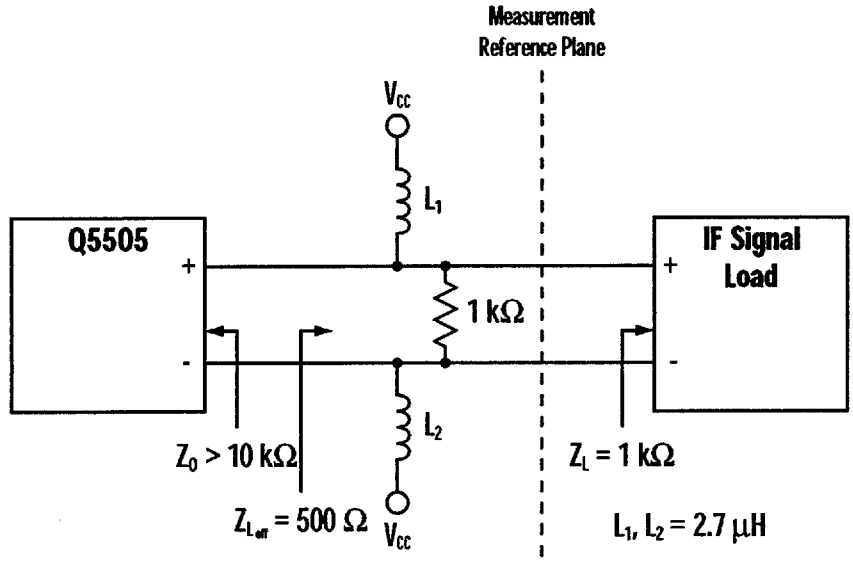

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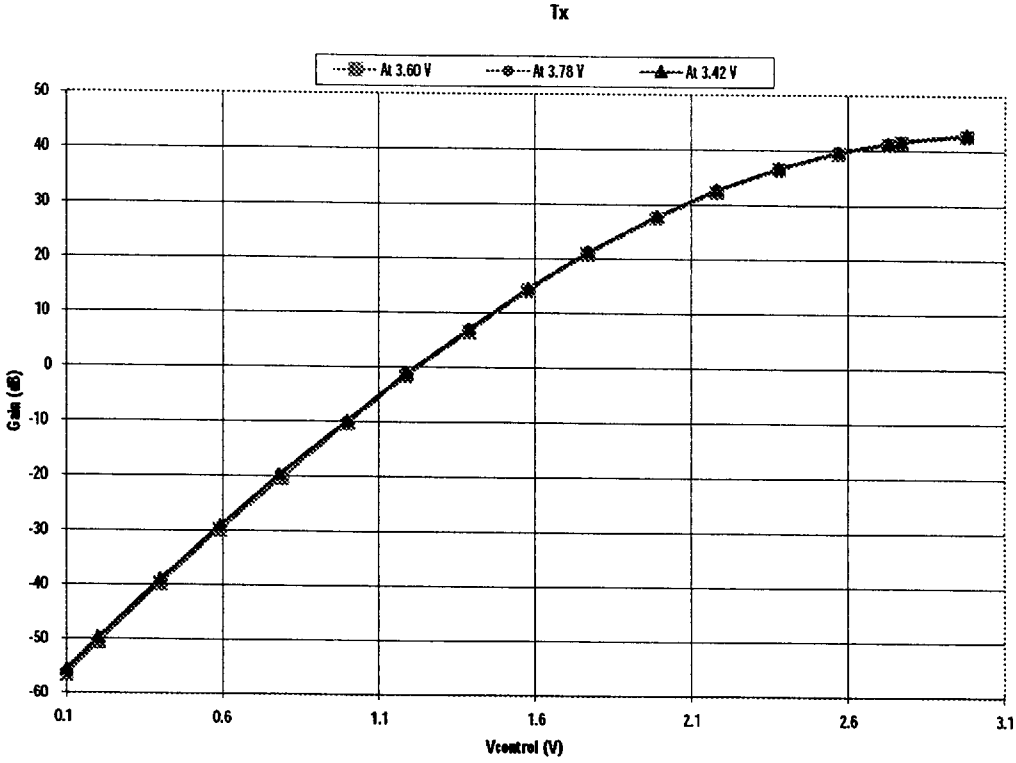
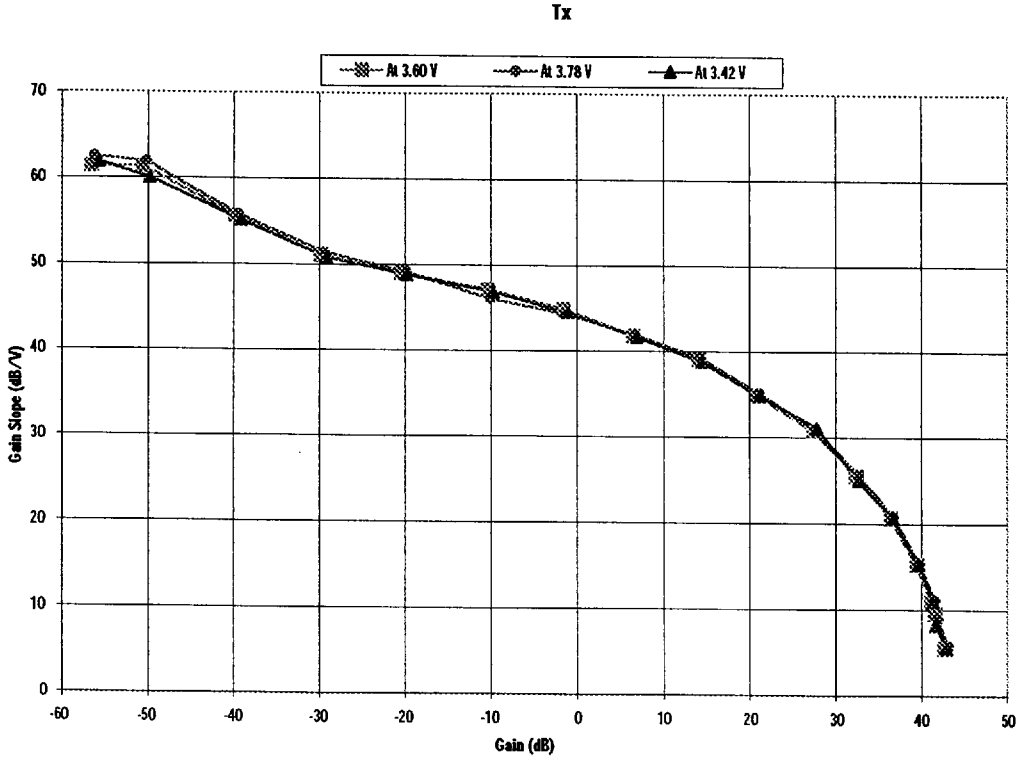
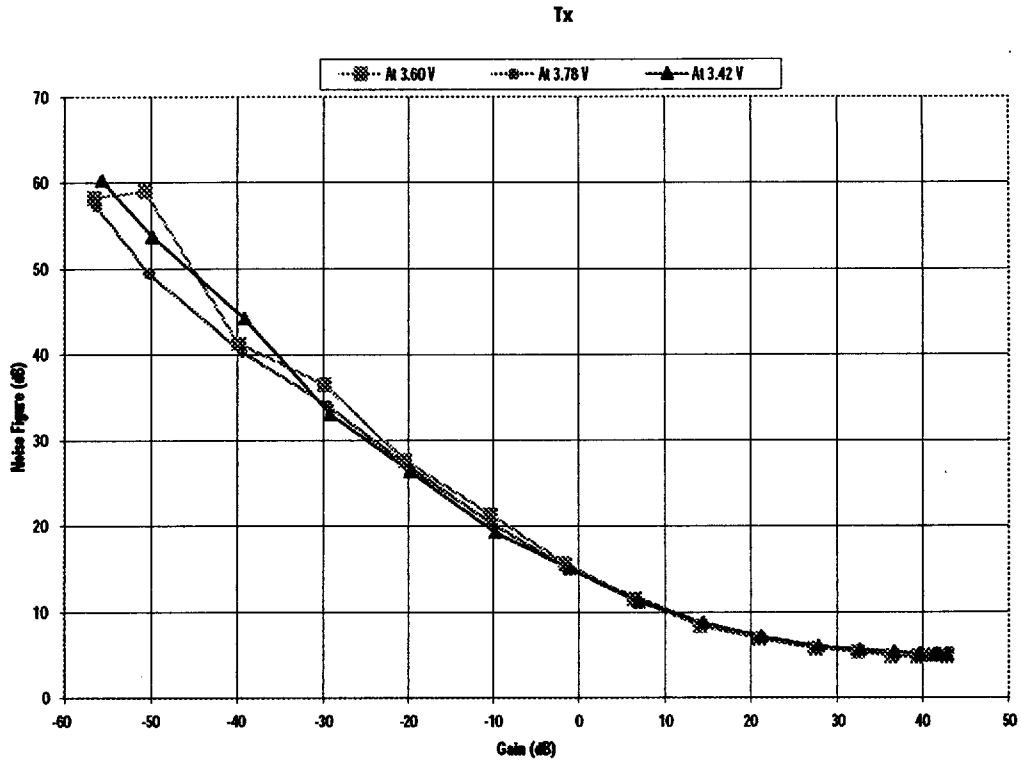
Figure 12a-e. Typical Q5505 Performance Characteristics Over Supply Voltage Range



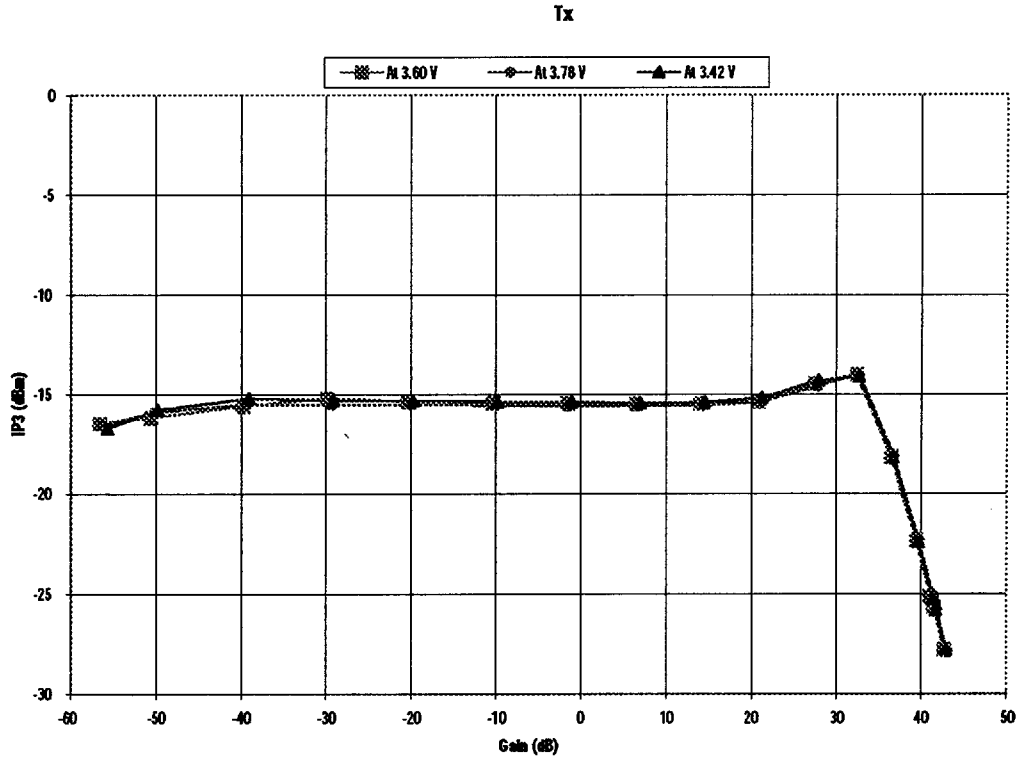
a. Gain vs. Control Voltage



b. Gain Slope vs. Gain



c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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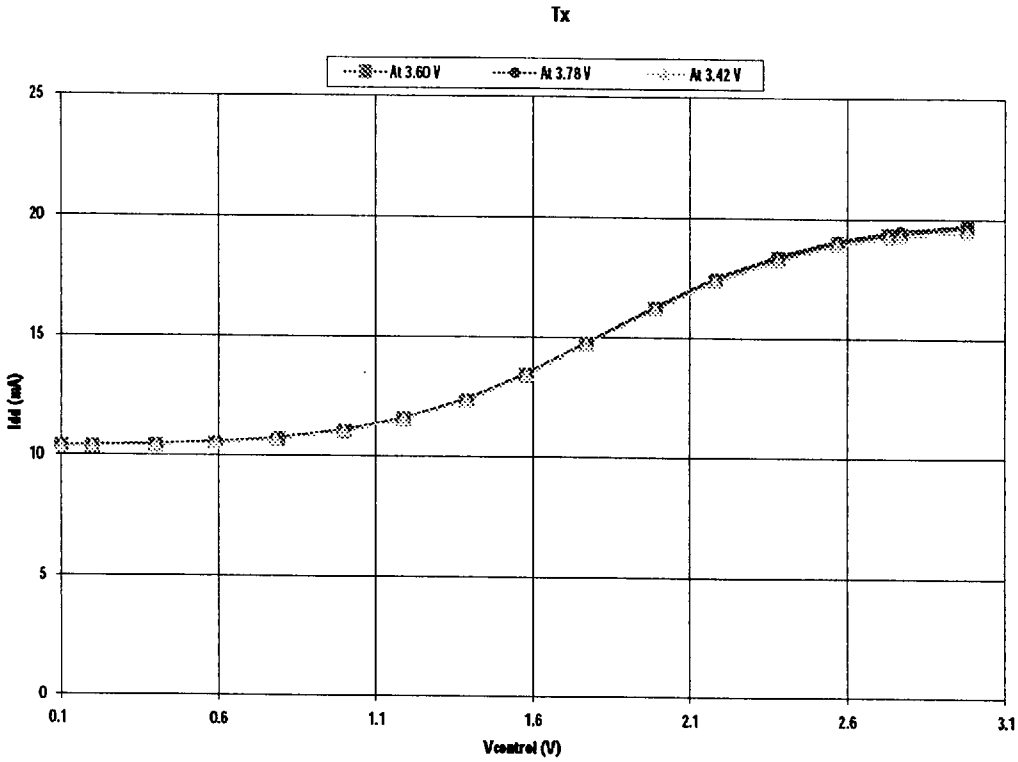
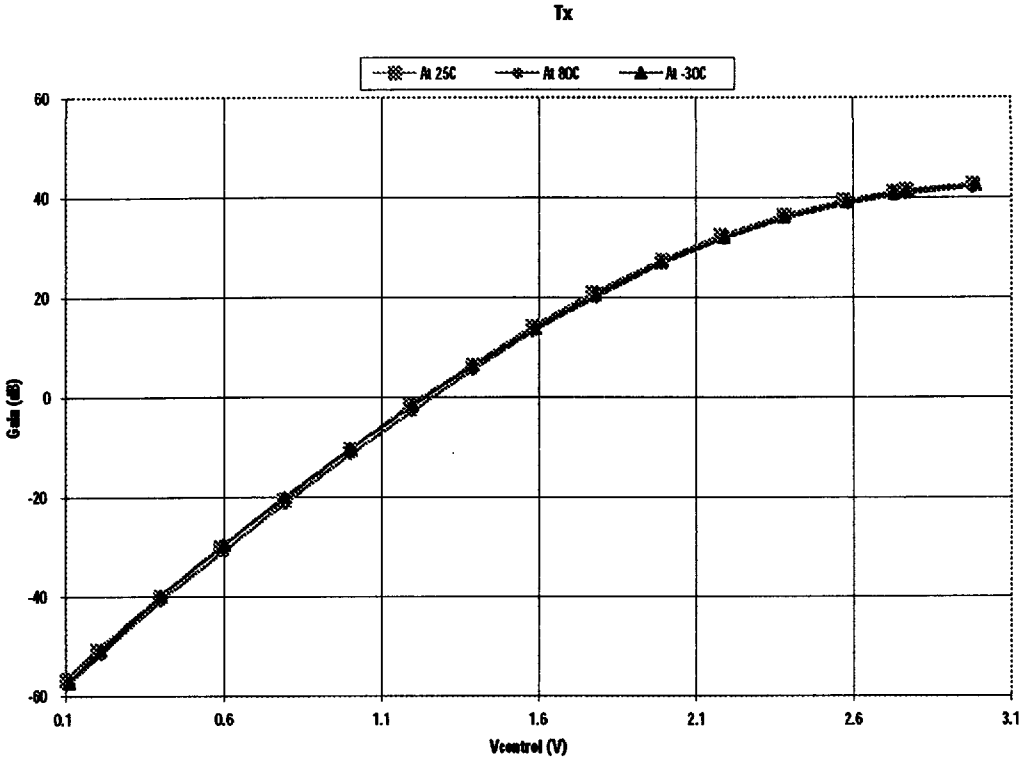
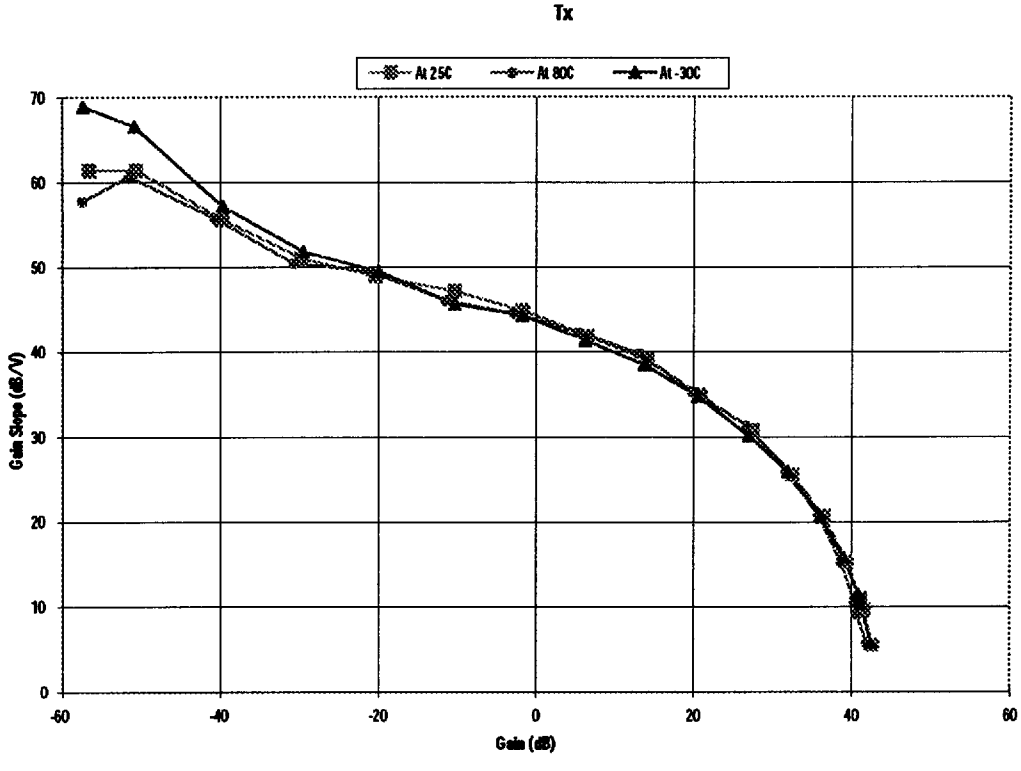


e. Supply Current vs. Control Voltage

Figure 13a-e. Typical Q5505 Performance Characteristics Over Operating Temperature Range



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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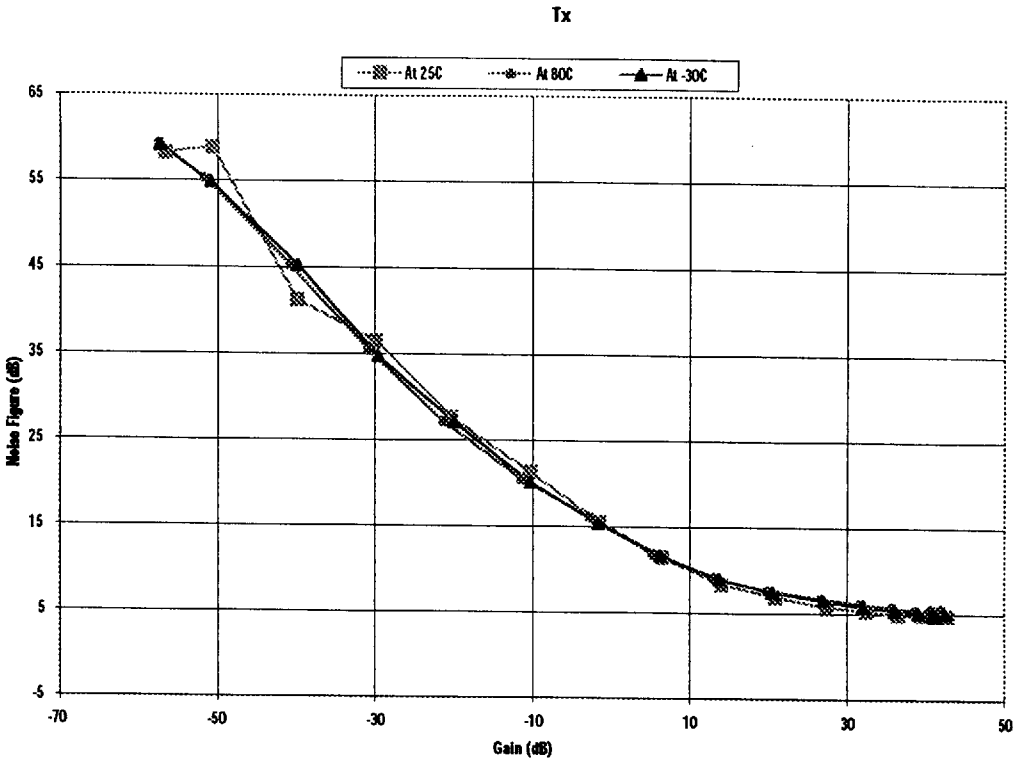
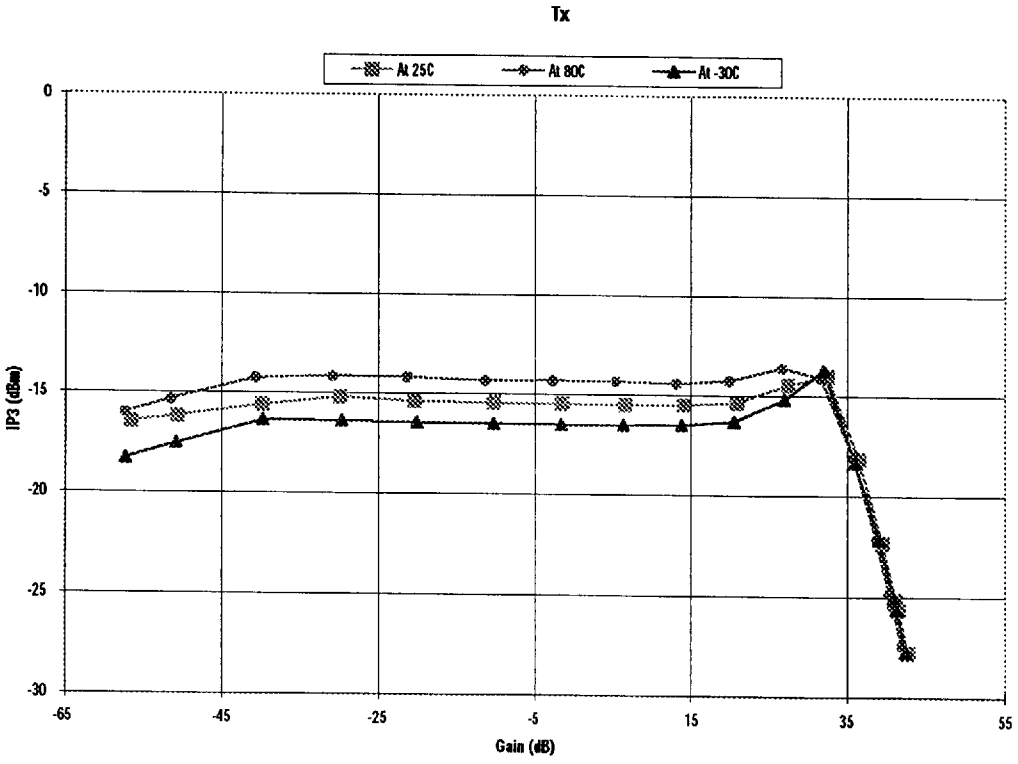
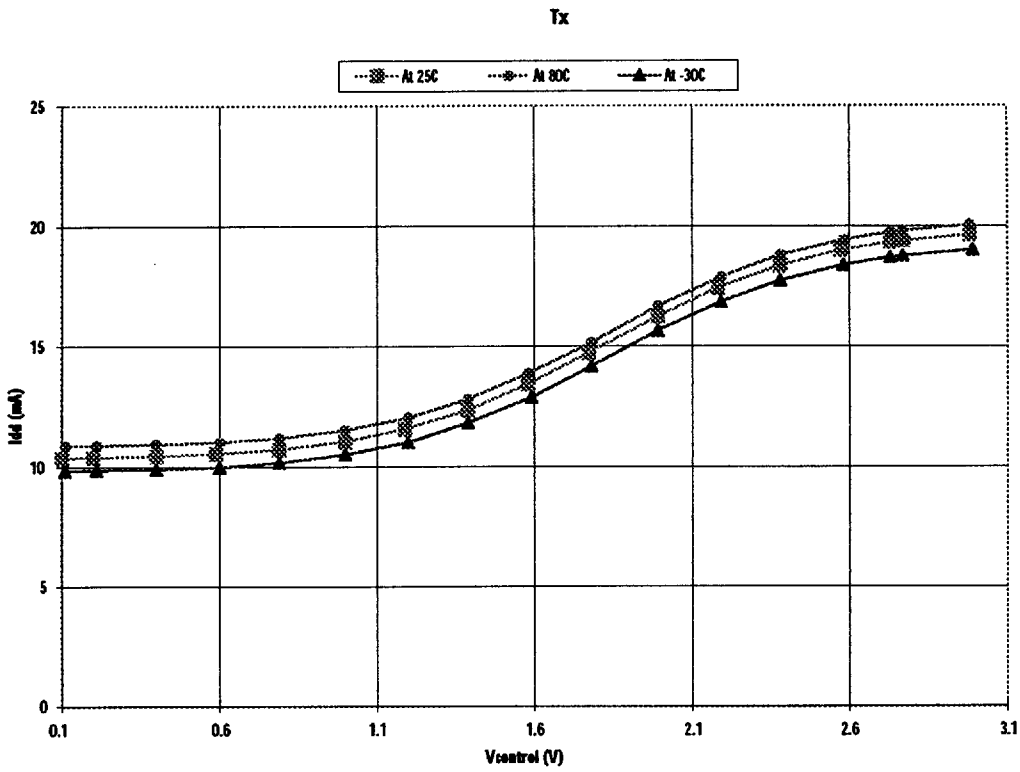


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain



e. Supply Current vs. Control Voltage

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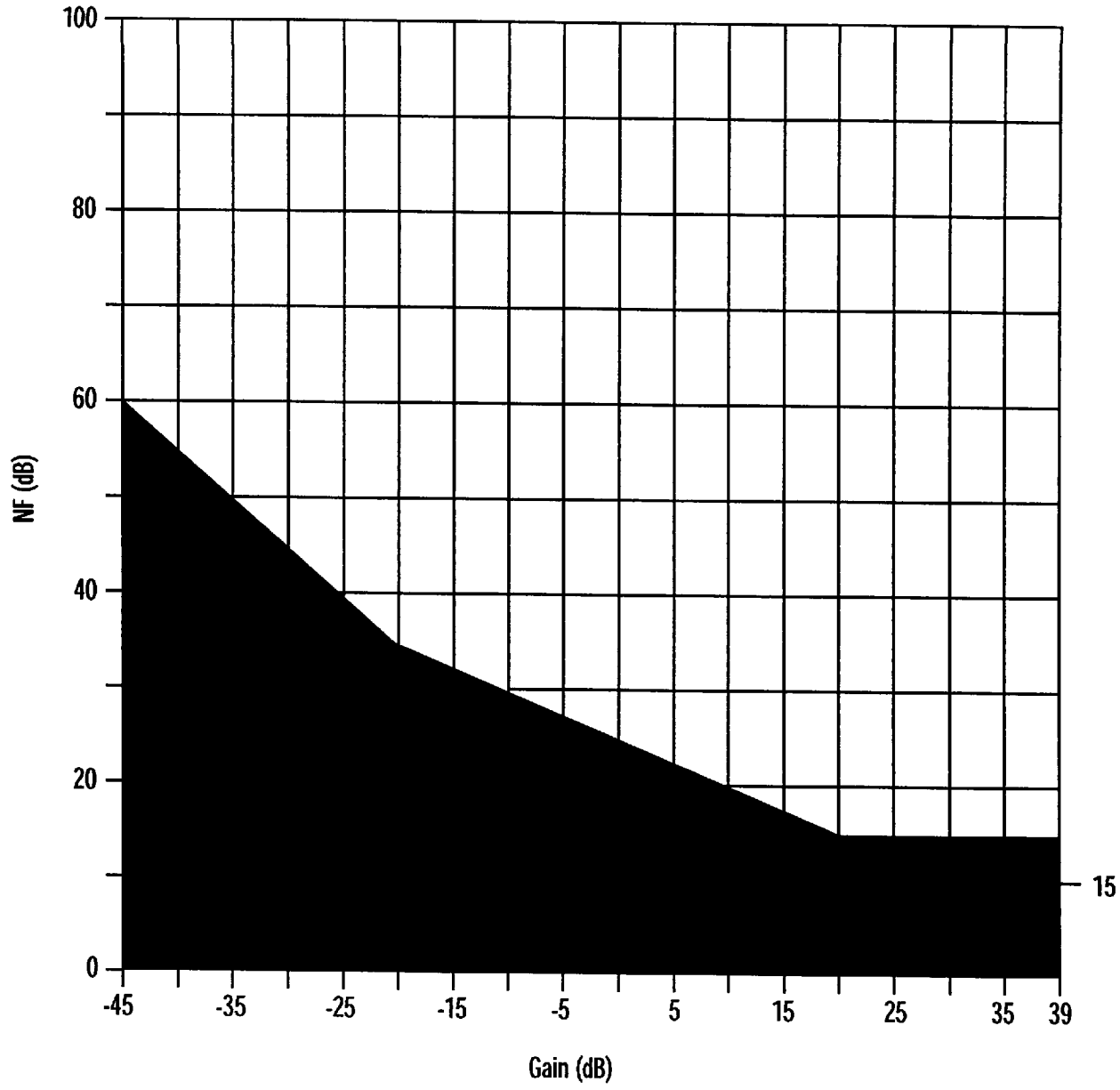
Figure 14. Q5505 Cascaded NF Model



NF < 14.5 - G (-45 < G < -20 dB) Gain
NF < 24.75 -0.4875* G (-20 ≤ G ≤ +20 dB)
NF < 15 (20 < G < 40 dB)

Figure 15. Q5505 Cascaded IIP3 Model

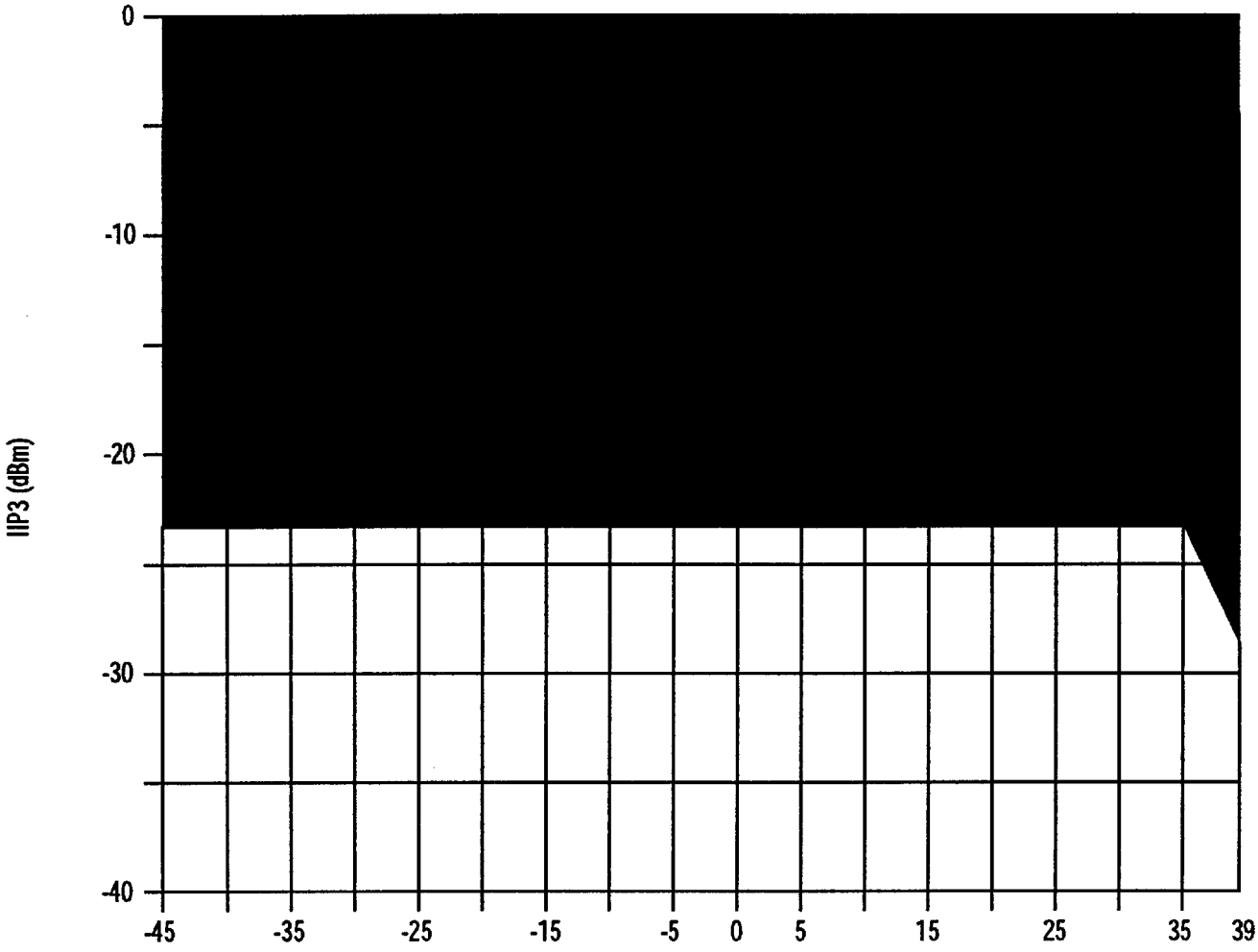


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Table 11a-e. Description of Q5505 Pin Functions

a. Hi-Gain Digital Mode Differential Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
IN +	1	Differential Input	Positive Differential Input
IN –	2	Differential Input	Negative Differential Input

b. Analog Gain Control Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
$V_{CONTROL}$	16	DC Input	$V_{CONTROL}$ = Analog Gain Control Input $V_{CONTROL}$ = 0.1 V, Low Gain Rail, $V_{CONTROL}$ = 3.0 V, High Gain Rail

c. Analog Differential Output Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
OUT +	10	Differential Output	Analog Positive Differential Output
OUT –	9	Differential Output	Analog Negative Differential Output

d. Unconnected Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
–	8	N/C	Unconnected Pin

e. Voltage Supply Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
V_{CC}	13, 14, 15	Power	V_{CC} Power Supply
GND	3, 4, 5, 6, 7, 11, 12	Ground	Ground Connection

Figure 16. Q5505 Functional Block Diagram

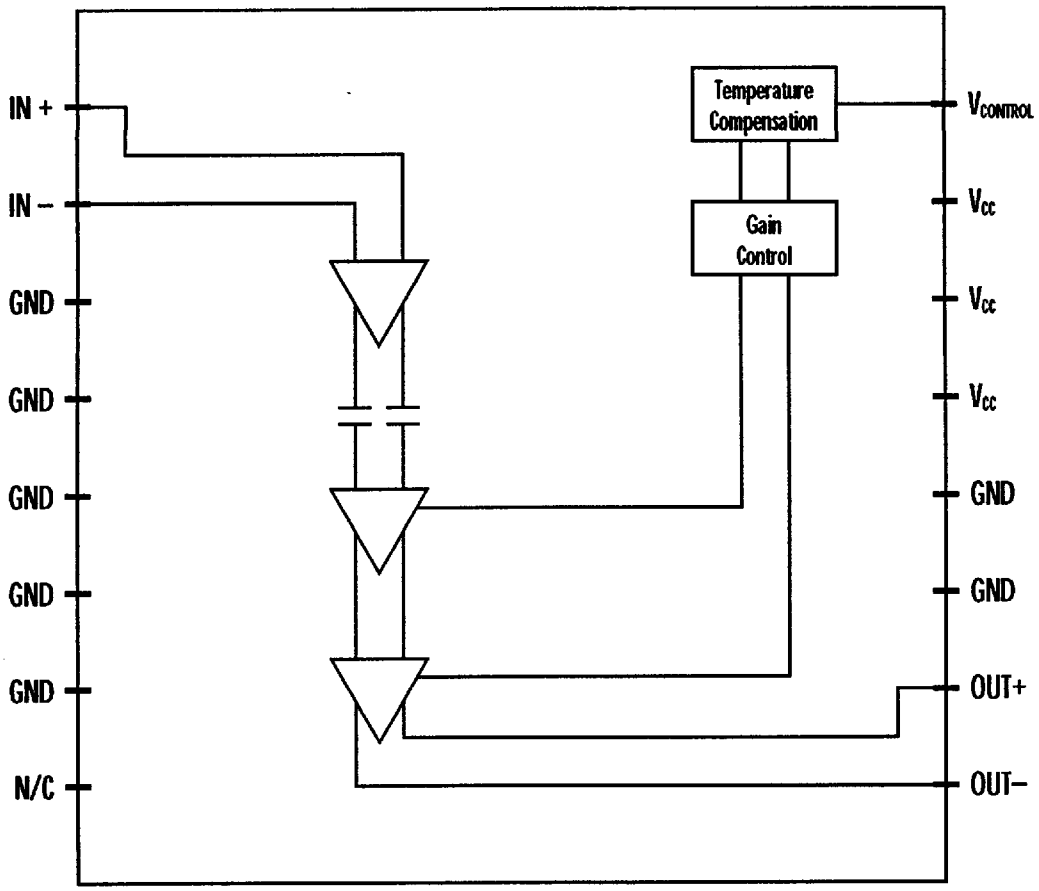

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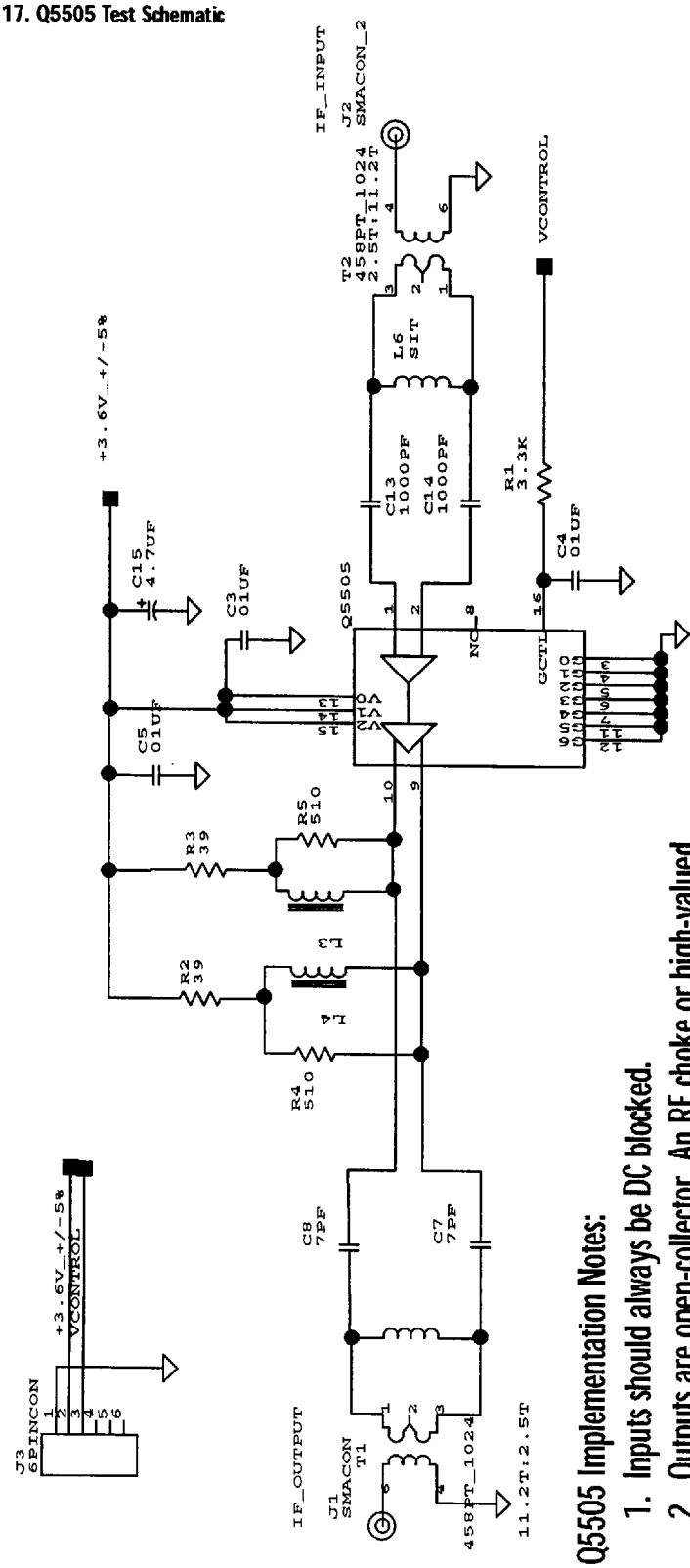
Figure 17. Q5505 Test Schematic



Q5505 Implementation Notes:

1. Inputs should always be DC blocked.
2. Outputs are open-collector. An RF choke or high-valued inductor is needed to provide DC bias to the output pins. Because the outputs are biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.
3. The input/output interface may require matching networks, however this requirement is very system dependent. The bias inductor is typically incorporated in the matching network between the output and next stage.
4. V_{CC} inputs should be bypassed to ground with about a 0.01µF capacitor, keeping trace connections to a minimum length.

INPUT IMPEDANCE MATCHING

As with all active and passive components in the signal paths of the RF subsystem, the impedance levels in the signal path should be controlled and matched to minimize losses. The input impedance of the CDMA inputs to the Q5500 and Q5505 is specified as 1000 Ω ±15%. When driving the Q5500 from a 500 Ω differential source impedance, a 1000 Ohm resister should be connected between the IN+ and IN- inputs. This will set the effective input impedance to 500 Ω ± 8% (assuming a stable and accurate 1000 Ω external resister).

The FM inputs of the Q5500 are differential but may be used with a single-ended input signal. In the single-ended case, pin 5 should be connected to ground through a 0.01 µF capacitor. This causes pin 5 to be an AC ground pin. The single-ended input impedance for the FM+ input is 850 Ohms ±15%. If driven from a 500 Ω source, an external resistor of 1.2 kΩ connected between the FM+ input and ground will set the effective single-ended FM input impedance to 500 Ω ±10%.

The Q5500 and Q5505 amplifiers include temperature-compensated input biasing circuits that maintain the DC input level of the IN+, IN-, FM+ and FM- inputs. The application circuit should AC-couple the IF signals into the AGC amplifiers. No DC biasing circuits are required.

OUTPUT IMPEDANCE MATCHING

The output devices of the Q5500 and Q5505 OUT+ and OUT- pins are open-collectors of NPN transistors. This allows the differential output impedance (the impedance between the OUT+ and OUT- pins) of the amplifier to be set to various levels and controlled by external components. The open-collector outputs require a DC path to VCC. The DC path requirement is satisfied by connecting either a resistor or an inductor between the OUT pin and VCC.

Resistive collector loads on the OUT+ and OUT- pins set the differential output impedance to the sum of the two load resistors. For example, if 250 Ω resistors are used for developing the output signal, the differential output impedance of the circuit will be (250 + 250) = 500 Ω. Resistive loads on the open collector outputs have disadvantages. Current flowing through the resistors carries with it a component at the IF frequency. This high-frequency component can add to power supply noise and require a more complex power supply decoupling network. Additionally, noise already on the power suppy voltage may be injected into the IF output signal through the collector load resistors.

An alternate method for loading the open-collector outputs of the AGC amplifiers is to employ relatively high-inductance "chokes" instead of resistors (see Figures 18 and 19). An inductor between the OUT and VCC pins meets the DC path requirement but blocks the IF frequency from the power supply voltage and blocks power supply noise from the amplifier's output signal. Inductor values on the order of 2.7 µH work well here. Inductive loads do not significantly contribute to the differential output impedance because their reactance at IF frequencies is high. When using inductive loads, the differential output impedance is set by connecting a resistor between the OUT+ and OUT- pins. The value of the resistor becomes the differential output impedance.

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Figure 18. Application Schematic for the Q5500 Rx AGC Amplifier

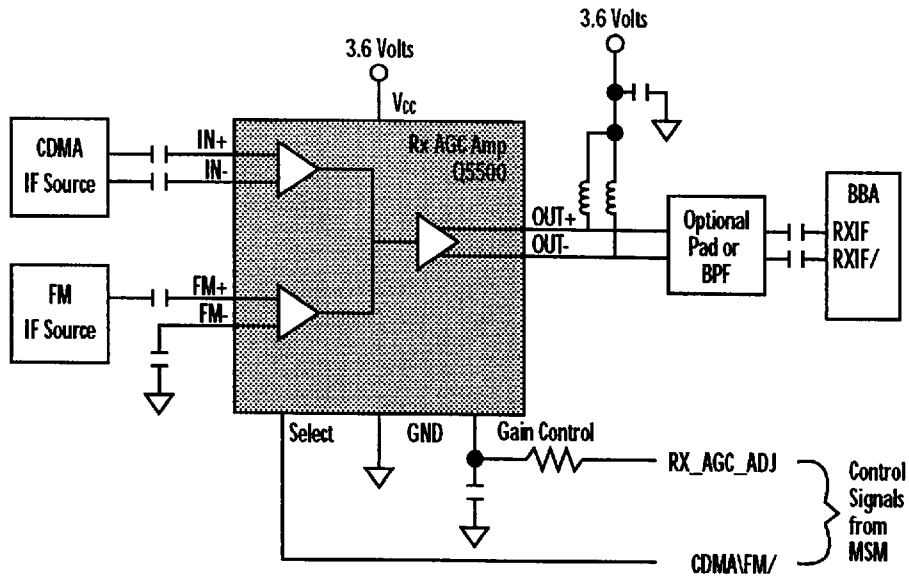
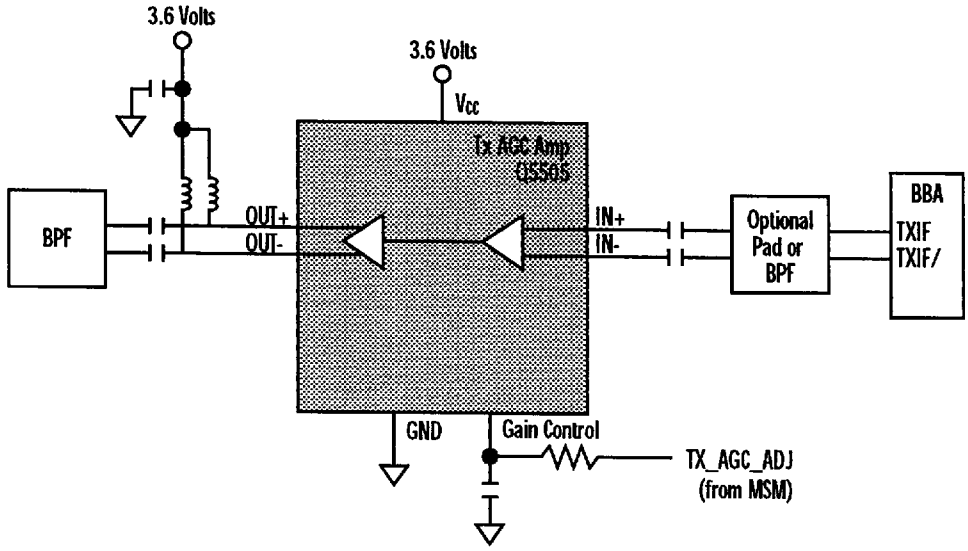


Figure 19. Application Schematic for the Q5505 Tx AGC Amplifier



CDMA APPLICATIONS

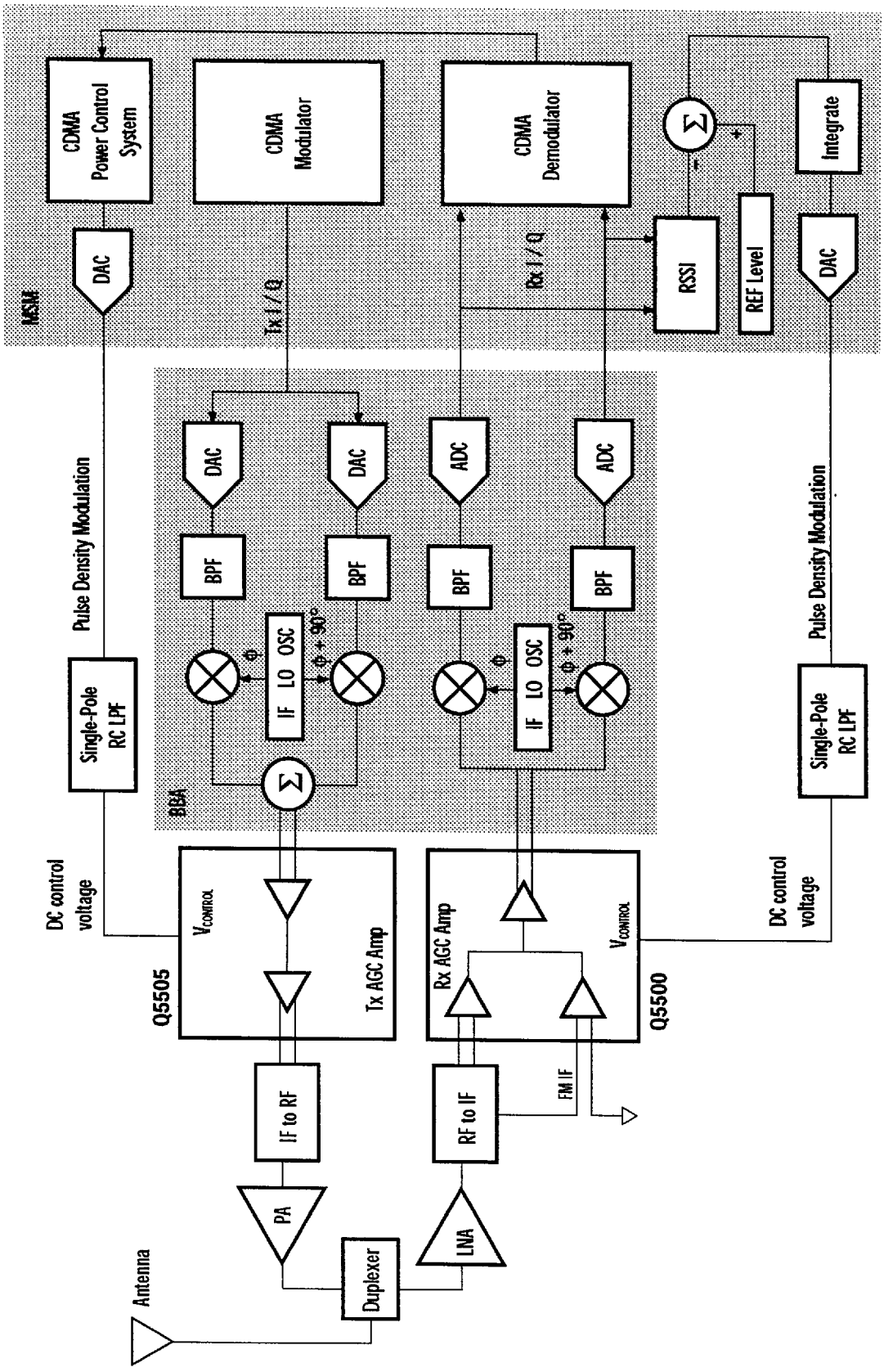
The AGC circuits are critical in maintaining consistent power levels with the changing distances between subscriber handsets and base stations in a cellular network. Figure 20 shows the basic distribution of control signals from the Mobile Station Modem (MSM) RF interface to the Analog Baseband Processor (BBA) and AGC components in the analog and RF sections of the QUALCOMM subscriber unit. The RF interface of the MSM is made up of several completely digital circuit blocks that monitor and control analog parameters. One of the important functions of the RF interface of the MSM is analog signal gain control. The RF interface communicates with the BBA and AGC circuits via Pulse Density Modulation (PDM). PDM signals require only 2 passsive components, a resistor and a capacitor, to provide a low-ripple DC control voltage for the Q5500/Q5505 VGAs and other analog circuit functions.

The basic structure of the Rx AGC loop (lower half of Figure 20) is the same as the architecture of the general AGC loop except that all of the functions such as RSSI estimation and generation of the VGA control voltage ($V_{CONTROL}$) are done by digital circuits. The Rx Signal-to-Noise Ratio (SNR) in the subscriber unit is optimized by controlling the gain of analog RF and IF stages in the receive signal path. CDMA receivers must operate over input signal strengths that range from -113 dBm to -25 dBm. The Rx AGC loop varies the Q5500 amplifier gain to compensate for the variation in power level of the incoming RF. The purpose of the receive AGC loop is to keep the signal amplitude high and power level consistent at the demodulator input without distorting and overdriving the demodulator. The Q5500's gain range of -45 to +45 dB attenuates or amplifies the IF signal so that the power level of the I and Q components at the input to the CDMA demodulator is constant. The Q5500 is required to operate in both FM and CDMA Modes. The main difference between FM and CDMA Modes is that the linearity requirement is less stringent for FM than for CDMA. Also, the FM input is single-ended while the CDMA input is balanced. The gain control section of the Q5500 processes the gain control voltage, $V_{CONTROL}$, so the overall IF signal gain, measured in dB, is approximately a linear function of $V_{CONTROL}$ and also provides temperature compensation.

The CDMA transmit AGC loop is part of the power control system that distinguishes CDMA from other multiple-access telecommunications protocols. The Tx AGC loop (upper half of Figure 20) is closed by communication with the base station. In CDMA, the base station controls the RF power output of all subscriber units. The signal strength of the subscriber unit is measured at the base station and varies widely due to the changing distance from the subscriber unit to the base station, multipath fading, terrain topology, and environmental conditions. The purpose of the Tx AGC control loop on the MSM is to provide a linear variable RF output power level to the subscriber unit antenna to compensate for these effects. The subscriber unit receives power control information from the base station which increases or decreases the subscriber unit Tx power. The base station maintains the Tx power level of each subscriber unit in the cell so that the received power from each subscriber unit is the same. For both CDMA and FM Modes in the subscriber unit, the Q5505 is the primary gain control element in the Tx signal path between the BBA and the upconverter. The signal which controls the gain of the Q5505 is a lowpass filtered PDM signal obtained from the MSM. The linearity of the VGA used in the path of a CDMA transmit AGC loop is typically depicted with an Adjacent Channel Power Rejection (ACPR) response to an input CDMA waveform. This provides a figure of merit for evaluating a VGA's nonlinearity at various gain settings. Figure 21 shows the Q5505's typical ACPR response at higher operating gains where device linearity is stressed the most.

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA,
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Figure 20. CDMA Subscriber Unit Simplified Block Diagram



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6455 Lusk Boulevard, San Diego, CA 92121-2779, USA,
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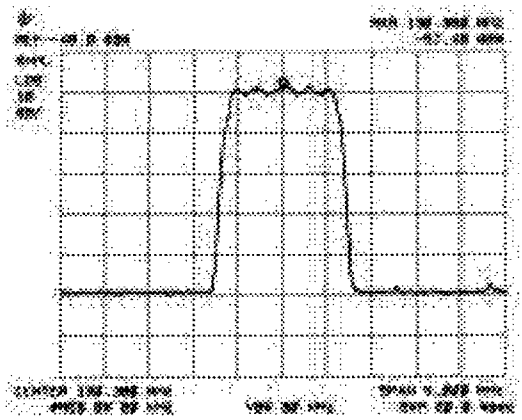
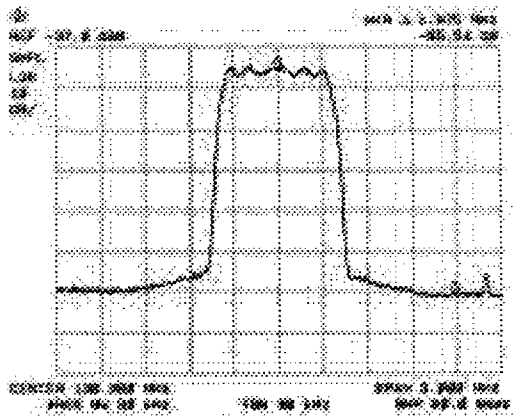
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

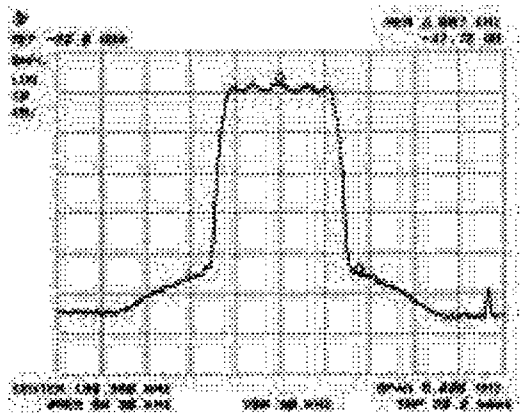
Figure 21a-d. Adjacent Channel Power Rejection (ACPR) Response of Q5505 to CDMA Waveform



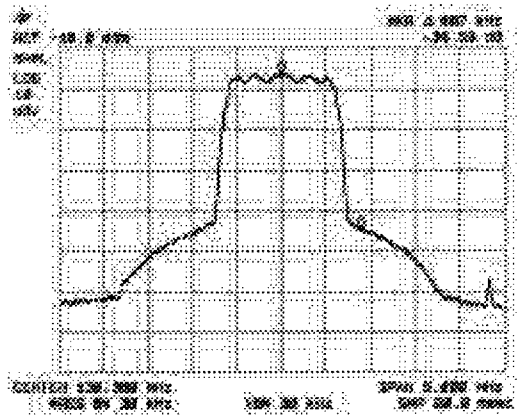
a. CDMA Input to Q5500



b. ACPR Response @ G = + 20 dB



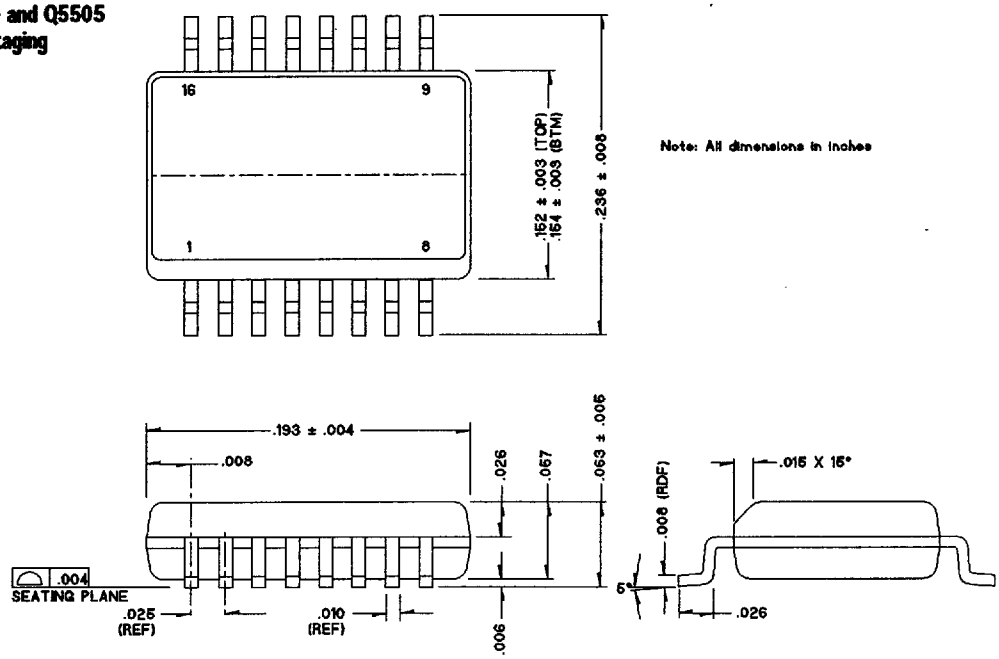
c. ACPR Response @ G = + 35 dB



d. ACPR Response @ G = + 39 dB

Test Conditions: Input Power @ - 42.2 dBm
VCC Supply @ 3.6 V

Figure 22. Q5500 and Q5505 16-pin SSOP Packaging



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA,
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

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