National Semiconductor

PRELIMINARY

microCMOS

NMC98C64
8k x 8 CMOS Electrically Erasable PROM

General Description

The NMC98C64 is a 5V only CMOS E²PROM with desirable ease of use features that facilitate in-circuit programming using a single suppy and TTL level signals. In addition, the NMC98C64 is compatible with present high density EPROMs which require high voltage programming and UV erasing. The NMC98C64 is a state-of-the-art product that uses the advanced microCMOS stepper based technology. The process is an enhancement of the proven XMOS™ process for reliable, non-volatile data storage.

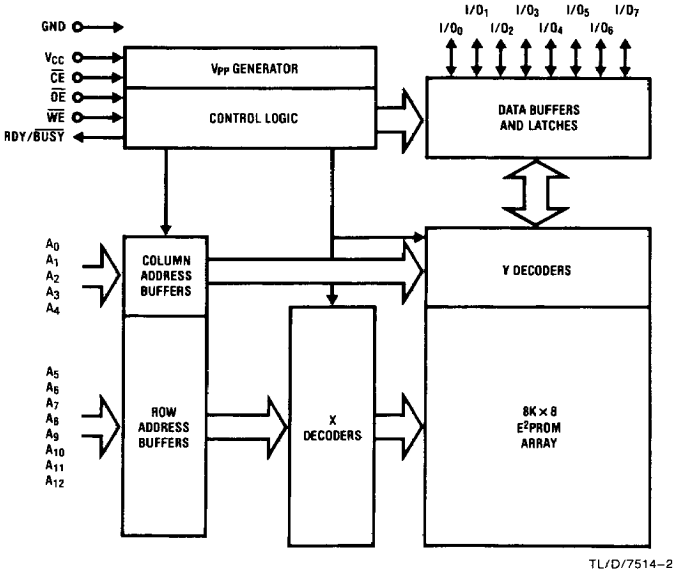
Writing data in NMC98C64 is analagous to writing to a SRAM. A 200 ns min TTL pulse to the $\overline{WE}$ pin initiates a byte write operation which is automatically timed out. Address and data latches free the system bus for the duration of the write. Ready/$\overline{Busy}$ facilitates service by providing an interrupt to the controller; an open drain output facilitates "wire or" connection in larger systems.

A 32-byte page write allows data to be accepted at an effective rate of 300 μs/page or 2.6 seconds to write an entire chip.

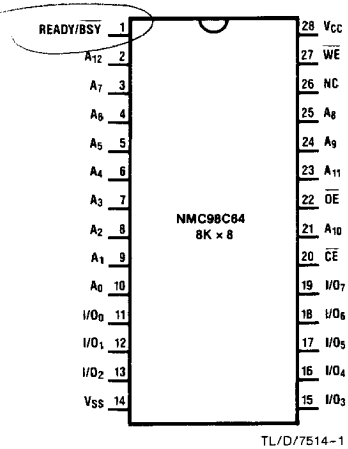
Features

- Single 5-V power supply
- Low CMOS power
  - — Active, 10 mA typical
  - — Standby, 100 μA typical
  - — Quiescent, 100 μA typical
- Simple byte write and page write
  - — On-chip address and data latches
  - — Self-timed cycle, auto erase before write
  - — Page write up to 32 bytes per page
  - — Ready/Busy open drain status output and $\overline{DATA}$ polling verification
  - — Write protection
- Fast write time
  - — Byte or page write, 10 ms max
  - — Entire chip write in 2.6 seconds
  - — Page data load, 300 μs typical
- Fast access time: 200 ns/250 ns/350 ns
- CMOS and TTL compatible level inputs/outputs

Block and Connection Diagrams



TL/D/7514–2



TL/D/7514–1

Order Number NMC98C64
See NS Package J28A

A_0–A_4	Column Addresses
A_5–A_{12}	Row Addresses
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BUSY}$	Device Ready/Busy
NC	No Connect

TABLE I. Operation Modes (V_{CC} = 5V + 10%)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/00-I/07	RDY/$\overline{BUSY}$	Power
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z	Active/Quiescent
Write Single Byte or 1st Byte in a Page	V_{IL}	V_{IH}	⊓	D_{IN}	High Z → Vol	Write
Write Subsequent Bytes in a Page	V_{IL}	X	⊓	D_{IN}	Vol	Write
Busy	V_{IH} X	X V_{IH}	X X	Hi-Z Hi-Z	Vol Vol	Write Write
$\overline{DATA}$ Polling	V_{IL}	V_{IL}	V_{IH}	$I/O_7 = \overline{D_{IN}}$	Vol/Hi-Z	—
Standby	V_{IH}	X	X	High Z	High Z	Standby
Write Inhibit	X X	V_{IL} X	X V_{IH}	– –	High Z High Z	– –

Device Operation

The NMC98C64 is organized as 256 rows of 32 bytes (256 × 32 × 8). Address inputs A5 through A12 are decoded to select one of the 256 rows (pages) of storage locations. A0 through A4 are decoded to select one of the 32 bytes within the selected row. The device has various modes of user operation (detailed in Table I). All input/output levels are TTL compatible. "X" denotes don't care situation to TTL levels.

READ MODE

The read cycle of the NMC98C64 is similar to that of an EPROM or a static RAM. A low $\overline{CE}$ and a low $\overline{OE}$ enable the output buffers. The Ready/$\overline{Busy}$ pin is at high impedance state during the read cycle.

WRITE MODE

Writing data to the NMC98C64 is similar to writing to a static RAM. There are two ways to load data into data latches of the device in a write cycle, which once initiated will automatically continue to the completion in 10 ms.

A byte write is accomplished by applying to the device a data load cycle in which a low going pulse to $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high is required. The data presented at I/O pins are written into the location selected by a byte address.

A page write allows a page of data to be written into E²PROM in a single write cycle. Instead of one data load cycle, up to 32 (page size) data load cycles can be applied to the device in 300 μs after the first data load cycle. The address (A5-A12), which is presented to address pins before the first $\overline{WE}$ pulse going low, is latched in the device and used as the page address for the rest of the cycle. The byte addresses (A0–A4) may be put in any order providing they are on the same page. Through page writes the entire memory can be written (or rewritten) in 2.6 seconds.

The data load cycle can be finished by bringing $\overline{CE}$ or $\overline{WE}$ high and keeping that through the rest of the data load time.

The row address (page address) is latched internally after first data load cycle.

The WRITE mode status can be interrogated in two ways:

- Ready/$\overline{Busy}$ — The Ready/$\overline{Busy}$ pin (pin 1) goes to a logic low level indicating that the NMC98C64 is in a write cycle. When Ready/$\overline{Busy}$ goes back to high impedance the NMC98C64 has completed writing, and is ready to accept another cycle.
- $\overline{DATA}$ Polling — The NMC98C64 features $\overline{DATA}$ Polling to signal the completion of a byte or page write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_7. After completion of the write cycle, true data is available. $\overline{DATA}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

STANDBY MODE

A device is disabled by bringing $\overline{CE}$ high. The power dissipation is reduced to I_{CCS} if it is disabled between operations. Writing to the memory in the standby mode is inhibited.

WRITE INHIBIT MODE

Holding $\overline{OE}$ low or $\overline{WE}$ high always inhibits a write cycle.

WRITE PROTECTION

There are three features that protect the non-volatile data from an inadvertent write:

- Noise Protection — A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- Write Inhibit — Holding $\overline{CE}$ high, $\overline{OE}$ low or $\overline{WE}$ high inhibits a write during the time when V_{CC} supply is being powered up/down,
- Optional V_{CC} Sense — To avoid the initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for V_{CC} less than 3.8 volts. It is the user's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.8 volts.

To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE}$ = V_{IH} must be applied simultaneously or before application of V_{CC}. $\overline{WE}$ or $\overline{CE}$ = V_{IH} must be removed simultaneously or after V_{CC}.

To prevent damage to the device it must not be inserted into or removed from a board with power applied.

ENDURANCE

National Semiconductor E²PROM devices are designed for applications requiring up to 10,000 Erase/Write cycles per byte.

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
Lead Temp. (Soldering, 10 Seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Operating Conditions

Temperature Range	0°C to +70°C
V_{CC} Power Supply (Notes 2 and 3)	5V ± 10%

DC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol		Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION							
I_{LI}		Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}			10	μA
I_{LO}		Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC} $\overline{CE} = V_{IH}$			10	μA
I_{CCA}	TTL	V_{CC} Current Active (Operating)	Inputs toggling with V_{IH} & V_{IL} levels, I/O's = Open		10	20 + 5/MHz	mA
	CMOS		Inputs toggling with CMOS levels (V_{CC} − 0.2V; V_{SS} + 0.2V), I/O's = Open			0.2 + 5/MHz	mA
I_{CCS}	TTL	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			2	mA
	CMOS		$\overline{CE} \geq V_{CC}$ − 0.2V		100	200	μA
I_{CCQ}	TTL	V_{CC} Current Quiescent	$\overline{OE} = \overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$ A_0–$A_{12} = V_{IL}$ or V_{IH}, I/O's = Open			20	mA
	CMOS		$\overline{OE} = \overline{CE} \leq V_{SS}$ + 0.2V, $\overline{WE} \geq V_{CC}$ − 0.2V I/O's = Open, A_0–$A_{12} = V_{SS}$ + 0.2V or V_{CC} − 0.2V			200	μA
V_{IL}		Input Low Voltage		−0.1		0.8	V
V_{IH}		Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	TTL	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
	CMOS	Output Low Voltage	I_{OL} = 10 μA			0.2	V
V_{OH}	TTL	Output High Voltage	I_{OH} = −400 μA	2.4			V
	CMOS	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.2			V
WRITE OPERATION							
I_{CCW}		V_{CC} Current (Write)	RDY/$\overline{Busy}$ = V_{OL}			20	mA

Capacitance T_A = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V		5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			10	pF

AC Test Conditions

Output Load	1 TTL gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V
Input Rise and Fall	5 ns

Read Mode AC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Conditions	NMC98C64-20			NMC98C64-25			NMC98C64-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200			250			350	ns
t_{CE}	Chip Enable Access Time	$\overline{OE}$ = V_{IL}			200			250			350	ns
t_{OE}	Output Enable Access Time	$\overline{CE}$ = V_{IL}			75			100			120	ns
t_{HZ}	Output in Hi-Z from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ or $\overline{OE}$ = V_{IL}			80			100			100	ns
t_{OH}	Output Hold from Address Change	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			0			0			ns
t_{TR}	Input Rise and Fall Time		3		50	3		50	3		50	ns (Notes 1 & 2)
t_{LZ}	Output Active from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ or $\overline{OE}$ = V_{IL}	20			20			20			ns

Write Mode AC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 10% (Note 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to $\overline{WE}$ Setup Time		10			ns
t_{AH}	Address to $\overline{WE}$ Hold Time		200			ns
t_{CS}	Write Setup Time		0			ns
t_{CH}	Write Hold Time		0			ns
t_{OES}	$\overline{OE}$ to $\overline{WE}$ Setup Time		30			ns
T_{OEH}	$\overline{OE}$ to $\overline{WE}$ Hold Time		200			ns
t_{WP}	Write Pulse Time		200			ns
t_{WPH}	Write Pulse High		200			ns
t_{DS}	Data Setup Time	$\overline{OE}$ = V_{IH}	100			ns
t_{DH}	Data Hold Time		20			ns
t_{DB}	Time to Device Busy				120	ns
t_{DLP}	Page Data Load Time		300		1000	µs (Note 4)
t_{WC}	Write Cycle Time				10	ms
t_{TR}	Input Rise and Fall Time		3		50	ns (Note 1 & 2)

Note 1: This parameter only sampled and not 100% tested.

Note 2: All input signals must transit from V_{IL} to V_{IH} or from V_{IH} to V_{IL} in a monotonic manner. Transition times are measured between V_{IL} (max) and V_{IH} (min).

Note 3: Write cycles can be controlled by either $\overline{WE}$ or $\overline{CE}$. Timing Diagram on page 5 indicates $\overline{WE}$ controlled Write Cycle. For $\overline{CE}$ controlled Write Cycle (i.e. $\overline{CE}$ goes LOW after $\overline{WE}$ and goes HIGH before $\overline{WE}$) timing specs referenced to $\overline{WE}$ edges should be referenced to $\overline{CE}$ edges.

Note 4: Proper DL cycles are guaranteed up to Minimum t_{DLP} time. $\overline{CE}$ or $\overline{WE}$ DON'T CARE starts after Maximum t_{DLP} time.

Timing Waveforms

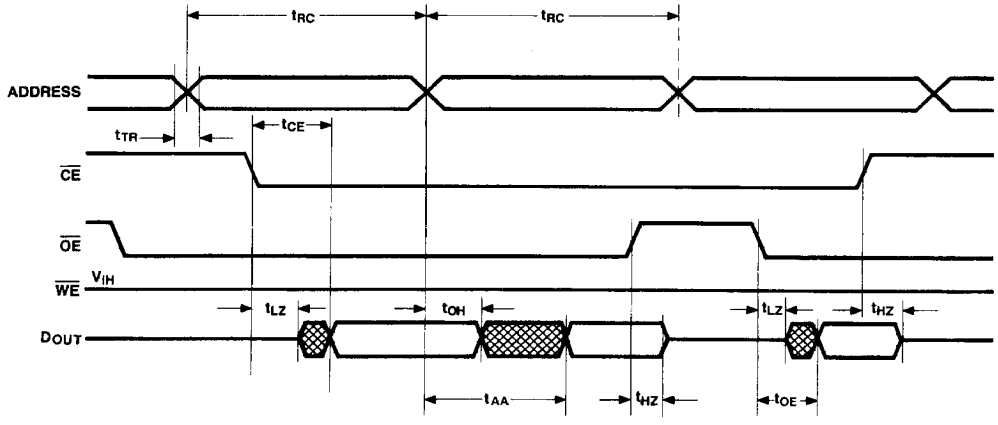


FIGURE 3. NMC98C64 Read Cycle Switching Time Waveforms

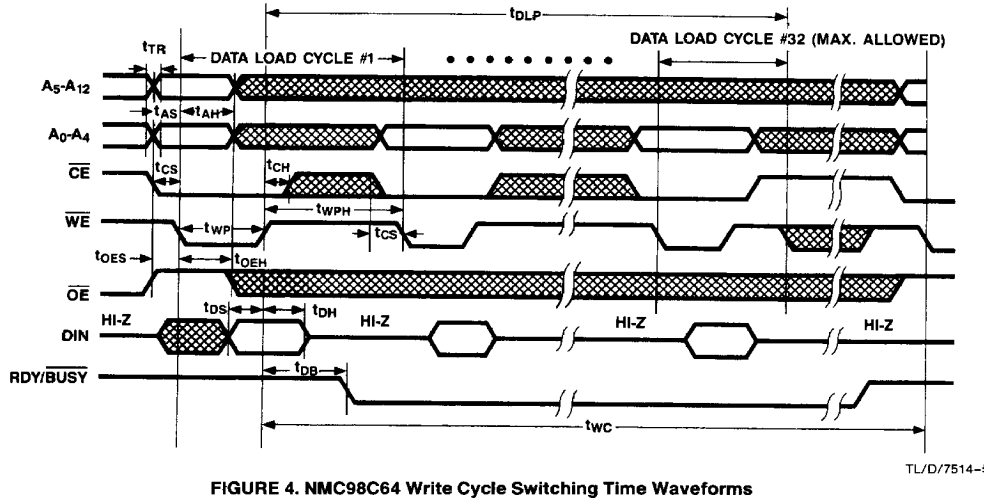


FIGURE 4. NMC98C64 Write Cycle Switching Time Waveforms