19-0874; Rev 0; 7/07

High-Voltage OVP with Battery Switchover

MAX4959/MAX4960

General Description

The MAX4959/MAX4960 overvoltage protection controllers protect low-voltage systems against high-voltage faults of up to +28V. When the input voltage exceeds the overvoltage lockout (OVLO) threshold, these devices turn off an external pFET to prevent damage to the protected components. The undervoltage lockout (UVLO) threshold holds the external pFET off until the input voltage rises to the correct level. An additional safety feature latches off the pFET when an incorrect low-power adapter is plugged in.

The MAX4959/MAX4960 control an external battery switchover pFET (P2) (see Figures 4 and 6) that switches in the battery when the AC adapter is unplugged. The undervoltage and overvoltage trip levels can be adjusted with external resistors.

The input is protected against ±15kV HBM ESD when bypassed with a 1µF ceramic capacitor to ground. All devices are available in a small 10-pin (2mm x 2mm) µDFN and 10-pin µMAX packages and are specified for operation over the extended -40°C to +85°C temperature range.

Applications

Notebooks

Laptops

Camcorders

Ultra-Mobile PCs

Features

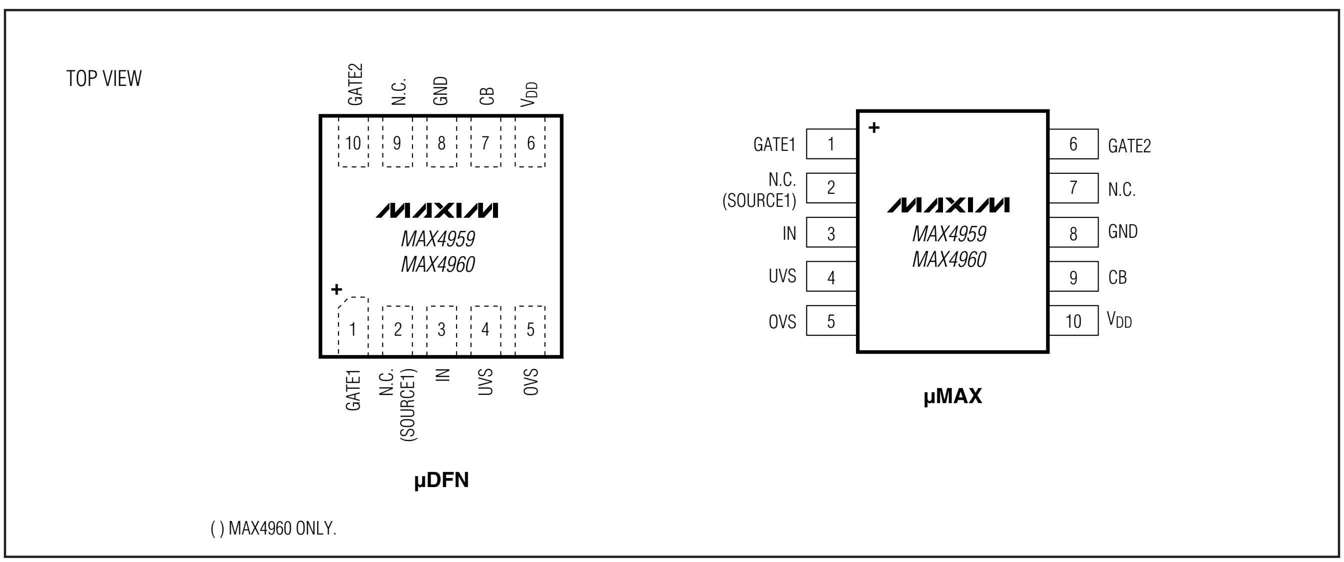
- ♦ **Overvoltage Protection Up to +28V**
- ♦ **± 2.5% Accurate Externally Adjustable OVLO/UVLO Thresholds**
- ♦ **Battery Switchover pFET Control**
- ♦ **Protection Against Incorrect Power Adapter**
- ♦ **Low (100µA Typ) Supply Current**
- ♦ **25ms Input Debounce Timer**
- ♦ **25ms Blanking Time**
- ♦ **10-Pin (2mm x 2mm) µDFN and 10-Pin µMAX Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX4959ELB+	-40°C to +85°C	10 µDFN	AAO	L1022-1
MAX4959EUB+*	-40°C to +85°C	10 µMAX	—	U10-1
MAX4960ELB+	-40°C to +85°C	10 µDFN	AAP	L1022-1
MAX4960EUB+*	-40°C to +85°C	10 µMAX	—	U10-1

+Denotes a lead-free package.
**Future product—Contact factory for availability.*

Pin Configurations



Typical Operating Circuits appear at end of data sheet.

For pricing delivery, and ordering information please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Voltage OVP with Battery Switchover

ABSOLUTE MAXIMUM RATINGS

IN, SOURCE1, GATE1, GATE2, to GND ....-0.3V to +30V
V_{DD} to GND ....-0.3V to +6V
UVS, OVS, CB to GND ....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
10-pin µDFN (derate 5.0mW/°C above +70°C) 403mW
10-pin µMAX (derate 5.6mW/°C above +70°C)...........444mW

Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +19V, T_A = -40°C to +85°C, unless otherwise noted, C_{VDD} = 100nF. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN						
Input Voltage Range	V_{IN}		4		28	V
Overvoltage Adjustable Trip Range	OVLO	(Note 2)	6		28	V
Overvoltage Comp Reference	OV_{REF}	V_{IN} rising edge	1.18	1.228	1.276	V
OVS Input Leakage Current	OVI_{LKG}		-100		+100	nA
Overvoltage Trip Hysteresis	OV_{HYS}			1		%
Undervoltage Adjustable Trip Range	UVLO	(Note 2)	5		28	V
Undervoltage Comp Reference	UV_{REF}	V_{IN} falling edge	1.18	1.228	1.276	V
UVS Input Leakage Current	UVI_{LKG}		-100		+100	nA
Undervoltage Trip Hysteresis	UV_{HYS}			1		%
Internal Undervoltage Trip Level	$INTUV_{REF}$	V_{IN} falling edge	4.1	4.4	4.7	V
Internal Undervoltage Trip Hysteresis	$INTUV_{HYS}$			1		%
Power-On Trip Level	POTL	V_{DD} > +3V, IN rising edge	0.5	0.75	1	V
Power-On Trip Hysteresis	$POTL_{HYS}$			10		%
IN Supply Current	I_{IN}	V_{IN} = +19V, V_{OVS} < OV_{REF} and V_{UVS} > UV_{REF}		100	300	µA
V_{DD}						
V_{DD} Voltage Range	V_{DD}		2.7		5.5	V
V_{DD} Undervoltage Lockout	V_{DDUVLO}	V_{DD} falling edge	1.55		2.40	V
V_{DD} Undervoltage Lockout Hysteresis	$V_{DDUVLOHYS}$			50		mV
V_{DD} Supply Current	I_{VDD}	V_{DD} = +5V, V_{IN} = 0V			10	µA
GATE_						
GATE1 Open-Drain MOS R_{ON} Resistance	R_{ON}	V_{CB} = 0V, V_{IN} = 19V, V_{OVS} < OV_{REF} and V_{UVS} > UV_{REF}, $I_{GATE\_}$ = 0.5mA (MAX4959)			1	kΩ
GATE2 Open-Drain MOS R_{ON} Resistance	R_{ON}	V_{CB} = 3V, $I_{GATE\_}$ = 0.5mA			1	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +19V, T_A = -40°C to +85°C, unless otherwise noted, C_{VDD} = 100nF. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE1 Leakage Current	$G1I_{LKG}$	$V_{OVS} > OV_{REF}$, $V_{UVS} < UV_{REF}$, or V_{CB} = +5V	-1		+1	µA
GATE2 Leakage Current	$G2I_{LKG}$	V_{CB} = 0V	-1		+1	µA
CB						
Logic-Level High	V_{IH}		1.5			V
Logic-Level Low	V_{IL}				0.4	V
CB Pulldown Resistor	R_{CBPD}		1	2	3	MΩ
TIMING						
Debounce Time	t_{DEB}	$V_{OVP} > V_{IN} > V_{UVP}$ for greater than t_{DEB} for GATE1 to go low	10	25	40	ms
GATE1 Assertion Delay from CB Pin	$t1_{GATE}$	CB = +3V to 0 rise time = fall time = 5ns (Note 3)		50		ns
GATE2 Assertion Delay from CB Pin	$t2_{GATE}$	CB = 0 to +3V rise time = fall time = 5ns (Note 3)		50		ns
Blanking Time	t_{BLANK}		10	25	40	ms
MAX4960						
SOURCE1/GATE1 Resistance	R_{SG}	(MAX4960)	140	200	260	kΩ
GATE1/Ground Resistance	R_{GG}	GATE1 Asserted (MAX4960)	140	200	260	kΩ

Note 1: Operation is tested at T_A= +25°C and guaranteed by design for µDFN package. Operation over specified temperature range is tested for µMAX package.

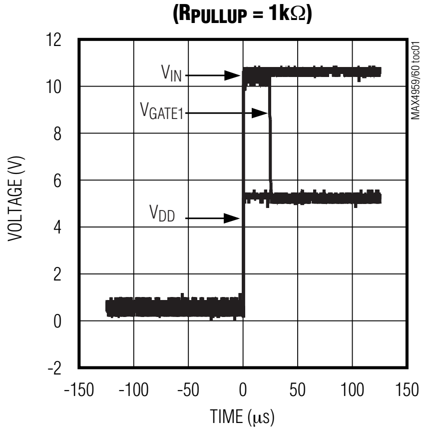
Note 2: Do not exceed absolute maximum rating; the ratio between the externally set OVLO and UVLO threshold must not exceed 4, $[OVLO/UVLO]_{MAX} \leq 4$.

Note 3: Assertion delay starts from switching of CB pin to reaching of 80% of GATE1/GATE2 transition. This delay is measured without external capacitive load.

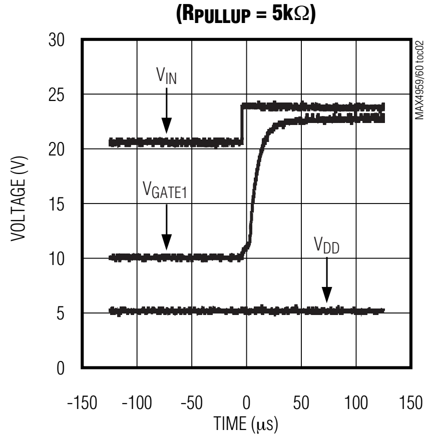
Typical Operating Characteristics

(V_{OVLO} = 22.2V and V_{UVLO} = 10.1V, R1 = 887kΩ, R2 = 66.5kΩ, R3 = 54.9kΩ, all resistors 1%, OV_{REF} = UV_{REF} = 1.228V.)

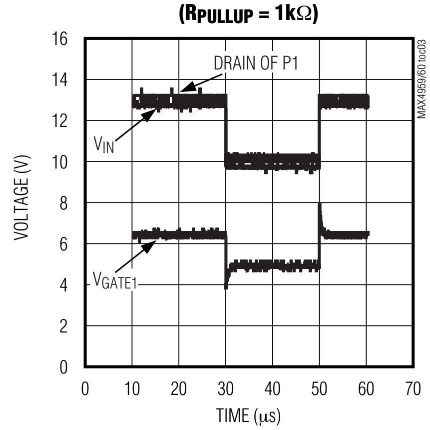
POWER-UP RESPONSE (R_{PULLUP} = 1kΩ)



OVERVOLTAGE RESPONSE (R_{PULLUP} = 5kΩ)



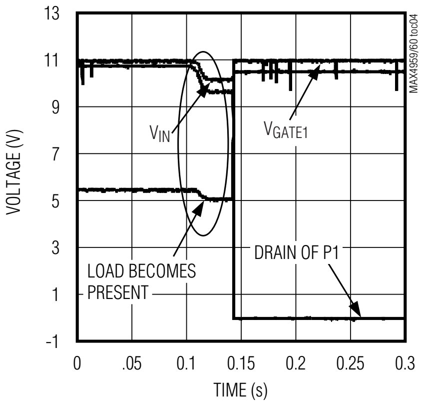
UNDERVOLTAGE RESPONSE (WITHIN BLANKING TIME) (R_{PULLUP} = 1kΩ)



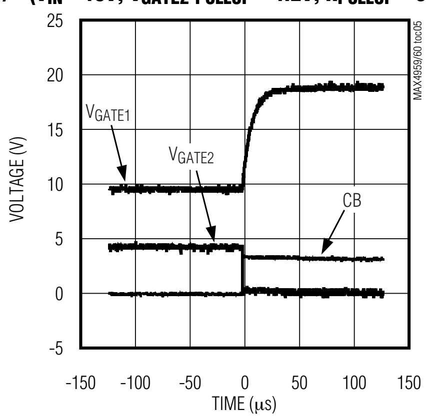
Typical Operating Characteristics (continued)

(V_{OVLO} = 22.2V and V_{UVLO} = 10.1V, R1 = 887kΩ, R2 = 66.5kΩ, R3 = 54.9kΩ, all resistors 1%, $OV_{REF} = UV_{REF}$ = 1.228V.)

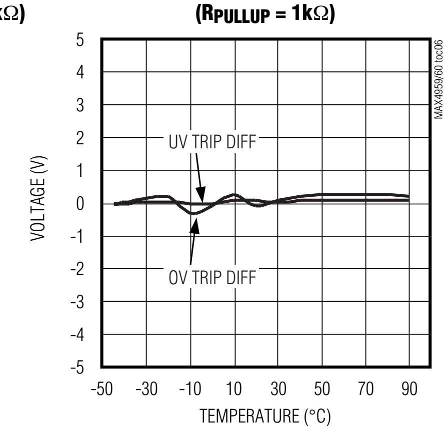
LOW-POWER ADAPTER RESPONSE (V_{OVLO} = 22.3V, V_{UVLO} = 10.1V, pFET = IRF7726)



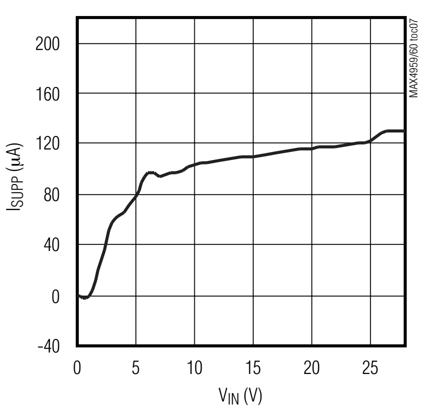
BATTERY SWITCHOVER WITH ADAPTER-PLUGGED RESPONSE (V_{IN} = 19V, $V_{GATE2-PULLUP}$ = 4.2V, R_{PULLUP} = 5kΩ)



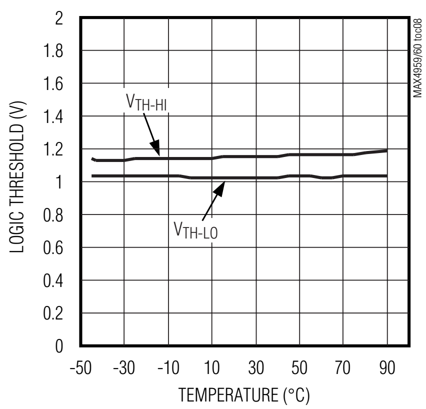
OVERVOLTAGE AND UNDERVOLTAGE TRIP DIFFERENCE vs. TEMPERATURE (R_{PULLUP} = 1kΩ)



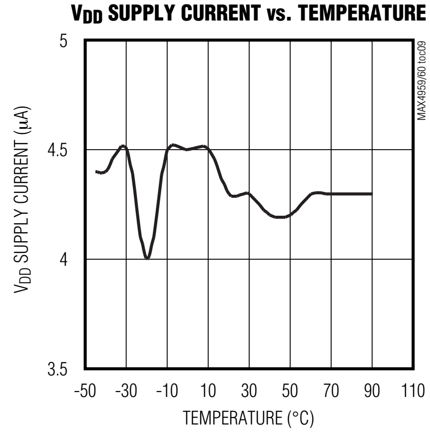
SUPPLY CURRENT vs. INPUT VOLTAGE



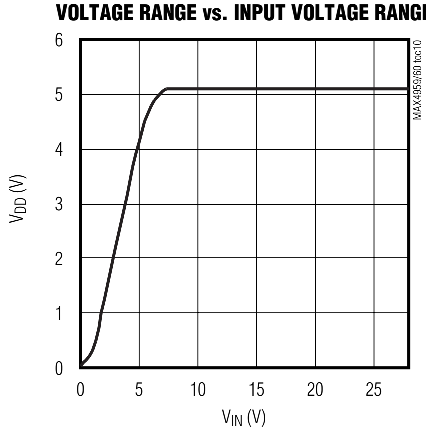
LOGIC-INPUT THRESHOLD vs. TEMPERATURE



V_{DD} SUPPLY CURRENT vs. TEMPERATURE



VOLTAGE RANGE vs. INPUT VOLTAGE RANGE



Pin Description

PIN		NAME	FUNCTION
MAX4959	MAX4960		
1	1	GATE1	pFET Gate Drive Output Open Drain. GATE1 is actively driven low, except during fault (OVP or UVP) condition (the external PFET is turned off). When $V_{UVLO} < V_{IN} < V_{OVLO}$, GATE1 is driven low (the external PFETP1 is turned on).
2, 9	9	N.C.	No Connection. Not internally connected. (Connect to ground or leave unconnected.)
—	2	SOURCE1	pFET Source Output. An internal resistor is connected between SOURCE1 and GATE1.
3	3	IN	Voltage Input. IN is both the power-supply input and the overvoltage/undervoltage sense input. Bypass IN to GND with a 1µF ceramic capacitor to get a ±15kV protected input. A minimum 0.1µF ceramic capacitor is required for proper operation.
4	4	UVS	Undervoltage Threshold Set Input. Connect UVS to an external resistive divider from IN to GND to set the undervoltage lockout threshold. (See *Typical Operating Circuits*.)
5	5	OVS	Overvoltage Threshold Set Input. Connect OVS to an external resistive divider from IN to GND to set the overvoltage lockout threshold. (See *Typical Operating Circuits*.)
6	6	V_{DD}	Internal Power-Supply Output. Bypass VDD to GND with a 0.1µF minimum capacitor. VDD powers the internal power-on reset circuits. (See the *V_{DD} Capacitor Selection* section.)
7	7	CB	Battery Switchover Control Input. When CB is high, GATE1 is high (P1 is off), and GATE2 is low (P2 is on). When CB is low, GATE1 is controlled by internal logic and GATE2 is high (P2 is off). GATE1 is controlled by CB only if $V_{ULO} < V_{IN} < V_{OVLO}$.
8	8	GND	Ground
10	10	GATE2	pFET Gate Drive Output, Open Drain. When CB is high, GATE2 is low (P2 is on). When CB is low, GATE2 is high impedance (P2 is off).

Detailed Description

The MAX4959/MAX4960 provide up to +28V overvoltage protection for low-voltage systems. When the input voltage exceeds the overvoltage trip level, the MAX4959/MAX4960 turn off an external pFET to prevent damage to the protected components.

The MAX4959/MAX4960 feature a control bit (CB) pin that controls an external battery-switchover function that switches in the battery when the adapter is unconnected. The host system detects when the battery switchover must take place and pulls CB high to turn on P2. The load current is not interrupted during battery switchover as the body diode of P2 conducts until the CB line is driven high (see the *MAX4959 Typical Operating Circuit 1*, Figure 4).

An additional safety feature latches off pFET P1 when a low-power adapter is plugged in. This protects the system from seeing repeated adapter insertions and removals when an incorrect low-power adapter is plugged in that cannot provide sufficient current.

Undervoltage Lockout (UVLO)

The MAX4959/MAX4960 have an adjustable undervoltage lockout threshold ranging from +5V to +28V. When V_{IN} is less than the V_{UVLO}, the device waits for a blanking time, t_{BLANK}, to see if the fault still exists. If the fault does not exist at the end of t_{BLANK}, P1 remains on. If V_{IN} is less than V_{UVLO} for longer than the blanking time, the device turns P1 off and P1 does not turn on again until $V_{IN} < 0.75V$. See Figure 1.

Overvoltage Lockout (OVLO)

The MAX4959/MAX4960 have an adjustable overvoltage lockout threshold ranging from +6V to +28V. When V_{IN} is greater than the V_{OVLO}, the device turns P1 off immediately. When V_{IN} drops below V_{OVLO}, P1 turns on again after the debounce time has elapsed.

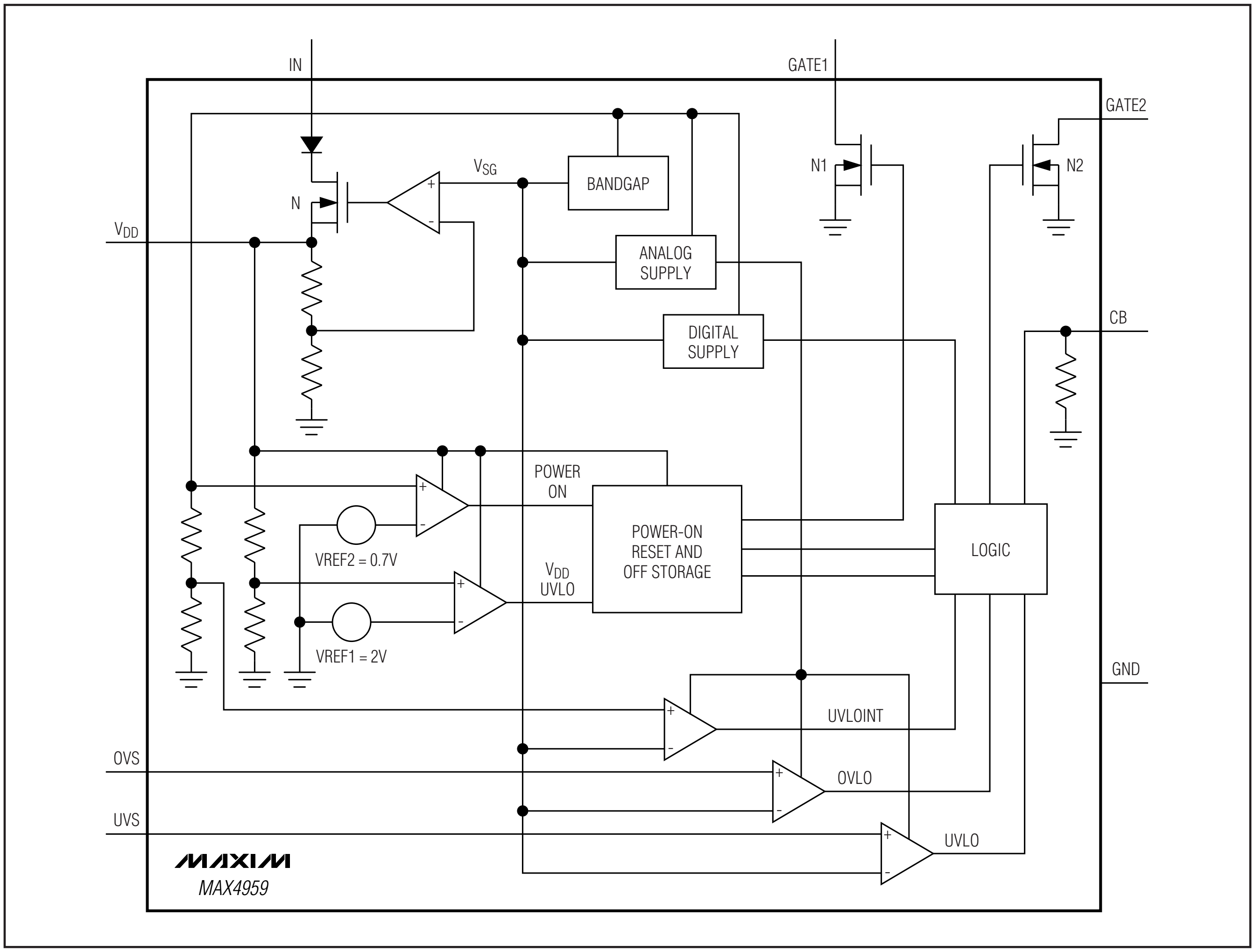
Device Operation

High-Voltage Adapter ($V_{IN} > V_{OVLO}$)

If an adapter with a voltage higher than V_{OVLO} is plugged in, the MAX4959/MAX4960 is in an OVP condition, so P1 is kept off or immediately turned off. There is

Functional Diagrams

Functional Diagram for the MAX4959



no blanking time for OVP, but the debounce time applies once the IN voltage falls below V_{OVLO} but above V_{UVLO}. When the voltage at IN is higher than V_{OVLO}, the CB pin does not control P1.

Correct Adapter ($V_{UVLO} < V_{IN} < V_{OVLO}$)

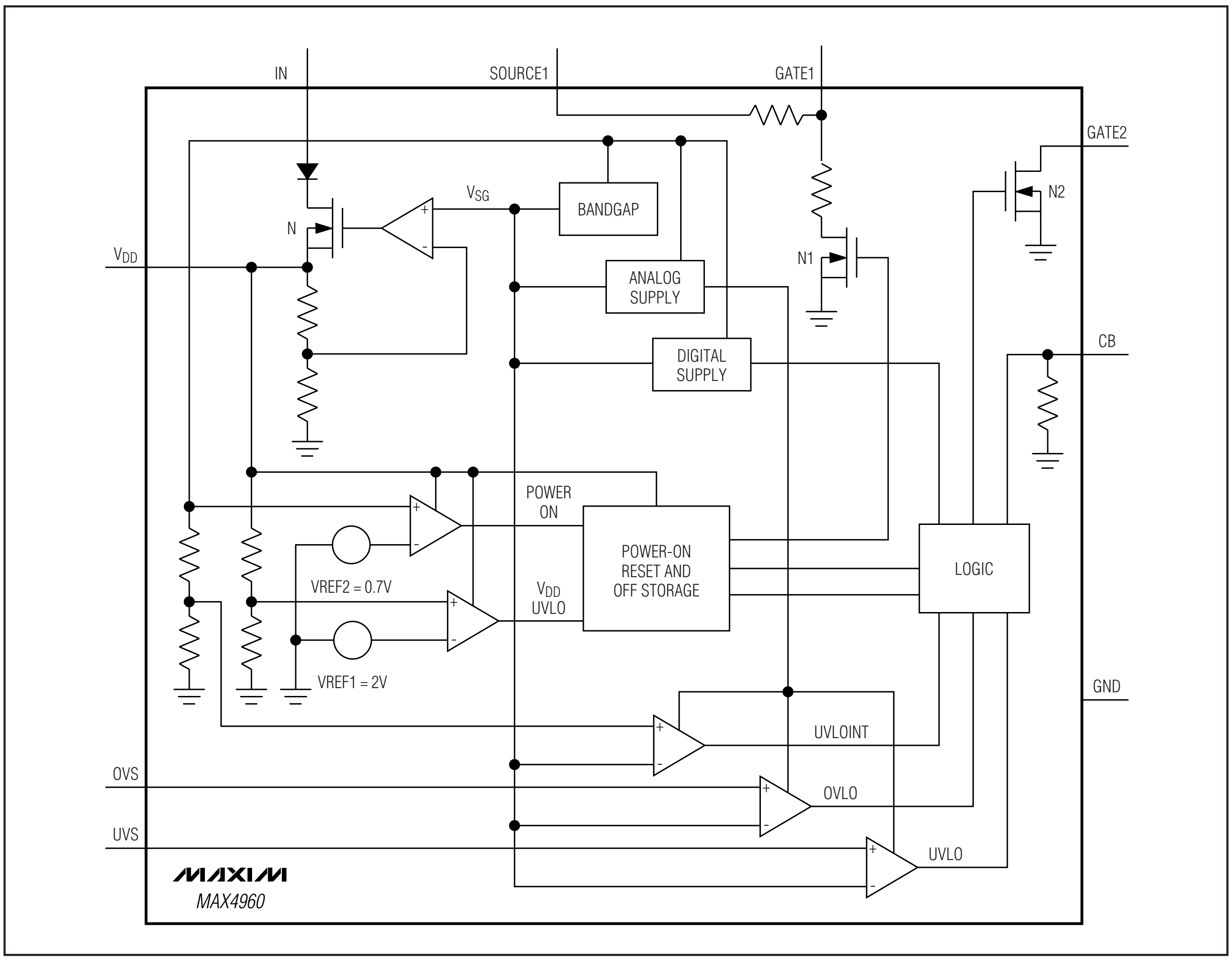
In this case, when the adapter is plugged in, the device goes through a 20ms (typ) debounce time and ensures that the voltage at IN is between V_{UVLO} and V_{OVLO} before P1 is turned on. In this state, the CB pin controls both P1 and P2.

Low-Power Adapter or Glitch Condition

If the adapter has the correct voltage but not enough power (incorrect low-power adapter), the MAX4959/MAX4960 protect pFET P1 from oscillation. When the adapter is first plugged in, P1 is off so the voltage is correct. When P1 is turned on after the debounce time, the low-power adapter is dragged down to below V_{UVLO}. The device waits for a 10ms blanking time to make sure it is not a temporary glitch, and, if a fault still exists, it latches off P1. P1 does not turn on again until the adapter is unplugged (V_{IN}<~0.75V) and plugged in again. This feature can work without the battery present

Functional Diagrams (continued)

Functional Diagram for the MAX4960



only if the backup capacitor on V_{DD} is large enough to maintain power for greater than the 10ms blanking time. The detection that the adapter is unplugged and plugged in again is implemented by monitoring the V_{IN} signal. The adapter is unplugged when V_{IN} drops below V_{IN} =~ 0.75V, and it is plugged in when V_{IN} becomes greater than V_{IN} =~ 0.75V. To ensure the monitoring of this lower threshold, an external storage capacitor at the V_{DD} pin is necessary. When the input voltage V_{IN} drops below 4V, power for some internal V_{IN} monitoring circuitry is supplied by the external capacitor at the V_{DD} pin. This capacitor is supplied by V_{IN} through a diode and is internally limited to 5.5V.

Adapter Not Present (V_{IN} < V_{UVLO})

When the input voltage V_{IN} drops below 4.4V, P1 is turned off automatically and P1 does not turn on again until the adapter is unplugged (V_{IN}<~0.75V) and plugged in again. When the adapter is not present, P1 is kept off with the gate-source resistor (which is internal for the MAX4960 and external for the MAX4959), and the CB pin controls the battery switchover pFET P2.

High-Voltage OVP with Battery Switchover

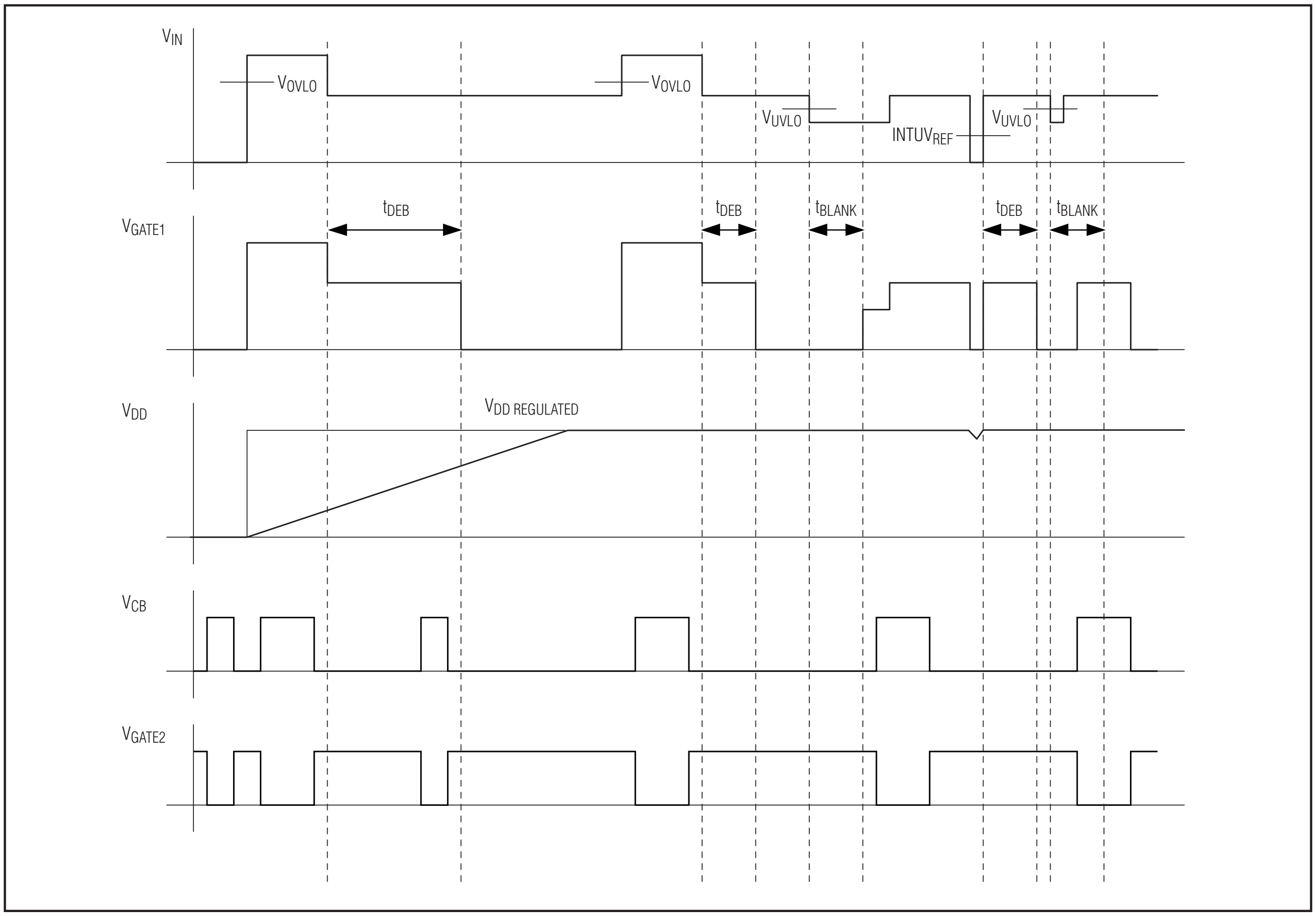


Figure 1. Timing Diagram

The following table lists the different modes of operations:

IN RANGE	P1 STATE	P2 STATE
$V_{IN} > V_{OVLO}$	P1 OFF (not affected by CB)	CB = 1 -> P2 is ON CB = 0 -> P2 is OFF
$V_{UVLO} < V_{IN} < V_{OVLO}$ (debounce timeout ongoing)	P1 OFF (not affected by CB)	
$V_{UVLO} < V_{IN} < V_{OVLO}$ (debounce timeout elapsed)	CB = 1 -> P1 is OFF CB = 0 -> P1 is ON	
$V_{INTUVREF} < V_{IN} < V_{OVLO}$ (blanking timeout ongoing)	CB = 1 -> P1 is OFF CB = 0 -> P1 is ON	
$V_{INTUVREF} < V_{IN} < V_{OVLO}$ (blanking timeout elapsed)	P1 OFF (not affected by CB). P1 does not turn on again until adapter is unplugged (V_{IN} <~0.75V) and plugged in again.	
$V_{IN} < V_{INTUVREF}$	P1 OFF (not affected by CB). P1 does not turn on again until adapter is unplugged (V_{IN} <~0.75V) and plugged in again.	

Applications Information

MOSFET Configuration and Selection

The MAX4959/MAX4960 are used with a single MOSFET configuration as shown in the *Typical Operating Circuits* to regulate voltage as a low-cost solution.

The MAX4959/MAX4960 are designed with pFETs. For lower on-resistance, the external MOSFET can be multiple pFETs in parallel. In most situations, MOSFETs with $R_{DS(ON)}$ specified for a V_{GS} of 4.5V work well. Also, MOSFETs (with $V_{DS} \geq 30V$) withstand the full +28V IN range of the MAX4959/MAX4960.

Resistor Selection for Overvoltage/Undervoltage Window

The MAX4959/MAX4960 include undervoltage and overvoltage comparators for window detection (see Figure 4). GATE1 is enhanced and after the debounce time, the pFET is turned on when the monitored voltage is within the selected window.

The resistor values R1, R2, and R3 can be calculated as follows:

$$V_{UVLO} = (UV_{REF})\left(\frac{R_{TOTAL}}{R2 + R3}\right)$$

$$V_{OVLO} = (OV_{REF})\left(\frac{R_{TOTAL}}{R3}\right)$$

where $R_{TOTAL} = R1 + R2 + R3$.

Use the following steps to determine the values for R1, R2, and R3:

1) Choose a value for R_{TOTAL}, the sum of R1, R2, and R3. Because the MAX4959/4960 have very high input impedance, R_{TOTAL} can be up to 5MΩ.
2) Calculate R3 based on R_{TOTAL} and the desired V_{OVLO} trip point:

$$R3 = \frac{OV_{REF} \times R_{TOTAL}}{V_{OVLO}}$$

3) Calculate R2 based on R_{TOTAL}, R3, and the desired V_{UVLO} trip point:

$$R2 = \left[\frac{UV_{REF} \times R_{TOTAL}}{V_{UVLO}}\right] - R3$$

4) Calculate R1 based on R_{TOTAL}, R2, and R3:

$$R1 = R_{TOTAL} - R2 - R3$$

Note that the ratio between the externally set OVLO and UVLO threshold must not exceed:

$$4\ [V_{OVLO} / V_{UVLO}]_{MAX} \leq 4)$$

V_{DD} Capacitor Selection

V_{DD} is regulated to +5V by a linear regulator. Since the minimum external adjustable UVLO trip threshold is +5V, the V_{DD} range is +5V to +28V and the value at V_{DD} is:

$V_{DD} = V_{IN} - 0.8V$ where V_{IN} = 5V to 5.8V

$V_{DD} = +5V$ where $V_{IN} > 5.8V$

The capacitor at V_{DD} must be large enough to provide power to the device for an external settable time, t_{HOLD}, when V_{IN} drops to 0V. The capacitor value to have a minimum time of t_{HOLD} is:

$$C = (I_{VDD} \times t_{HOLD}) / (V_{DD} - V_{DD}UVLO)$$

The worst case scenario is where V_{IN} = +5V, $V_{DD} = V_{IN}$ - 0.8V = +4.2V, I_{VDD} = 10μA (max). For a t_{HOLD} time of 20ms, C = (10μA x 20ms) / (4.2V - 2.2V) = 100nF.

Note: The capacitor must be greater than 100nF for the internal regulator to be stable, and needs to have low ESR and low leakage current, for example, a ceramic capacitor.

IN Bypass Considerations

For most applications, bypass IN to GND with a 1μF ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit, and provide protection if necessary to prevent exceeding the +30V absolute maximum rating on V_{IN}.

The MAX4959/MAX4960 provide protection against voltage faults up to+28V, but this does not include negative voltages. If negative voltages are a concern, connect a Schottky diode from IN to GND to clamp negative input voltages.

ESD Test Conditions

The MAX4959/MAX4960 are protected from ±15kV Human Body Model ESD on IN when IN is bypassed to ground with a 1μF ceramic capacitor.

Human Body Model

Figure 2 shows the Human Body Model and Figure 3 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

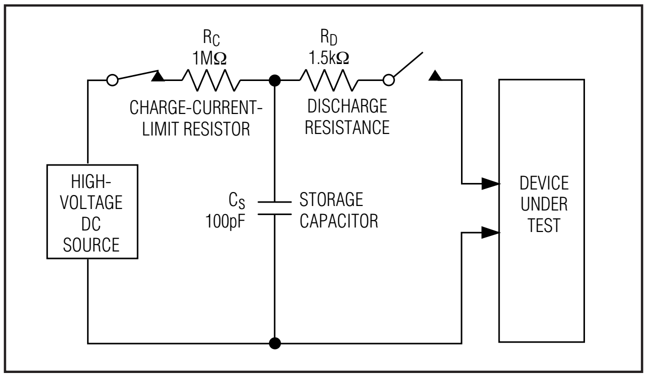


Figure 2. Human Body ESD Test Model

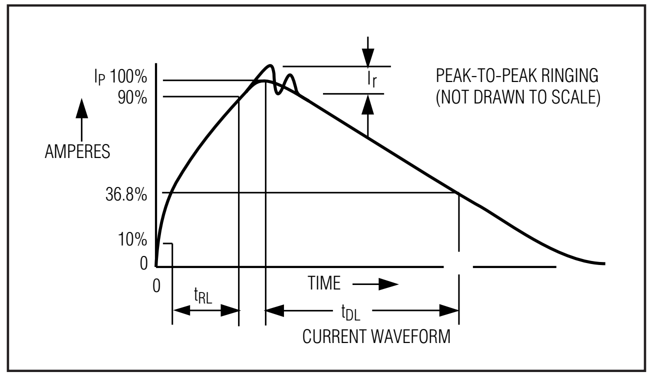


Figure 3. Human Body Current Waveform

Chip Information

PROCESS: BiCMOS

Typical Operating Circuits

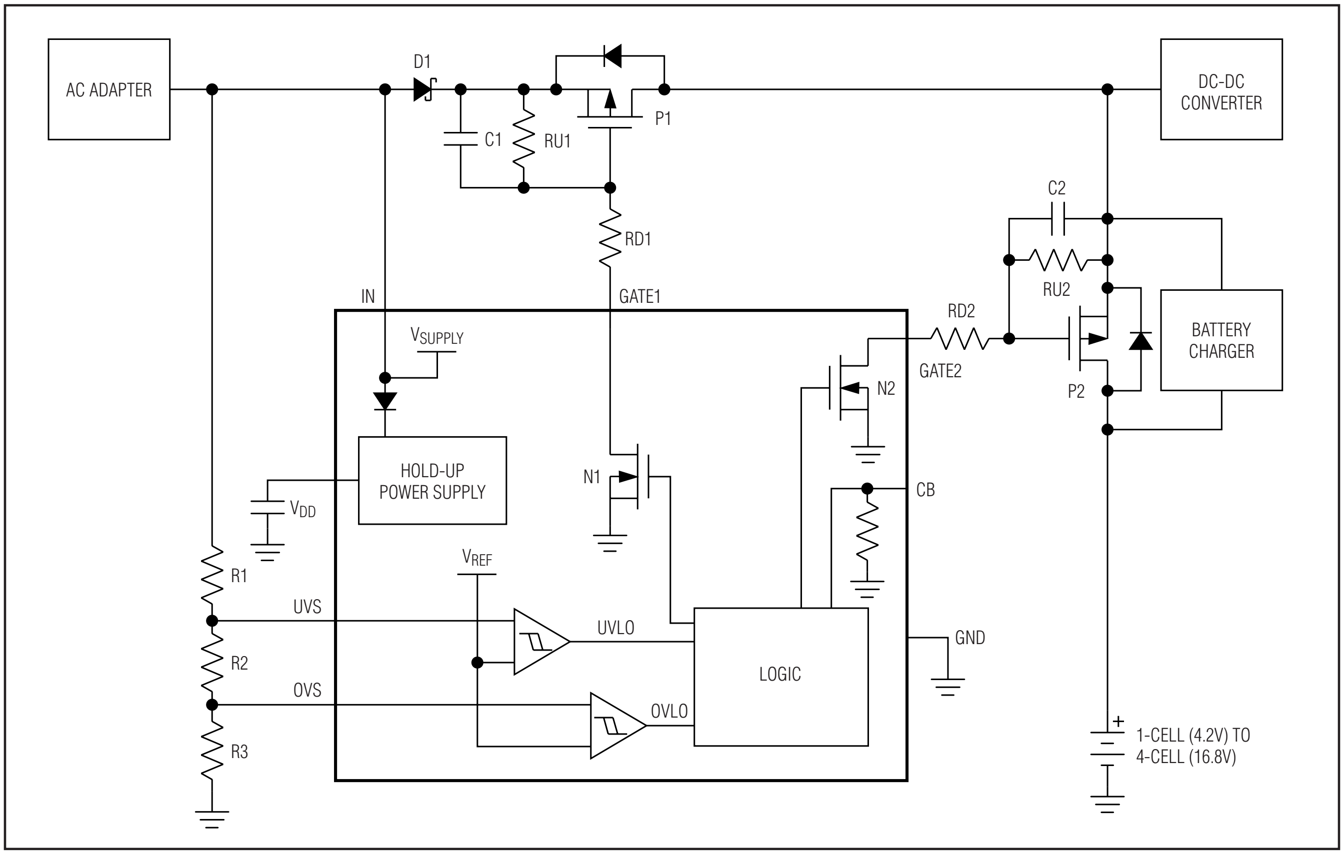


Figure 4. MAX4959 Typical Operating Circuit 1

High-Voltage OVP with Battery Switchover

Typical Operating Circuits (continued)

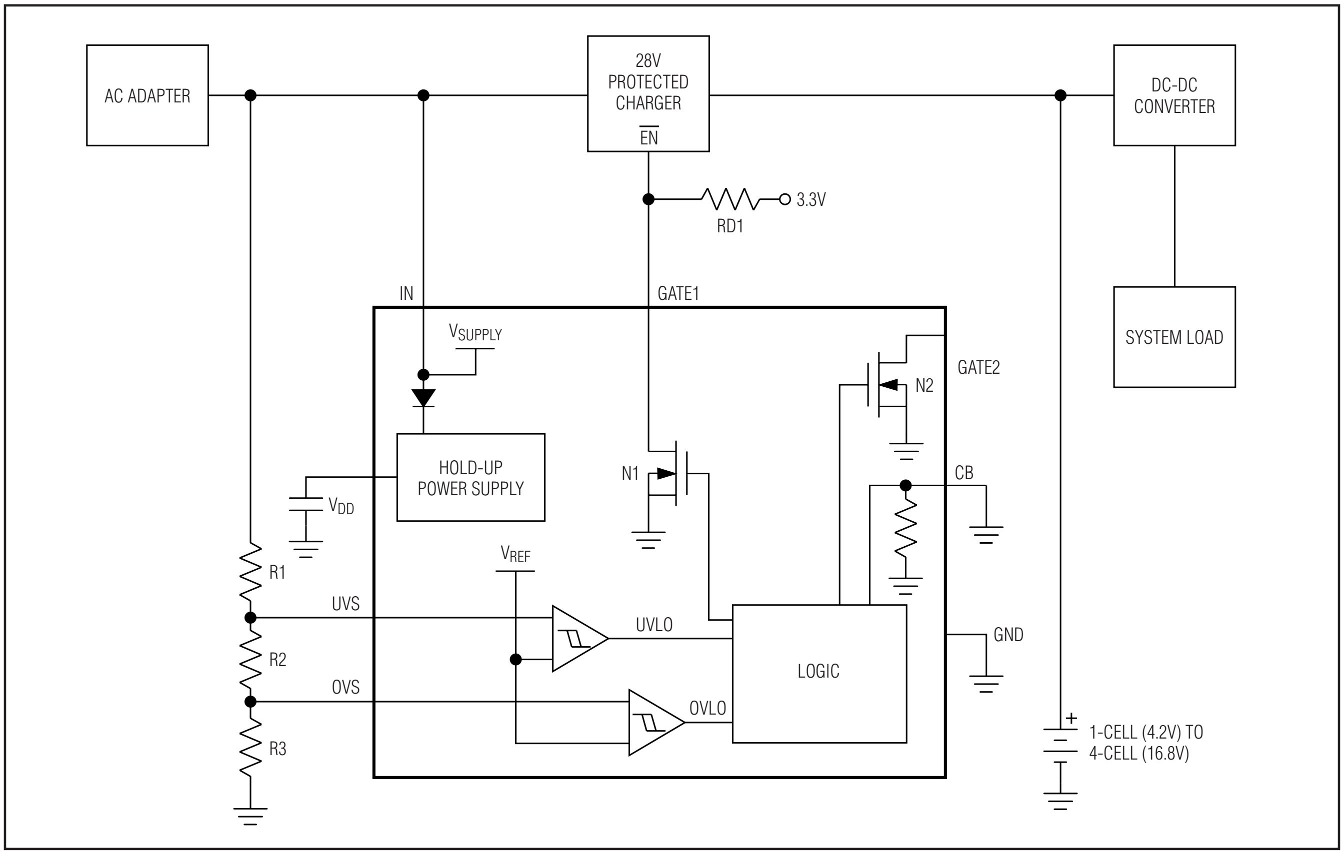


Figure 5. MAX4959 Typical Operating Circuit 2

Typical Operating Circuits (continued)

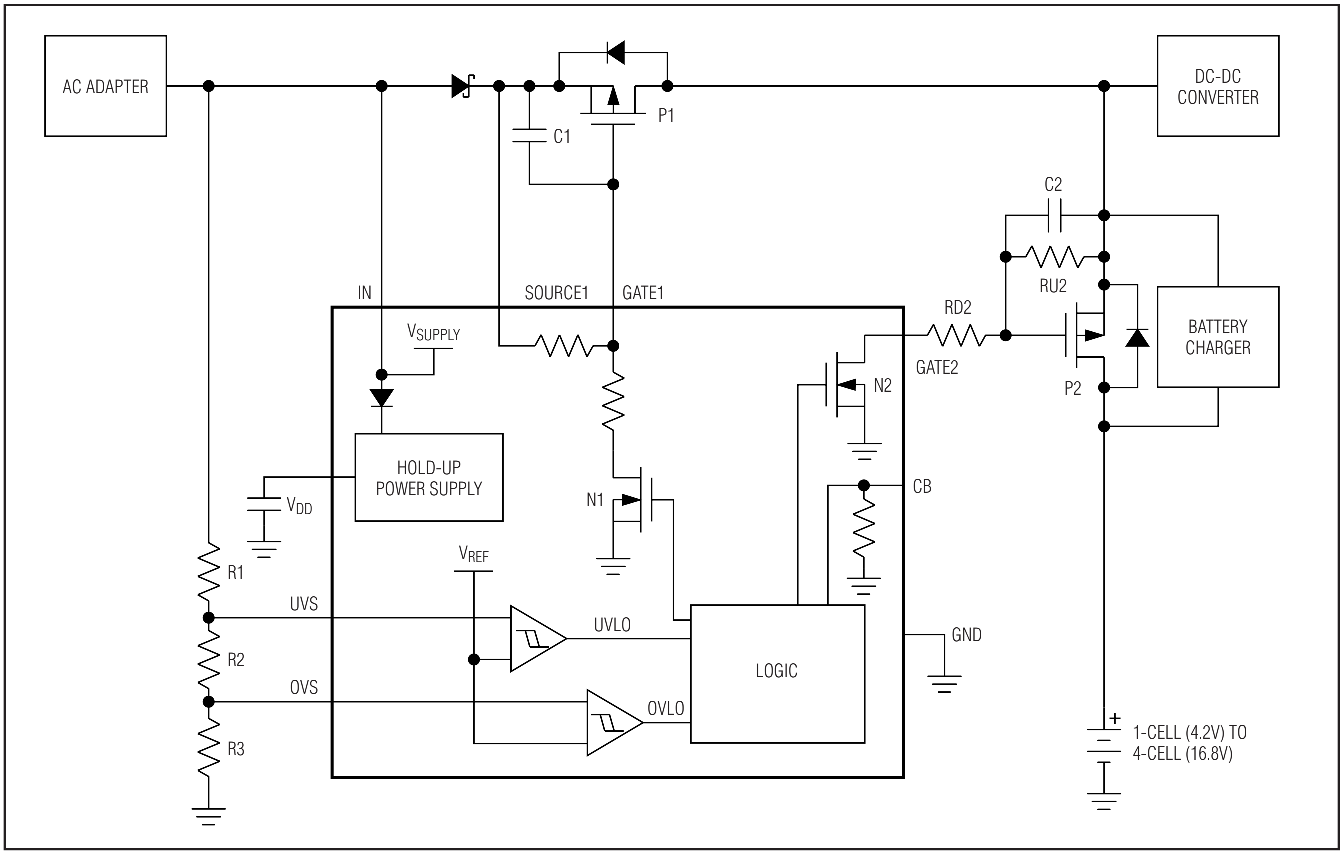


Figure 6. MAX4960 Typical Operating Circuit 1

High-Voltage OVP with Battery Switchover

Typical Operating Circuits (continued)

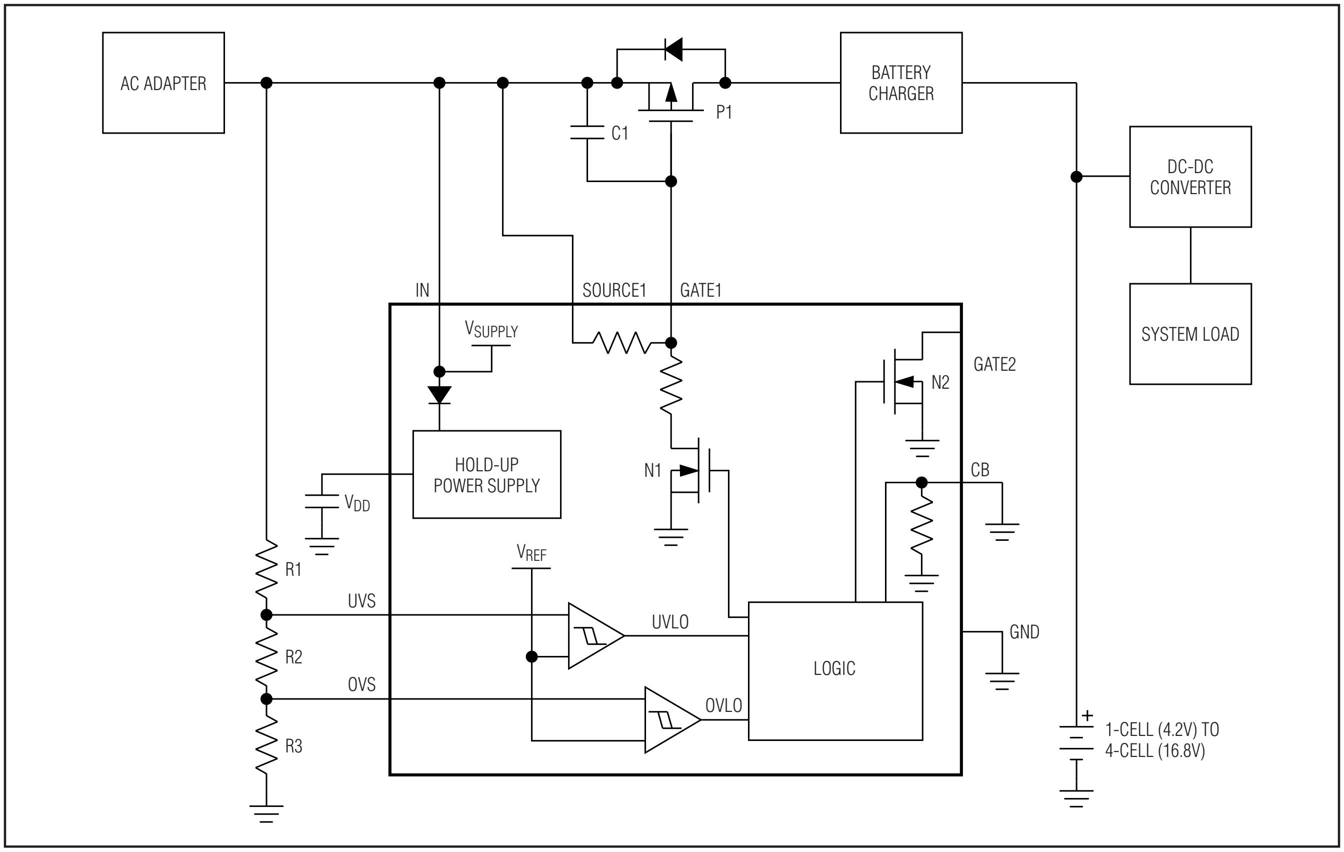
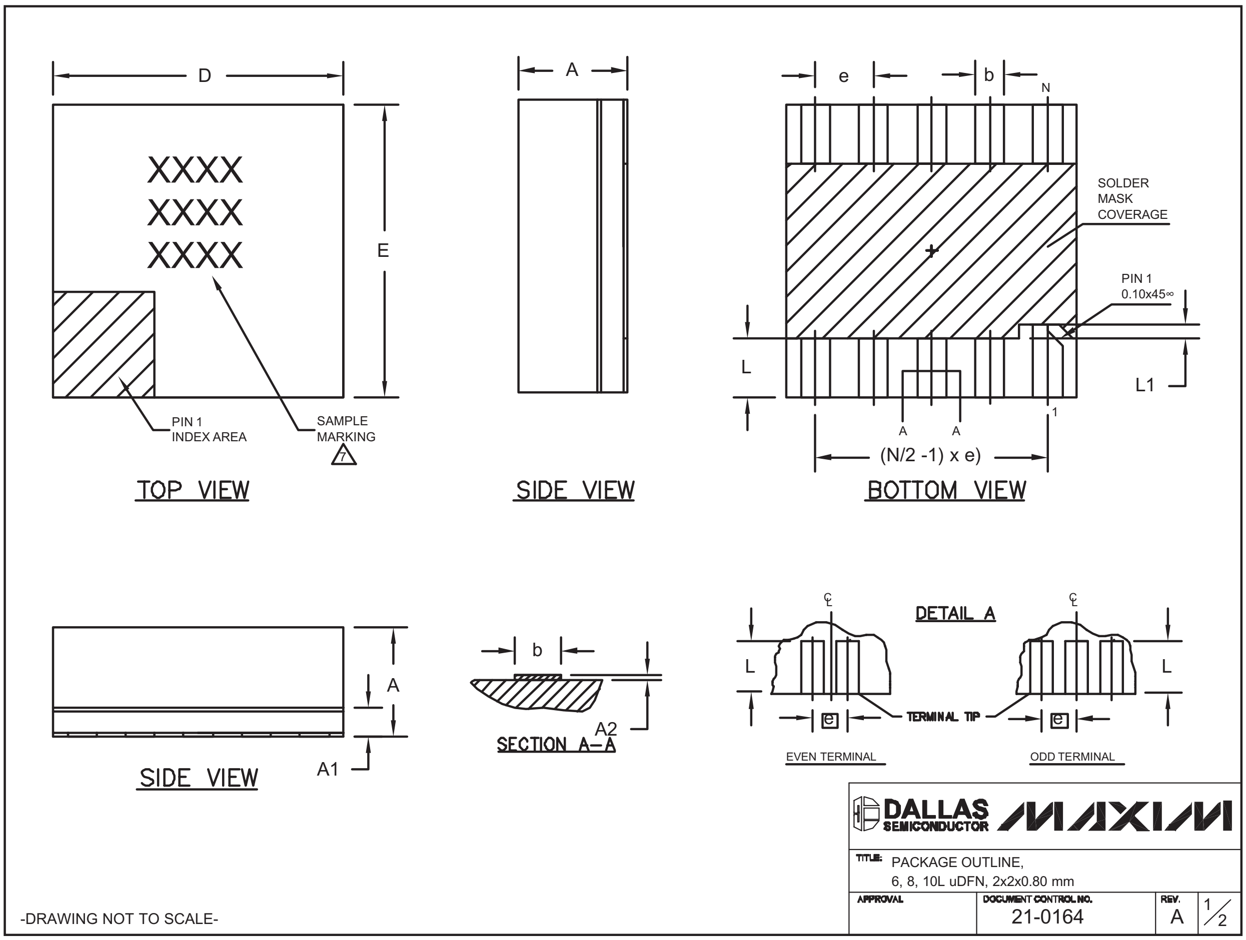


Figure 7. MAX4960 Typical Operating Circuit 2

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.15	0.20	0.25
A2	0.020	0.025	0.035
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.30	0.40	0.50
L1	0.10 REF.		

PACKAGE VARIATIONS				
PKG. CODE	N	e	b	(N/2 -1) x e
L622-1	6	0.65 BSC	0.30±0.05	1.30 REF.
L822-1	8	0.50 BSC	0.25±0.05	1.50 REF.
L1022-1	10	0.40 BSC	0.20±0.03	1.60 REF.

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6, 8, 10L uDFN, 2x2x0.80 mm

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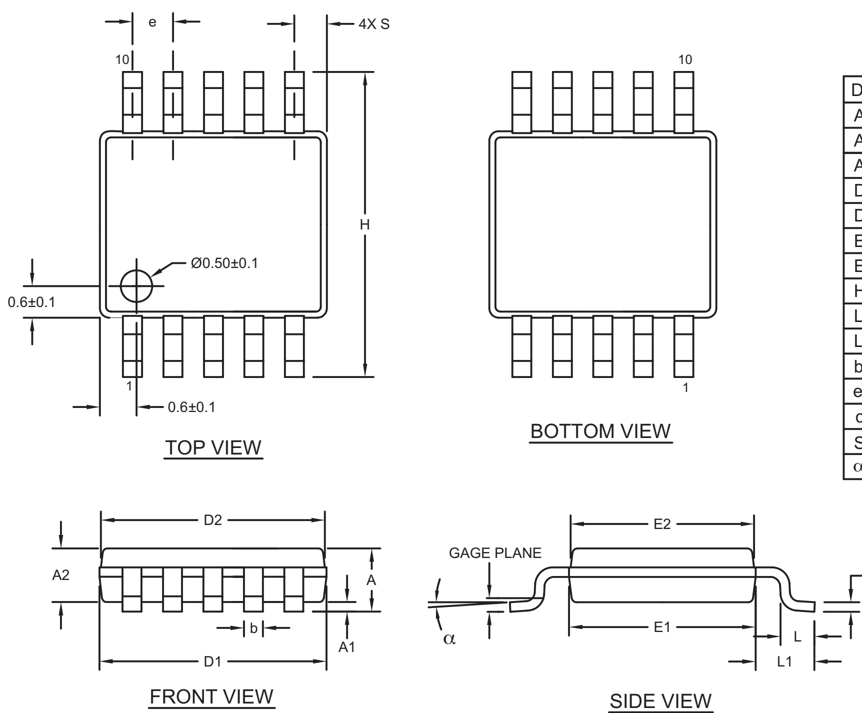
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

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	21-0061	I	1/1