

LH52256

LH52256L

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CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times:
70/90/120 ns (MAX.)
- Low power consumption:
Operating: 440/385/385 mW (MAX.)
Standby: 550 μW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
28-pin, 600-mil DIP
28-pin, 450-mil SOP

DESCRIPTION

The LH52256 is a low-power CMOS-periphery static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

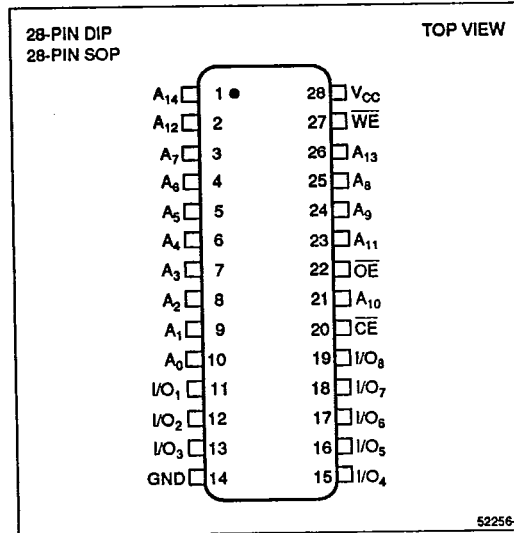


Figure 1. Pin Connections for DIP and SOP Packages

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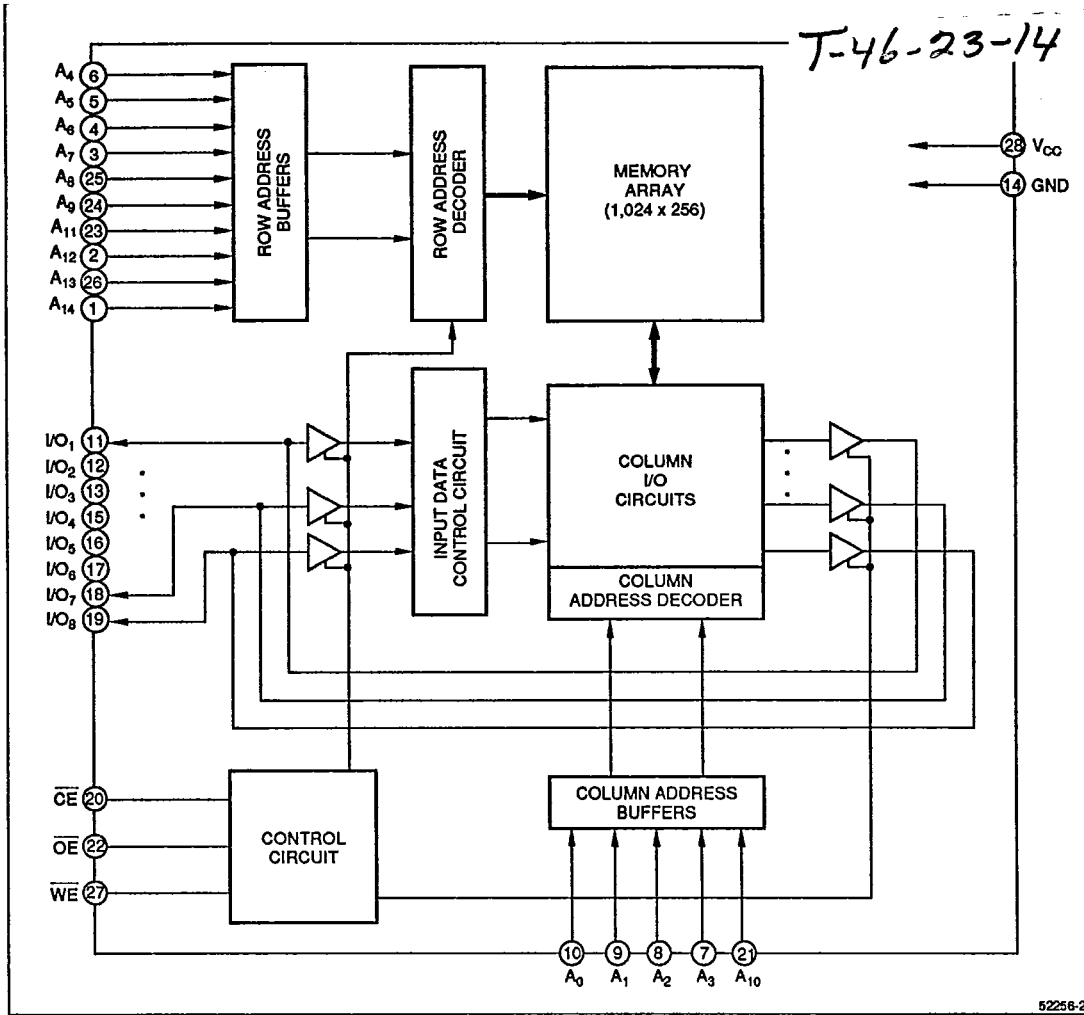


Figure 2. LH52256/LH52256L Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₄	Address inputs
\overline{CE}	Chip Enable input
\overline{WE}	Write Enable input
\overline{OE}	Output Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data inputs and outputs
V _{CC}	Power supply
GND	Ground

TRUTH TABLE

CE	WE	OE	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I _{SB})	1
L	H	L	Read	Dout	Operating (I _{CC})	
L	H	H	Output disable	High-Z	Operating (I _{CC})	
L	L	X	Write	Din	Operating (I _{CC})	1

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NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	0.3 to +7.0	V	1
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{IH}	2.2	3.5	V _{CC} + 0.3	V
	V _{IL}	-0.3		+0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	LH52256L-70 LH52256N-70L			LH52256L-90,-12 LH52256N-90L,-12L			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I _I	V _{CC} = 5.5 V _{IN} = 0 to V _{CC}			1			1	μA
Output leakage current	I _O	CE = V _{IH} or OE = V _{IH} , V _{IO} = 0 to V _{CC}			1			1	μA
Operating current	I _{CC}	CE = V _{IL} , Outputs open			80			70	mA
	I _{CC1}	V _{IH} = 3.5 V, V _{IL} = 0.6 V Outputs open			70			65	mA
	I _{CC2}	V _{IH} = 2.2 V, V _{IL} = 0.8 V Outputs open			80			70	mA
Standby current	I _{SB1}	CE = V _{IH}			3			3	mA
	I _{SB}	CE ≥ V _{CC} - 0.2			0.1			0.1	mA
Output voltage	V _{OL}	I _{OL} = 2 mA			0.4			0.4	V
	V _{OH}	I _{OH} = -1.0 mA	2.4			2.4			V

AC CHARACTERISTICS

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(1) READ CYCLE ($V_{CC} = 5V \pm 10\%$, $T_A = 0$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	LH52256L-70 LH52256N-70L		LH52256L-90 LH52256N-90L		LH52256L-12 LH52256N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	70		90		120		ns	
Address access time	t _{AA}		70		90		120	ns	
Chip enable access time	t _{ACE}		70		90		120	ns	
Output enable access time	t _{OE}		40		50		60	ns	
Output hold from address change	t _{OH}	10		10		10		ns	1
Chip enable Low to output in Low-Z	t _{LZ}	5		5		5		ns	1
Output enable Low to output in Low-Z	t _{OLZ}	5		5		5		ns	1
Chip disable to output in High-Z	t _{HZ}	0	35	0	40	0	45	ns	1
Output enable High to output in High-Z	t _{OHZ}	0	35	0	40	0	45	ns	1

(2) WRITE CYCLE ($V_{CC} = 5V \pm 10\%$, $T_A = 0$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	LH52256L-70 LH52256N-70L		LH52256L-90 LH52256N-90L		LH52256L-12 LH52256N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	70		90		120		ns	
Chip enable to end of write	t _{CW}	45		55		65		ns	
Address valid to end of write	t _{AW}	65		80		90		ns	
Address setup time	t _{AS}	0		0		10		ns	
Write pulse width	t _{WP}	45		55		65		ns	
Write recovery time	t _{WR}	5		5		10		ns	
Data valid to end of write	t _{DW}	30		30		35		ns	
Data hold time	t _{DH}	0		0		10		ns	
Output active from end of write	t _{OW}	5		5		5		ns	1
Write Low to output in High-Z	t _{WZ}	0	40	0	40	0	45	ns	1
Output enable High to output in High-Z	t _{OHZ}	0	35	0	40	0	45	ns	1

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a ± 500 mV transition from steady state levels into the test load. $C_{LOAD} = 5$ pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, $C_L = 100$ pF (Includes scope and jig capacitance)

DATA RETENTION CHARACTERISTICS (TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V _{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2 V$	2.0			V
Data retention current	I _{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2 V$, V _{CCDR} = 3.0 V		6	50	μA
Chip disable to data retention	t _{CDR}		0			ns
Recovery time	t _R		t _{RC} *			ns

* t_{RC} = Read cycle time

CAPACITANCE¹ (TA = 25°C, f = 1MHz)

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PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input capacitance	C _{IN}	V _{IN} = 0 V	8	pF
Input/output capacitance	C _{IO}	V _{IO} = 0 V	10	pF

NOTE:

1. This parameter is sampled and not production tested.

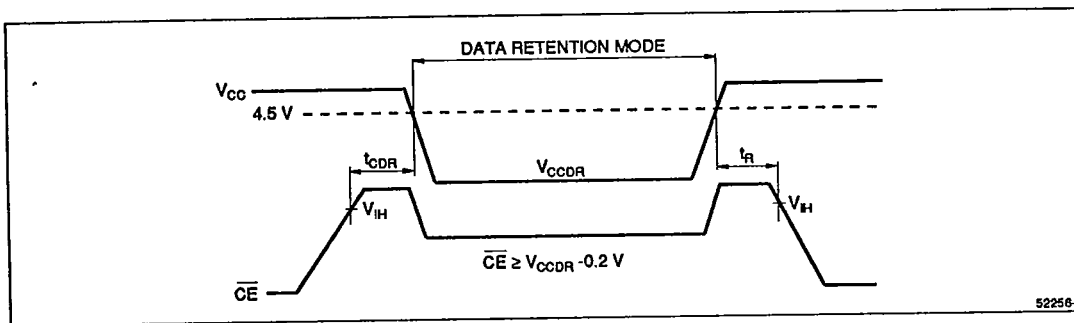
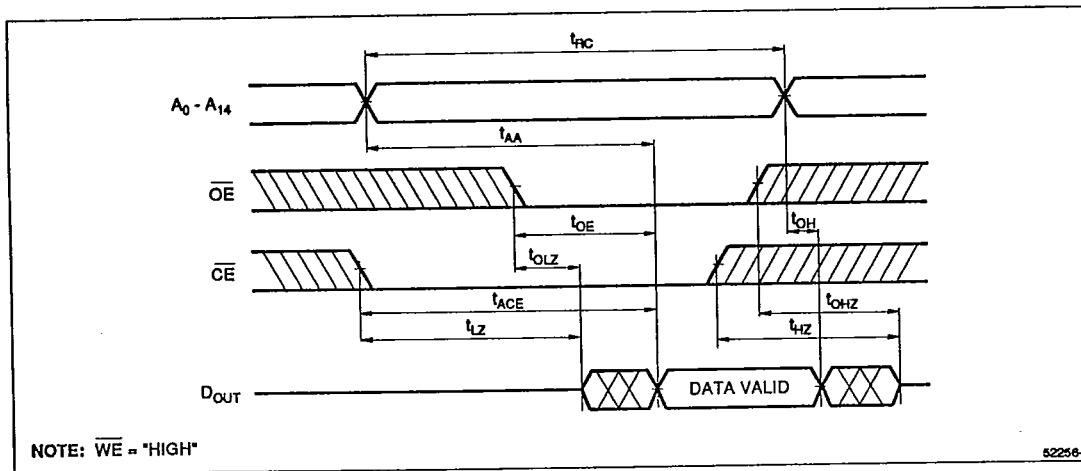


Figure 3. Low Voltage Data Retention



NOTE: \overline{WE} = "HIGH"

Figure 4. Read Cycle

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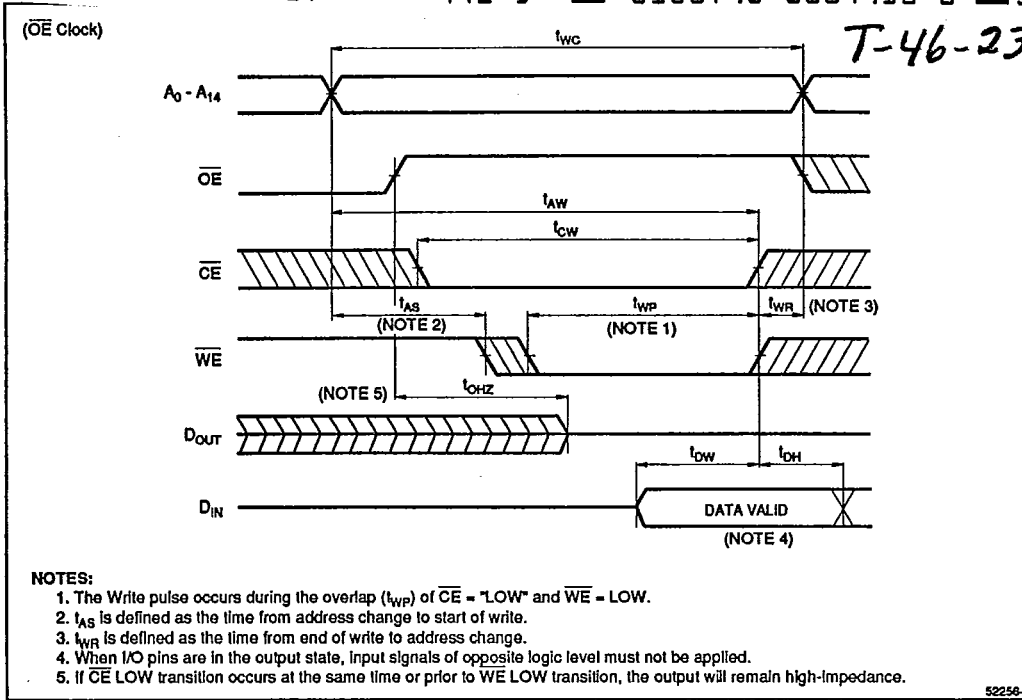


Figure 5. Write Cycle 1

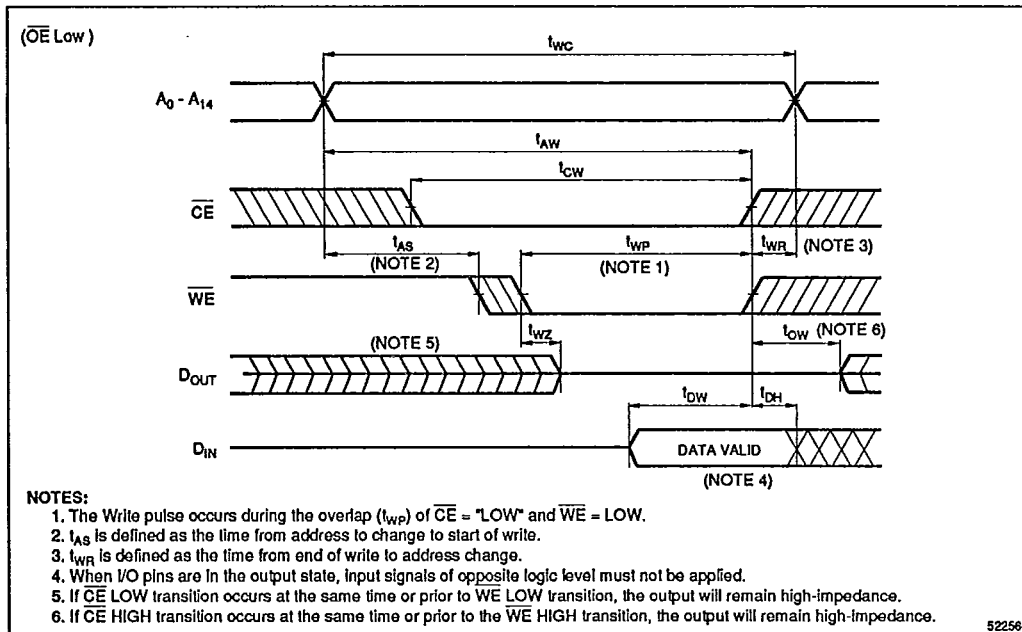


Figure 6. Write Cycle 2

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