SHARP

	Date Aug.	8. 2002
Preliminary Dat	TAQUEET	
F NELIMINAN'I DA	DATASHEET	
	64M (x16) Flash Memory	
MODEL NO :	LH28F640BFHE-PBTL80	
	bject to change without notice.	
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- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.
 - The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
 - Office electronics
 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliance
 - Communication equipment other than for trunk lines
 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
 - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.
 - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.
 - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.

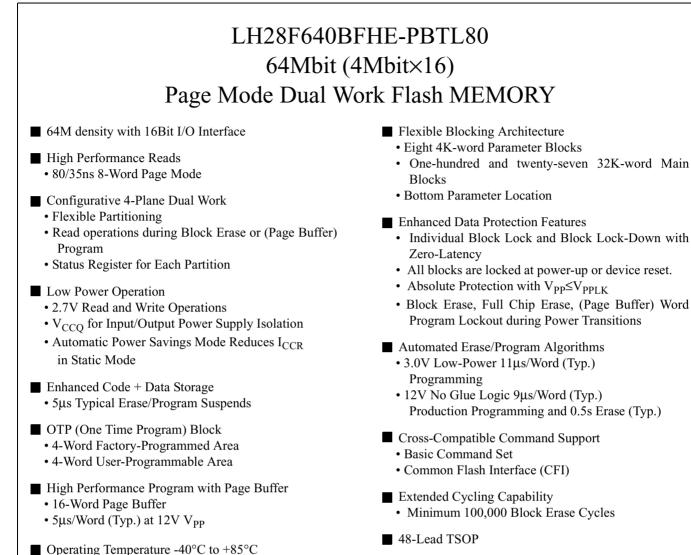
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- CMOS Process (P-type silicon substrate)
- ETOX^{TM*} Flash Technology
- Not designed or rated as radiation hardened

The product, which is 4-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC} =2.7V-3.6V and V_{PP} =1.65V-3.6V or 11.7V-12.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states. Furthermore, its newly configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

* ETOX is a trademark of Intel Corporation.

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A15 1 A14 2 A13 3 A12 4 A11 5 A10 6 A9 7 A8 8 A20 10 WE# 11 RST# 12 VPP 13 WP# 14 A19 15 A18 16 A17 17 A7 18 A6 19 A5 20 A1 22 A2 23 A1 24	48-LEAD TSOP STANDARD PINOUT 12mm x 20mm TOP VIEW	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

Figure 1. 48-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

Symbol	Туре	Name and Function
A ₀ -A ₂₁	INPUT	ADDRESS INPUTS: Inputs for addresses. 64M: A ₀ -A ₂₁
DQ ₀ -DQ ₁₅	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command Use Interface) write cycles, outputs data during memory array, status register, query code identifier code and partition configuration register code reads. Data pins float to high impedance (High Z) when the chip or outputs are deselected. Data is internally latche during an erase or program cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
RST#	INPUT	RESET: When low (V_{IL}) , RST# resets internal automation and inhibits write operation which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# mu be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first).
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL} , locked-down blocks cannot be unlocked. Eras or program operation can be executed to the blocks which are not locked and not locked down. When WP# is V_{IH} , lock-down is disabled.
V _{PP}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V _{PP} is not used for power supply pi With V _{PP} \leq V _{PPLK} , block erase, full chip erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 12V \pm 0.3V to V _{PP} provides fast erasing or fast programming mode. In th mode, V _{PP} is power supply pin. Applying 12V \pm 0.3V to V _{PP} during erase/program ca only be done for a maximum of 1,000 cycles on each block. V _{PP} may be connected to 12V \pm 0.3V for a total of 80 hours maximum. Use of this pin at 12V beyond these limit may reduce block cycling capability or cause permanent damage.
V _{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see D Characteristics) produce spurious results and should not be attempted.
V _{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (2.7V-3.6V): Power supply for all input/outpup pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
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	-		Simunuit	cous ope	number 1910	ues Allow		ur i iune	5		
			THEN 7	THE MO	DES ALL	OWED IN	THE OTI	HER PAI	RTITION I	S:	
IF ONE PARTITION IS:	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	
Read Array	Х	Х	Х	Х	Х	Х		Х		Х	Х
Read ID/OTP	Х	Х	Х	Х	Х	Х		Х		Х	Х
Read Status	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х
Read Query	Х	Х	Х	Х	Х	Х		Х		Х	Х
Word Program	Х	Х	Х	Х							Х
Page Buffer Program	Х	X	Х	Х							Х
OTP Program			Х								
Block Erase	Х	Х	Х	Х							
Full Chip Erase			Х								
Program Suspend	Х	X	Х	Х							Х
Block Erase Suspend	Х	Х	Х	Х	Х	Х				Х	

Table 2. Simultaneous Operation Modes Allowed with Four $Planes^{(1, 2)}$

"X" denotes the operation available.
 Configurative Partition Dual Work Restrictions:

Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition. Only one partition can be erased or programmed at a time - no command queuing. Commands must be written to an address within the block targeted by that command.

BLOCK NUMBER ADDRESS RANGE

	BL	OCK NUMBI	ER ADDRESS RANGE
	134	32K-WORD	3F8000H - 3FFFFFH
	134	32K-WORD	3F0000H - 3F7FFFH
	132	32K-WORD	3E8000H - 3EFFFFH
	131	32K-WORD	3E0000H - 3E7FFFH
	130	32K-WORD	3D8000H - 3DFFFFH
	129	32K-WORD	3D0000H - 3D7FFFH
	128	32K-WORD	3C8000H - 3CFFFFH
	127 126	32K-WORD	3C0000H - 3C7FFFH 3B8000H - 3BFFFFH
Ē	120	32K-WORD 32K-WORD	3B0000H - 3B7FFFH
PLANE3 (UNIFORM PLANE)	123	32K-WORD	3A8000H - 3AFFFH
	123	32K-WORD	3A0000H - 3A7FFFH
E	122	32K-WORD	398000H - 39FFFFH
Σ	121	32K-WORD	390000H - 397FFFH
1×	120	32K-WORD	388000H - 38FFFFH
L C L	119	32K-WORD	380000H - 387FFFH
E	118	32K-WORD	378000H - 37FFFFH
15	117	32K-WORD	370000H - 377FFFH
	116	32K-WORD	368000H - 36FFFFH
EB-	115 114	32K-WORD 32K-WORD	360000H - 367FFFH 358000H - 35FFFFH
	114	32K-WORD	350000H - 357FFFH
	112	32K-WORD	348000H - 34FFFFH
L I	111	32K-WORD	340000H - 347FFFH
	110	32K-WORD	338000H - 33FFFFH
	109	32K-WORD	330000H - 337FFFH
	108	32K-WORD	328000H - 32FFFFH
	107	32K-WORD	320000H - 327FFFH
	106	32K-WORD	318000H - 31FFFFH
	105 104	32K-WORD	310000H - 317FFFH
	104	32K-WORD 32K-WORD	308000H - 30FFFFH 300000H - 307FFFH
	105	J2K-WORD	50000011 - 507171711
		221/ WORD	26800011 26666611
	102	32K-WORD 32K-WORD	2F8000H - 2FFFFFH 2F0000H - 2F7FFFH
	101 100	32K-WORD	2E8000H - 2EFFFH
	99	32K-WORD	2E0000H - 2E7FFH
	98	32K-WORD	2D8000H - 2DFFFFH
	97	32K-WORD	2D0000H - 2D7FFFH
	96	32K-WORD	2C8000H - 2CFFFFH
	95	32K-WORD	2C0000H - 2C7FFFH
	94	32K-WORD	2B8000H - 2BFFFFH
E	93	32K-WORD	2B0000H - 2B7FFFH
F	92	32K-WORD	2A8000H - 2AFFFFH
RM PLANE)	91 90	32K-WORD 32K-WORD	2A0000H - 2A7FFFH 298000H - 29FFFFH
L L	89	32K-WORD	290000H - 297FFFH
l ≩ l	88	32K-WORD	288000H - 28FFFFH
1Å	87	32K-WORD	280000H - 287FFFH
Ĕ	86	32K-WORD	278000H - 27FFFFH
IZ.	85	32K-WORD	270000H - 277FFFH
Ð	84	32K-WORD	268000H - 26FFFFH
10	83	32K-WORD	260000H - 267FFFH
Η	82	32K-WORD	258000H - 25FFFFH
PLANE2 (UNIFO	81	32K-WORD	250000H - 257FFFH
L	80	32K-WORD	248000H - 24FFFFH
	79 78	32K-WORD	240000H - 247FFFH 238000H - 23FFFFH
	77	32K-WORD 32K-WORD	230000H - 237FFFH
	76	32K-WORD	228000H - 22FFFFH
	75	32K-WORD	220000H - 227FFFH
	74	32K-WORD	218000H - 21FFFFH
	73	32K-WORD	210000H - 217FFFH
	72	32K-WORD	208000H - 20FFFFH
	71	32K-WORD	200000H - 207FFFH

70 32K-WORD 1F8000H - IFFFFH 69 32K-WORD 1E8000H - IFFFFH 67 32K-WORD 1E8000H - IEFFFH 66 32K-WORD 1D8000H - IDFFFFH 66 32K-WORD 1D8000H - IDFFFFH 66 32K-WORD 1D0000H - IDFFFFH 64 32K-WORD 1B8000H - IDFFFFH 63 32K-WORD 1B8000H - IDFFFFH 60 32K-WORD 18000H - IDFFFFH 59 32K-WORD 18000H - IBFFFH 59 32K-WORD 18000H - IBFFFH 50 32K-WORD 18000H - IBFFFH 53 32K-WORD 18000H - IBFFFH 53 32K-WORD 18000H - IBFFFH 53 32K-WORD 18000H - ISFFFH 40 32K-WORD 18000H - ISFFFH 41 32K-WORD 18000H - ISFFFH 42 32K-WORD 130000H - ISFFFH 43 32K-WORD 130000H - ISFFFH 43 32K-WORD 130000H - ISFFFH 43 32K-WORD			en en beneret	_
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68 32K-WORD IE8000H IEFFFH 67 32K-WORD ID8000H IDFFFH 66 32K-WORD ID8000H IDFFFH 63 32K-WORD IC8000H IDFFFFH 64 32K-WORD IC8000H IC7FFFH 63 32K-WORD IB8000H IDFFFFH 60 32K-WORD IA8000H IAFFFFH 60 32K-WORD IA8000H IAFFFFH 57 32K-WORD IA8000H IPFFFH 58 32K-WORD I8000H IPFFFH 53 32K-WORD I8000H IPFFFH 53 32K-WORD I8000H IPFFFH 53 32K-WORD IS000H IPFFFH 51 32K-WORD IS000H IPFFFH 51 32K-WORD IS000H IPFFFH 47 32K-WORD I3000H IPFFFH 43 32K-WORD IS000H IPFFFH 44 32K-WORD IS000H IPFFFH </td <td></td> <td>69</td> <td></td> <td>1F0000H - 1F7FFFH</td>		69		1F0000H - 1F7FFFH
67 32K-WORD IE0000H IE7FFFH 66 32K-WORD ID8000H IDFFFFH 64 32K-WORD IC0000H IC7FFFH 63 32K-WORD IB0000H IBFFFFH 61 32K-WORD IB0000H IBFFFFH 60 32K-WORD IA0000H IAFFFFH 59 32K-WORD IA8000H IAFFFFH 50 32K-WORD I98000H IS7FFFH 54 32K-WORD I88000H IS7FFFH 53 32K-WORD IS8000H IS7FFFH 50 32K-WORD IS8000H IS7FFFH 50 32K-WORD IS8000H IS7FFFH 40 32K-WORD IS8000H IS7FFFH 41 32K-WORD I38000H IAFFFFH 42 32K-WORD I38000H IAFFFFH 43 32K-WORD I30000H IAFFFFH 43 32K-WORD I30000H IAFFFFH 44 32K-WORD I30000H <		-		1E8000H - 1EFFFFH
66 32K-WORD ID8000H - ID7FFFH 65 32K-WORD ID0000H - ID7FFFH 63 32K-WORD IC8000H - ICFFFFH 61 32K-WORD IB8000H - IB7FFFH 61 32K-WORD IA8000H - IAFFFFH 59 32K-WORD IA8000H - IAFFFFH 57 32K-WORD IA8000H - IAFFFFH 56 32K-WORD I80000H - IAFFFFH 57 32K-WORD I80000H - IAFFFFH 53 32K-WORD I80000H - IAFFFFH 54 32K-WORD I80000H - IAFFFFH 52 32K-WORD I80000H - IFFFFH 53 32K-WORD I58000H - IFFFFH 50 32K-WORD I58000H - IFFFFH 46 32K-WORD I38000H - IFFFFH 45 32K-WORD I38000H - IFFFFH 45 32K-WORD I38000H - IFFFFH 46 32K-WORD I38000H - IFFFFH 47 32K-WORD I38000H - IFFFFH 43 32K-WORD I38000H - IFFFFH 36 32K-WORD <td></td> <td></td> <td></td> <td>1E0000H - 1E7FFFH</td>				1E0000H - 1E7FFFH
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20 32K-WORD 068800H 06FFFH 19 32K-WORD 060000H 067FFFH 18 32K-WORD 058000H 057FFFH 17 32K-WORD 05000H 057FFFH 16 32K-WORD 048000H 047FFFH 16 32K-WORD 040000H 047FFFH 13 32K-WORD 038000H 037FFFH 13 32K-WORD 038000H 037FFFH 12 32K-WORD 028000H 027FFFH 10 32K-WORD 018000H 027FFFH 10 32K-WORD 018000H 017FFFH 9 32K-WORD 018000H 007FFFH 9 32K-WORD 018000H 007FFFH 10 32K-WORD 008000H 007FFFH 9 32K-WORD 008000H 007FFFH 10 32K-WORD 0008000H 007FFFH 14 4K-WORD 007000H 007FFFH 14 4K-WORD 005000H 005	1 K	23	32K-WORD	080000H - 087FFFH
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11 32K WORD 018000H 01FFFFH 9 32K-WORD 018000H 01FFFFH 9 32K-WORD 010000H 017FFFH 8 32K-WORD 008000H 00FFFFH 7 4K-WORD 007000H 007FFFH 6 4K-WORD 006000H 005FFFH 5 4K-WORD 005000H 005FFFH 4 4K-WORD 004000H 004FFFH 3 4K-WORD 003000H 003FFFH 2 4K-WORD 002000H 002FFFH 1 4K-WORD 001000H 001FFFH	2			060000H - 067FFFH
11 32K WORD 018000H 01FFFFH 9 32K-WORD 018000H 01FFFFH 9 32K-WORD 010000H 017FFFH 8 32K-WORD 008000H 00FFFFH 7 4K-WORD 007000H 007FFFH 6 4K-WORD 006000H 005FFFH 5 4K-WORD 005000H 005FFFH 4 4K-WORD 004000H 004FFFH 3 4K-WORD 003000H 003FFFH 2 4K-WORD 002000H 002FFFH 1 4K-WORD 001000H 001FFFH		-		058000H - 05FFFFH
11 32K WORD 018000H 01FFFFH 9 32K-WORD 018000H 01FFFFH 9 32K-WORD 010000H 017FFFH 8 32K-WORD 008000H 00FFFFH 7 4K-WORD 007000H 007FFFH 6 4K-WORD 006000H 005FFFH 5 4K-WORD 005000H 005FFFH 4 4K-WORD 004000H 004FFFH 3 4K-WORD 003000H 003FFFH 2 4K-WORD 002000H 002FFFH 1 4K-WORD 001000H 001FFFH	\mathbf{P}			
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2 4K-WORD 002000H - 002FFFH 1 4K-WORD 001000H - 001FFFH		3		003000H - 003FFFH
1 4K-WORD 001000H - 001FFFH	1			
	•	•		

Figure 2. Memory Map (Bottom Parameter)

Table 3.	Identifier	Codes and	OTP A	Address	for Read	Operation
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		1		
	Code	Address $[A_{15}-A_0]^{(1)}$	Data [DQ ₁₅ -DQ ₀]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	
Device Code	Bottom Parameter Device Code	0001H	00B1H	2
Block Lock Configuration	Block is Unlocked		$DQ_0 = 0$	3
Code	Block is Locked	Block	$DQ_0 = 1$	3
	Block is not Locked-Down	Address + 2	$DQ_1 = 0$	3
	Block is Locked-Down		$DQ_1 = 1$	3
Device Configuration Code	Partition Configuration Register	0006Н	PCRC	4
OTP	OTP Lock	0080H	OTP-LK	5
	OTP	0081-0088H	OTP	6

1. The address A₂₁-A₁₆ are shown in below table for reading the manufacturer, device, lock configuration,

device configuration code and OTP data.

2. Bottom parameter device has its parameter blocks in the plane0 (The lowest address).

3. DQ₁₅-DQ₂ are reserved for future implementation.
 4. PCRC=Partition Configuration Register Code.

5. OTP-LK=OTP Block Lock configuration.

6. OTP=OTP Block data.

Partition C	Configuration 1	Register ⁽²⁾	Address (64M-bit device)
PCR.10	PCR.9	PCR.8	[A ₂₁ -A ₁₆]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

Table 4. Identifier Codes and OTP Address for Read Operation on Partition Configuration⁽¹⁾ (64M-bit device)

NOTES:

1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).

2. Refer to Table 12 for the partition configuration register.

000088H	
	Customer Programmable Area
000085H	
000084H	
	Factory Programmed Area
000081H	
000080H	Reserved for Future Implementation (DO15-DO2)

Figure 3. OTP Block Address Map for OTP Program (The area outside 80H~88H cannot be used.)

Mode	Notes	RST#	CE#	OE#	WE#	Address	V _{PP}	DQ ₀₋₁₅			
Read Array	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	Х	Х	D _{OUT}			
Output Disable		V _{IH}	V _{IL}	V _{IH}	V _{IH}	Х	Х	High Z			
Standby		V _{IH}	V _{IH}	Х	Х	Х	Х	High Z			
Reset	3	V _{IL}	Х	Х	Х	Х	Х	High Z			
Read Identifier Codes/OTP	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	See Table 3 and Table 4	Х	See Table 3 and Table 4			
Read Query	6,7	V _{IH}	V _{IL}	V _{IL}	V _{IH}	See Appendix	Х	See Appendix			
Write	4,5,6	V _{IH}	V _{IL}	V _{IH}	V _{IL}	Х	Х	D _{IN}			

Table 5. Bus $Operation^{(1,2)}$

Refer to DC Characteristics. When V_{PP}≤V_{PPLK}, memory contents can be read, but cannot be altered.
 X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH1/2} for V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH1/2} voltages.
 RST# at GND±0.2V ensures the lowest power consumption.

4. Command writes involving block erase, (page buffer) program or OTP program are reliably executed when V_{PP}=V_{PPH1/2} and V_{CC}=2.7V-3.6V.
 Command writes involving full chip erase are reliably executed when V_{PP}=V_{PPH1} and V_{CC}=2.7V-3.6V.
 Refer to Table 6 for valid D_{IN} during a write operation.

6. Never hold OE# low and WE# low at the same timing.

7. Refer to Appendix of LH28F640BF series for more information about query code.

	Т	able 6. C	Command	Definitions ⁽¹	1)			
	Bus		1	First Bus Cyc	ele	Se	econd Bus C	ycle
Command	Cycles Req'd	Notes	Oper ⁽¹⁾	Addr ⁽²⁾	Data	Oper ⁽¹⁾	Addr ⁽²⁾	Data ⁽³⁾
Read Array	1		Write	PA	FFH			
Read Identifier Codes/OTP	≥2	4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5,9	Write	Х	30H	Write	Х	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥4	5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8,9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
OTP Program	2	9	Write	OA	С0Н	Write	OA	OD
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

1. Bus operations are defined in Table 5.

2. The address which is written at the first bus cycle should be the same as the address which is written at the second bus cvcle.

X=Any valid address within the device.

PA=Address within the selected partition.

IA=Identifier codes address (See Table 3 and Table 4).

QA=Query codes address. Refer to Appendix of LH28F640BF series for details.

BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.

WA=Address of memory location for the Program command or the first address for the Page Buffer Program command. OA=Address of OTP block to be read or programmed (See Figure 3).

PCRC=Partition configuration register code presented on the address A₀-A₁₅.

3. ID=Data read from identifier codes. (See Table 3 and Table 4).

QD=Data read from query database. Refer to Appendix of LH28F640BF series for details.

SRD=Data read from status register. See Table 10 and Table 11 for a description of the status register bits.

WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.

OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.

N-1=N is the number of the words to be loaded into a page buffer.

4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 3 and Table 4). The Read Query command is available for reading CFI (Common Flash Interface) information.

5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH}.

6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.

7. Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target partition to be programmed and the confirm command (D0H). Refer to Appendix of LH28F640BF series for details.

- 8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
- 9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
- 10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is V_{IL}. When WP# is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
 11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be
- used.

		Cu	rrent State		(2)	
State	WP#	DQ1 ⁽¹⁾	DQ ₀ ⁽¹⁾	State Name	Erase/Program Allowed ⁽²⁾	
[000]	0	0	0	Unlocked	Yes	
[001] ⁽³⁾	0	0	1	Locked	No	
[011]	0	1	1	Locked-down	No	
[100]	1	0	0	Unlocked	Yes	
[101] ⁽³⁾	1	0	1	Locked	No	
[110] ⁽⁴⁾	1	1	0	Lock-down Disable	Yes	
[111]	1	1	1	Lock-down Disable	No	

Table 7. Functions of Block Lock⁽⁵⁾ and Block Lock-Down

1. $DQ_0=1$: a block is locked; $DQ_0=0$: a block is unlocked.

 $DQ_1=1$: a block is locked-down; $DQ_1=0$: a block is not locked-down.

2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.

3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is,

[001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation. 4. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

5. OTP (One Time Program) block has the lock function which is different from those described above.

	Curren	t State		Result after L	ock Command Writte	n (Next State)
State	WP#	DQ ₁	DQ ₀	Set Lock ⁽¹⁾	Clear Lock ⁽¹⁾	Set Lock-down ⁽¹⁾
[000]	0	0	0	[001]	No Change	[011] ⁽²⁾
[001]	0	0	1	No Change ⁽³⁾	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] ⁽²⁾
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] ⁽²⁾
[111]	1	1	1	No Change	[110]	No Change

Table 8. Block Locking State Transitions upon Command Write⁽⁴⁾

NOTES:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.

2. When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0=0$), the corresponding block is locked-down and automatically locked at the same time.

3. "No Change" means that the state remains unchanged after the command written.

4. In this state transitions table, assumes that WP# is not changed and fixed V_{IL} or V_{IH} .

Due is a Chata		Current S	State		Result after WP# Transition (Next State)			
Previous State	State	WP#	DQ ₁	DQ ₀	WP#= $0 \rightarrow 1^{(1)}$	WP#= $1 \rightarrow 0^{(1)}$		
-	[000]	0	0	0	[100]	-		
-	[001]	0	0	1	[101]	-		
[110] ⁽²⁾	[011]	0	1	1	[110]	-		
Other than $[110]^{(2)}$	[011]	0			[111]	-		
-	[100]	1	0	0	-	[000]		
-	[101]	1	0	1	-	[001]		
-	[110]	1	1	0	-	[011] ⁽³⁾		
-	[111]	1	1	1	-	[011]		

Table 9. Block Locking State Transitions upon WP# Transition⁽⁴⁾

1. "WP#=0 \rightarrow 1" means that WP# is driven to V_{IH} and "WP#=1 \rightarrow 0" means that WP# is driven to V_{IL}.

2. State transition from the current state [011] to the next state depends on the previous state.

3. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

R	R	R	R	R	R	R	R	
15	14	13	12	11	10	9	8	
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R	
7	6	5	4	3	2	1	0	
ENHANCE	= RESERVED F MENTS (R) E STATE MACH		(WSMS)	Status Register	NOT		tion not WS	
1 = Ready 0 = Busy SR.6 = BLOC	K ERASE SUS	PEND STATUS	S (BESS)	(Write State Ma be occupied by 3 or 4 partitions	achine). Even if the other partit	the SR.7 is "1", ion when the de	the WSM ma	
1 = Block	Erase Suspende Erase in Progres	d		Check SR.7 to buffer) program invalid while S	n or OTP progra			
 SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES) 1 = Error in Block Erase or Full Chip Erase 0 = Successful Block Erase or Full Chip Erase 				If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit, set partition configuration register attempt, an improper command sequence was entered.				
OTP $1 = Error is$ $0 = Succes$	BUFFER) PRO PROGRAM ST n (Page Buffer) sful (Page Buffe	ATUS (PBPOP Program or OT	P Program	SR.3 does not provide a continuous indication of V_{PP} level The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OT Program command sequences. SR.3 is not guaranteed				
	TATUS (VPPS) DW Detect, Ope K	eration Abort		SR.1 does not p bit. The WSM i	provide a continue of the arron of the provide a continue of the provi	nuous indication block lock bit o	n of block loo nly after Bloo	
STAT $1 = (Page I)$	BUFFER) PRO US (PBPSS) Buffer) Program Buffer) Program	n Suspended		Erase, Full Cl Program comm depending on th set. Reading the the Read Iden lock bit status.	mand sequence he attempted op block lock co	es. It informs beration, if the b nfiguration cod	s the syster block lock bit es after writir	
1 = Erase of	CE PROTECT S or Program Atte d Block, Operat ced	mpted on a		SR.15 - SR.8 and SR.0 are reserved for future use and shou be masked out when polling the status register.				

		Table 1	1. Extended Sta	atus Register De	efinition		
R	R	R	R	R	R	R	R
15	14	13	12	11	9	8	
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R) XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available			NOTES: After issue a Page Buffer Program command (E8H) XSR.7="1" indicates that the entered command is accepted If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not. XSR.15-8 and XSR.6-0 are reserved for future use and				
XSR.6-0 = RES	SERVED FOR FU	JTURE ENHAN	CEMENTS (R)	should be ma register.	sked out when	polling the e	extended status

		Table 12. I	Partition Config	guration Regis	ter Definition		
R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
PCR.15-11 = RPCR.10-8 = PA000 = No001 = Plan(defau010 = Plan(defau011 = Planthreeoperat101 = Planthreeoperat101 = Planthreeoperat000<	RESERVED FOR ENHANCEME ARTITION COM partitioning. Du ne1-3 are merge It in a bottom param ne 0-1 and Plane on respectively. ne 0-2 are merge partitions in the ion is available ne 0-1 are merge partitions in the ion is available ne 1-2 are merge partitions in the ion is available ne 1-2 are merge partitions in the ion is available ne 1-2 are merge partitions in the ion is available PARTITION PARTITION PARTITION	R FUTURE ENTS (R) IFIGURATION al Work is not a d into one partin arameter device e2-3 are merged ed into one part is configuratic between any tw ed into one part is configuratic is configura	(PC2-0) allowed. tion. i into one ition. There are on. Dual work o partitions. ition. There are on. Dual work o partitions. ition. There are on. Dual work o partitions. Ition. There are on. Dual work o partitions. IL WORK	111 = Th Each tivel two PCR.7-0 = R After power- "001" in a parameter de See Figure 4 PCR.15-11 a should be configuration PC2 PC1PC0 0 1 1 1 1 0 1 0 1 1 1 1 1	PARTITION2 PARTITION3 PARTITIA PARTITION3 PARTITIA PARTITION3 PARTITIA PARTITION3 PARTITIA PARTITIA PARTITION3 PARTITIA P	tions in this comods to each peration is available FUTURE JTS (R) TES: Set, PCR10-8 (If partition config partition config partition config NING FOR DU N2 PARTITION EAU N2 PARTITION EAU N12 PARTITION EAU PARTITION1 PAR EAU PARTITION1 PAR	AL WORK 1 PARTITIONO AL WORK 1 PARTITIONO PARTITIONO PARTITIONO PARTITIONO PARTITIONO PARTITIONO
		F	igure 4. Partiti	on Configurat	1011		
							Pov 242

Rev. 2.42

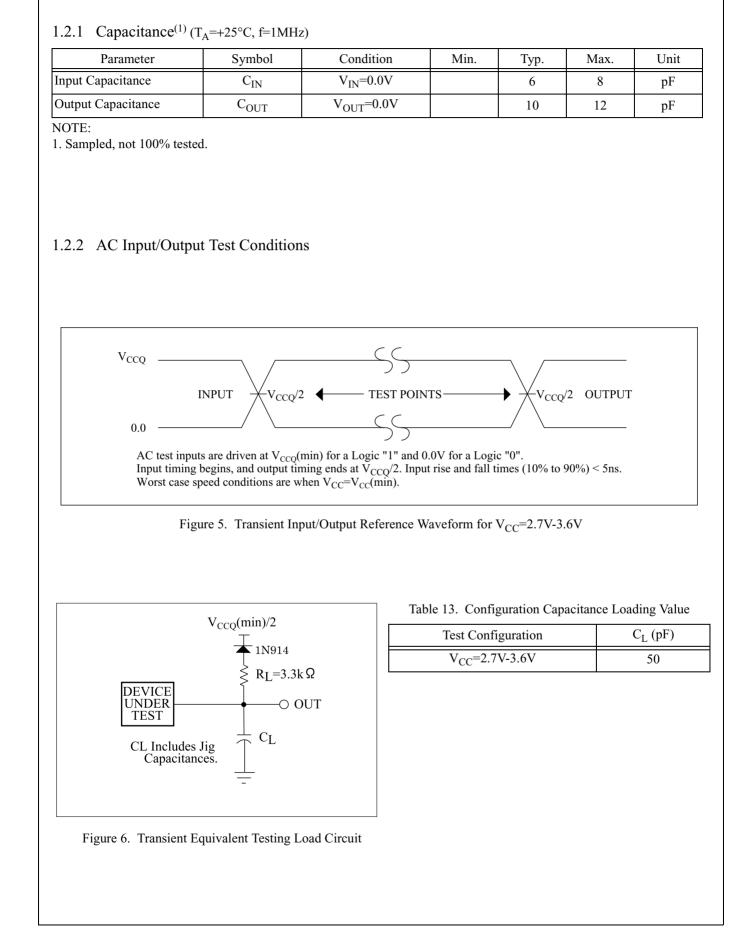
 Electrical Specifications Absolute Maximum Ratings* Operating Temperature During Read, Erase and Program40°C to +85°C ⁽¹⁾ 	*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.
	NOTES:
Storage Temperature During under Bias40°C to +85°C During non Bias65°C to +125°C	 Operating temperature is for extended temperature product defined by this specification. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions,
Voltage On Any Pin (except V_{CC} and V_{PP})0.5V to V_{CC} +0.5V $^{(2)}$	this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC} +0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20ns.
V_{CC} and V_{CCQ} Supply Voltage0.2V to +3.9V $^{(2)}$	 Maximum DC voltage on V_{PP} may overshoot to +13.0V for periods <20ns. V_{PP} erase/program voltage is normally 2.7V-3.6V. Applying 11.7V-12.3V to V_{PP} during erase/program
V_{PP} Supply Voltage0.2V to +12.6V ^(2, 3, 4)	can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. V_{PP} may be connected to 11.7V-12.3V for a total of 80
Output Short Circuit Current 100mA ⁽⁵⁾	hours maximum.5. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Operating Temperature	T _A	-40	+25	+85	°C	
V _{CC} Supply Voltage	V _{CC}	2.7	3.0	3.6	V	1
I/O Supply Voltage	V _{CCQ}	2.7	3.0	3.6	V	1
V _{PP} Voltage when Used as a Logic Control	V _{PPH1}	1.65	3.0	3.6	V	1
V _{PP} Supply Voltage	V _{PPH2}	11.7	12	12.3	V	1, 2
Main Block Erase Cycling: V _{PP} =3.0V		100,000			Cycles	
Parameter Block Erase Cycling: V _{PP} =3.0V		100,000			Cycles	
Main Block Erase Cycling: V _{PP} =12V, 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: V _{PP} =12V, 80 hrs.				1,000	Cycles	
Maximum V _{PP} hours at 12V				80	Hours	

NOTES:

See DC Characteristics tables for voltage range-specific specification.
 Applying V_{PP}=11.7V-12.3V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to V_{PP}=11.7V-12.3V is not allowed and can cause damage to the device.



1.2.3 DC Characteristics

V_{CC}=2.7V-3.6V

Symbol	Paran	neter	Notes	Min.	Тур.	Max.	Unit	Test Conditions
I _{LI}	Input Load Current		1	-1.0		+1.0	μΑ	V _{CC} =V _{CC} Max.,
I _{LO}	Output Leakage Cur	rent	1	-1.0		+1.0	μΑ	V _{CCQ} =V _{CCQ} Max., V _{IN} /V _{OUT} =V _{CCQ} or GND
I _{CCS}	V _{CC} Standby Curren	t	1		4	20	μΑ	$V_{CC}=V_{CC}Max.,$ $CE\#=RST\#=$ $V_{CCQ}\pm0.2V,$ $WP\#=V_{CCQ} \text{ or } GND$
I _{CCAS}	V _{CC} Automatic Pow	1,4		4	20	μΑ	V _{CC} =V _{CC} Max., CE#=GND±0.2V, WP#=V _{CCQ} or GND	
I _{CCD}	V _{CC} Reset Power-D	1		4	20	μΑ	RST#=GND±0.2V	
I	Average V _{CC} Read Current Normal Mode		1,7		15	25	mA	V _{CC} =V _{CC} Max., CE#=V _{IL} ,
I _{CCR}	Average V _{CC} Read Current Page Mode	8 Word Read	1,7		5	10	mA	OE#=V _{IH} , f=5MHz
т	V (De ce Duffer) D	no anome Cumuont	1,5,7		20	60	mA	V _{PP} =V _{PPH1}
I _{CCW}	V _{CC} (Page Buffer) P	Togram Current	1,5,7		10	20	mA	V _{PP} =V _{PPH2}
т	V _{CC} Block Erase, Fu	ıll Chip	1,5,7		10	30	mA	V _{PP} =V _{PPH1}
I _{CCE}	Erase Current		1,5,7		10	30	mA	V _{PP} =V _{PPH2}
I _{CCWS} I _{CCES}	V _{CC} (Page Buffer) P Block Erase Suspend	-	1,2,7		10	200	μA	CE#=V _{IH}
I _{PPS} I _{PPR}	V _{PP} Standby or Read	d Current	1,6,7		2	5	μΑ	V _{PP} ≤V _{CC}
I	V _{PP} (Page Buffer) P	rogram Current	1,5,6,7		2	5	μA	V _{PP} =V _{PPH1}
I _{PPW}	· pp (1 age Duilet) I		1,5,6,7		10	30	mA	V _{PP} =V _{PPH2}
I	V _{PP} Block Erase, Fu	ıll Chip	1,5,6,7		2	5	μΑ	V _{PP} =V _{PPH1}
I _{PPE}	Erase Current		1,5,6,7		5	15	mA	V _{PP} =V _{PPH2}
Innura	V _{PP} (Page Buffer) P	rogram	1,6,7		2	5	μA	V _{PP} =V _{PPH1}
I _{PPWS}	Suspend Current		1,6,7		10	200	μA	V _{PP} =V _{PPH2}
Innec	V _{PP} Block Erase Sus	spend Current	1,6,7		2	5	μA	V _{PP} =V _{PPH1}
I _{PPES}	v pp block Elase Su	spena Current	1,6,7		10	200	μA	V _{PP} =V _{PPH2}

		V _{CC} =2	2.7V-3.6V	7			
Symbol	Parameter	Notes	Min.	Тур.	Max.	Unit	Test Conditions
V _{IL}	Input Low Voltage	5	-0.4		0.4	V	
V _{IH}	Input High Voltage	5	2.4		V _{CCQ} + 0.4	V	
V _{OL}	Output Low Voltage	5			0.2	V	$\begin{array}{l} V_{CC} = V_{CC} Min., \\ V_{CCQ} = V_{CCQ} Min., \\ I_{OL} = 100 \mu A \end{array}$
V _{OH}	Output High Voltage	5	V _{CCQ} -0.2			V	V _{CC} =V _{CC} Min., V _{CCQ} =V _{CCQ} Min., I _{OH} =-100µA
V _{PPLK}	V _{PP} Lockout during Normal Operations	3,5,6			0.4	V	
V _{PPH1}	V _{PP} during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations	6	1.65	3.0	3.6	V	
V _{PPH2}	V _{PP} during Block Erase, (Page Buffer) Program or OTP Program Operations	6	11.7	12	12.3	V	
V _{LKO}	V _{CC} Lockout Voltage		1.5			V	

DC Characteristics (Continued)

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC}=3.0V and T_A=+25°C unless V_{CC} is specified.

2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR} . 3. Block erase, full chip erase, (page buffer) program and OTP program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed

in the range between V_{PPLK}(max.) and V_{PPH1}(min.), between V_{PPH1}(max.) and V_{PPH2}(min.) and above V_{PPH2}(max.).

4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVOV}) provide new data when addresses are changed.

5. Sampled, not 100% tested.

6. V_{PP} is not used for power supply pin. With V_{PP}≤V_{PPLK}, block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.

Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{CC} power bus.

Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to $12V\pm0.3V$ for a total of 80 hours maximum.

7. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.

1.2.4 AC Characteristics - Read-Only Operations⁽¹⁾

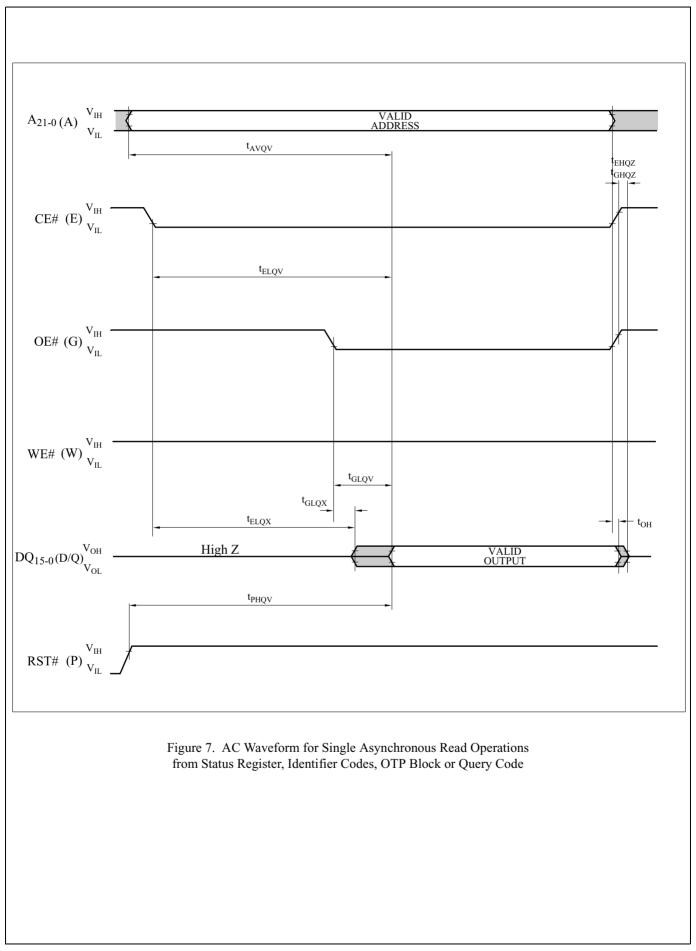
$V_{CC}=2.7V-3.6V$	$T_A = -40^{\circ}C$ to $+85^{\circ}C$
CC 2.7 = 5.0	$I_{A} = 0 C 10 + 05 C$

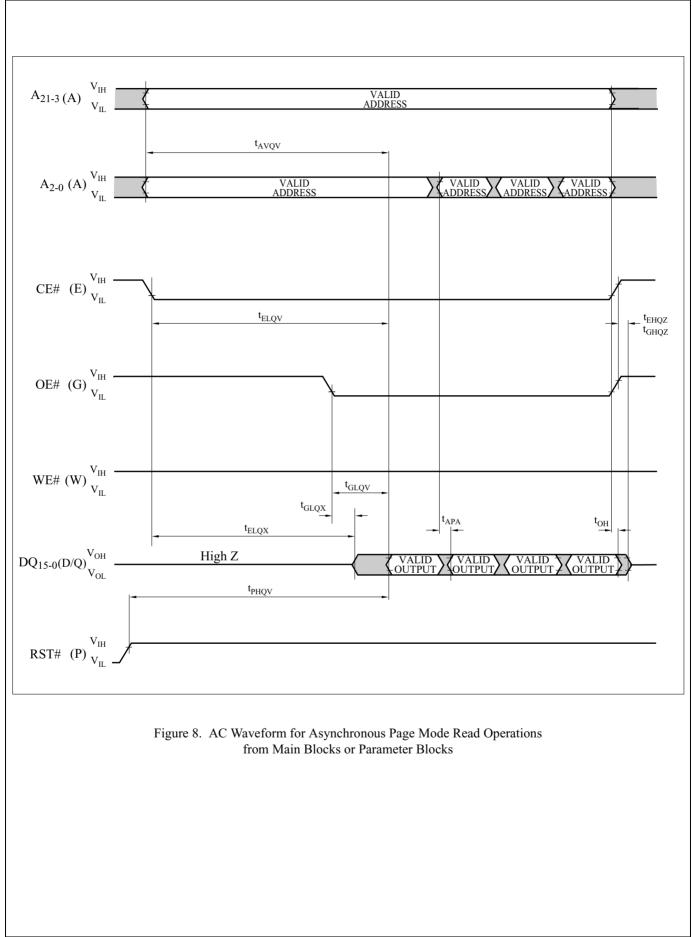
Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Read Cycle Time		80		ns
t _{AVQV}	Address to Output Delay			80	ns
t _{ELQV}	CE# to Output Delay	3		80	ns
t _{APA}	Page Address Access Time			35	ns
t _{GLQV}	OE# to Output Delay	3		20	ns
t _{PHQV}	RST# High to Output Delay			150	ns
t _{EHQZ} , t _{GHQZ}	CE# or OE# to Output in High Z, Whichever Occurs First	2		20	ns
t _{ELQX}	CE# to Output in Low Z	2	0		ns
t _{GLQX}	OE# to Output in Low Z	2	0		ns
t _{OH}	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns

NOTES:

1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.

2. Sampled, not 100% tested. 3. OE# may be delayed up to t_{ELQV} — t_{GLQV} after the falling edge of CE# without impact to t_{ELQV} .





1.2.5 AC Characteristics - Write Operations^{(1), (2)}

$V_{CC}=2.7V-3.6V, T_{A}=-40^{\circ}C \text{ to }+85^{\circ}C$	V_{CC}	~=2.7V-3	.6V, T	$=-40^{\circ}$ C to	o +85°C
--	----------	----------	--------	---------------------	---------

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Write Cycle Time		80		ns
t _{PHWL} (t _{PHEL})	RST# High Recovery to WE# (CE#) Going Low	3	150		ns
$t_{\rm ELWL} \left(t_{\rm WLEL} \right)$	CE# (WE#) Setup to WE# (CE#) Going Low	4	0		ns
t _{WLWH} (t _{ELEH})	WE# (CE#) Pulse Width	4	50		ns
t _{DVWH} (t _{DVEH})	Data Setup to WE# (CE#) Going High	8	40		ns
$t_{AVWH} (t_{AVEH})$	Address Setup to WE# (CE#) Going High	8	50		ns
t _{WHEH} (t _{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		ns
t _{WHDX} (t _{EHDX})	DX) Data Hold from WE# (CE#) High		0		ns
$t_{WHAX} (t_{EHAX})$	X (t _{EHAX}) Address Hold from WE# (CE#) High		0		ns
t _{WHWL} (t _{EHEL})	HEL) WE# (CE#) Pulse Width High 5 30			ns	
$t_{\rm SHWH} \left(t_{\rm SHEH} ight)$	WP# High Setup to WE# (CE#) Going High	3	0		ns
t _{VVWH} (t _{VVEH})	V _{PP} Setup to WE# (CE#) Going High	3	200		ns
t _{WHGL} (t _{EHGL})	Write Recovery before Read		30		ns
t _{QVSL}	WP# High Hold from Valid SRD	3, 6	0		ns
t _{QVVL}	V _{PP} Hold from Valid SRD	3, 6	0		ns
$t_{WHR0} (t_{EHR0})$	WE# (CE#) High to SR.7 Going "0"	3, 7		t_{AVQV}^+ 50	ns

NOTES:

1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.

2. A write operation can be initiated and terminated with either CE# or WE#.

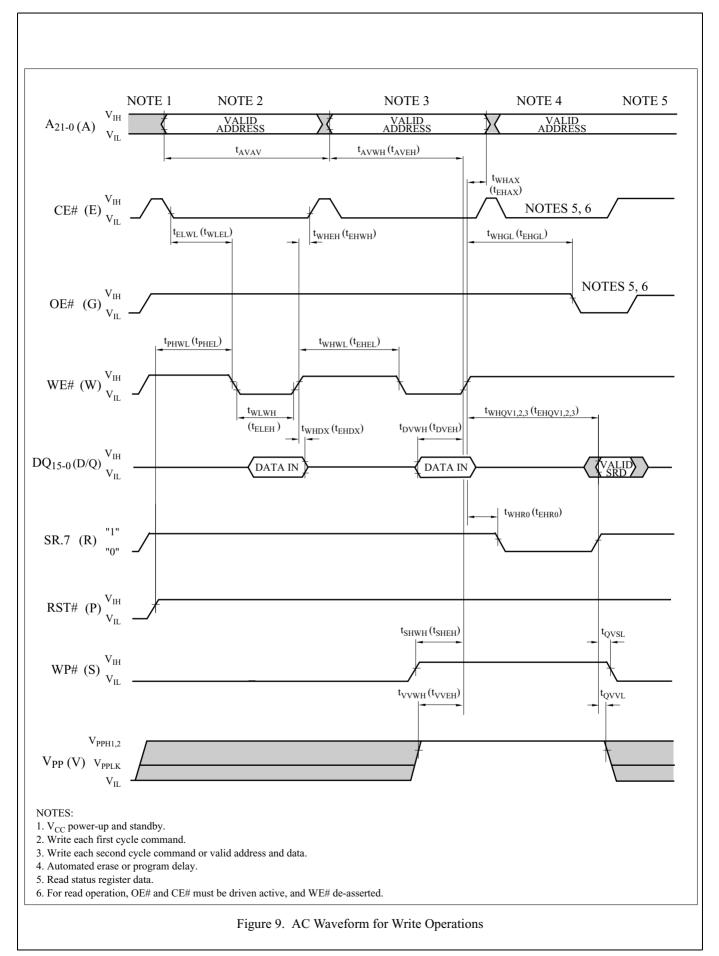
3. Sampled, not 100% tested.

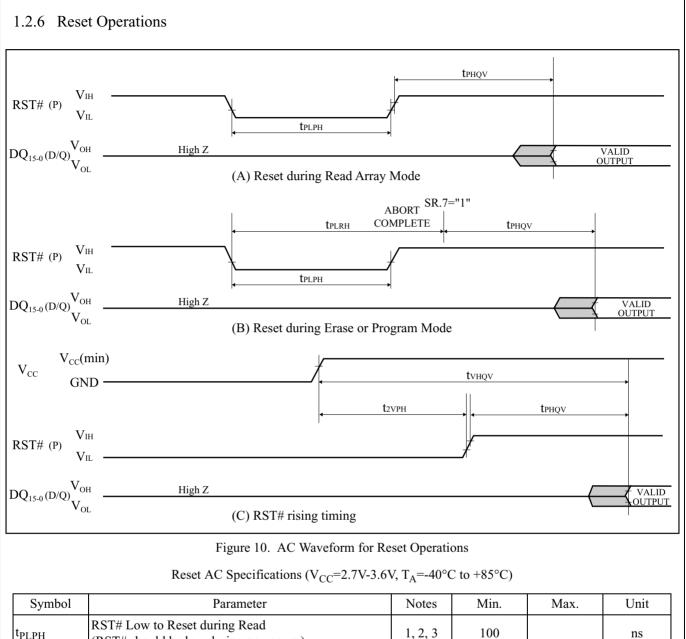
4. Write pulse width (t_{WP}) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of

CE# or WE# (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$. 5. Write pulse width high (t_{WPH}) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling

6. V_{PP} should be held at V_{PP}=V_{PPH1/2} until determination of block erase, (page buffer) program or OTP program success (SR.1/3/4/5=0) and held at V_{PP}=V_{PPH1} until determination of full chip erase success (SR.1/3/5=0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command=t_{AVQV}+100ns.

8. Refer to Table 6 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.





Symbol	Parameter		Min.	Max.	Unit
t _{PLPH}	RST# Low to Reset during Read (RST# should be low during power-up.)		100		ns
t _{PLRH}	RST# Low to Reset during Erase or Program	1, 3, 4		22	μs
t _{2VPH}	VPH V _{CC} 2.7V to RST# High		100		ns
t _{VHQV}	_{QV} V _{CC} 2.7V to Output Delay			1	ms
NOTES					

1. A reset time, t_{PHQV}, is required from the later of SR.7 going "1" or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.

2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.

3. Sampled, not 100% tested.

4. If RST# asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.

5. When the device power-up, holding RST# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

	·	<u> </u>	-5.0 v, 1 _A 40			,				
Symbol	Parameter	Notes	Page Buffer Command is Used or not	V _{PP} =V _{PPH1} (In System)			V _{PP} =V _{PPH2} (In Manufacturing)			Unit
			Used	Min.	Тур. ⁽¹⁾	Max. ⁽²⁾	Min.	Тур. ⁽¹⁾	Max. ⁽²⁾	
t _{WPB}	4K-Word Parameter Block	2	Not Used		0.05	0.3		0.04	0.12	S
WPB	Program Time	2	Used		0.03	0.12		0.02	0.06	s
t _{WMB}	32K-Word Main Block	2	Not Used		0.38	2.4		0.31	1.0	s
ч	Program Time	2	Used		0.24	1.0		0.17	0.5	S
t _{WHQV1} /	Word Program Time	2	Not Used		11	200		9	185	μs
t _{EHQV1}	word Program Time	2	Used		7	100		5	90	μs
t _{WHOV1} / t _{EHOV1}	OTP Program Time	2	Not Used		36	400		27	185	μs
t _{WHQV2} / t _{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4		0.2	4	s
t _{WHQV3} / t _{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5		0.5	5	s
	Full Chip Erase Time	2	ĺ		80	700				s
t _{WHRH1} / t _{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10		5	10	μs
t _{WHRH2} / t _{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20		5	20	μs
t _{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			μs

 $V_{CC}=2.7V-3.6V$, $T_{A}=-40^{\circ}C$ to $+85^{\circ}C$

NOTES:

1. Typical values measured at V_{CC} =3.0V, V_{PP} =3.0V or 12V, and T_A =+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.

2. Excludes external system-level overhead.

3. Sampled, but not 100% tested.

4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1".

5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

2 Related Document Information⁽¹⁾

Document No.	Document Name
FUM00701	LH28F640BF series Appendix

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

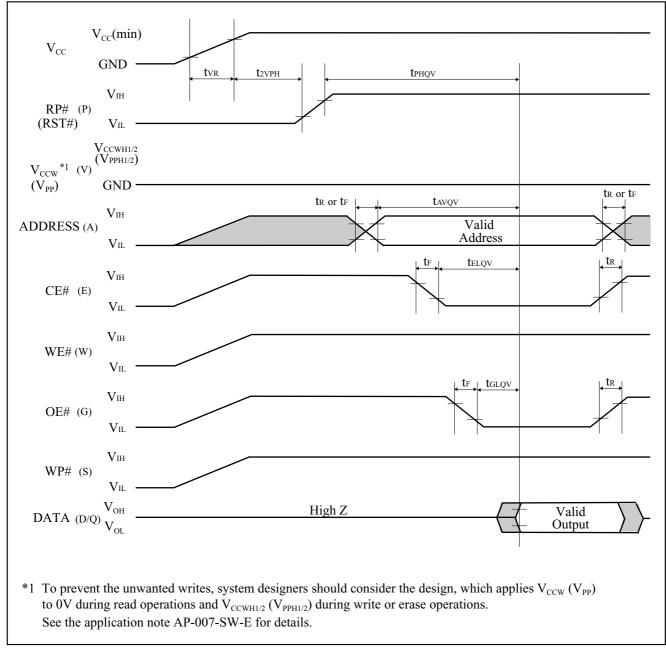


Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR} , t_R , t_F in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{VR}	V _{CC} Rise Time		0.5	30000	μs/V
t _R	Input Signal Rise Time			1	μs/V
t _F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:

1. Sampled, not 100% tested.

2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

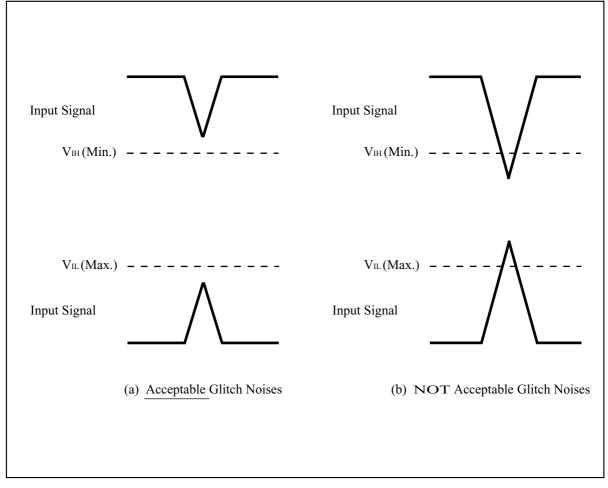


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION⁽¹⁾

Document No.	Document Name	
AP-001-SD-E	Flash Memory Family Software Drivers	
AP-006-PT-E	Data Protection Method of SHARP Flash Memory	
AP-007-SW-E	RP#, V _{PP} Electric Potential Switching Circuit	

NOTE:

1. International customers should contact their local SHARP or distribution sales office.