
HD74CBT3244

Octal FET Bus Switch

HITACHI

ADE-205-643 (Z)

Preliminary
Rev. 0
August 2001

Description

The HD74CBT3244 provides eight bits of high speed TTL-compatible bus switching in a standard '244 device pinout. The low on state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as two 4-bit low impedance switches with separate output enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open, and the high impedance state exists between the two ports.

Features

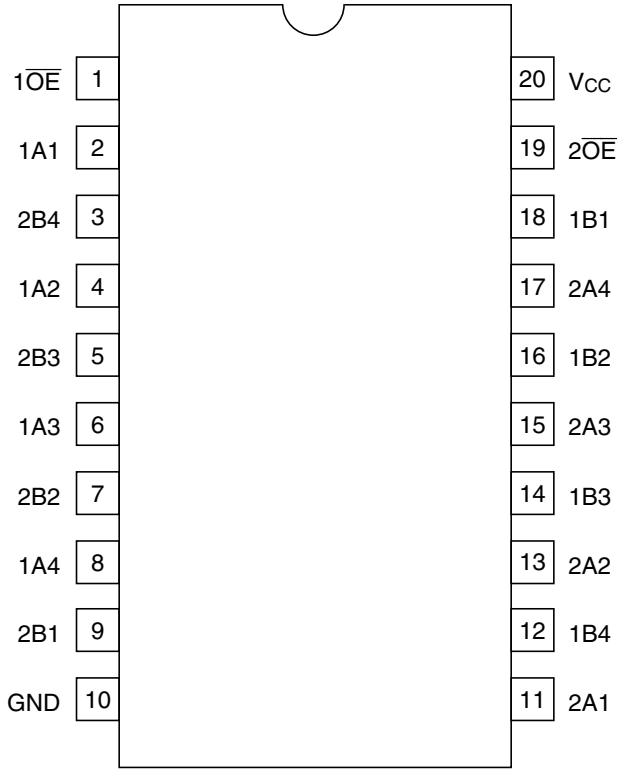
- Standard '244 type pinout.
 - Minimal propagation delay through the switch.
 - 5 Ω switch connection between two ports.
 - TTL-compatible input levels.
 - Ultra low quiescent power.
- Ideally suited for notebook applications.

Function Table

| Input \overline{OE} | Function |
|-----------------------|-----------------|
| L | A port = B port |
| H | Disconnect |

H: High level
L: Low level

Pin Arrangement



(Top view)

Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|-----------------------|-------------|------------------|-----------------------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V | |
| Input voltage range ¹ | V_I | -0.5 to 7.0 | V | |
| Input clamp current | I_{IK} | -50 | mA | $V_I < 0$ |
| Continuous output current | I_O | 128 | mA | $V_O = 0$ to V_{CC} |
| Continuous current through V_{CC} or GND | I_{CC} or I_{GND} | ± 100 | mA | |
| Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ² | P_T | 757 | mW | TSSOP |
| Storage temperature | T_{stg} | -65 to 150 | $^\circ\text{C}$ | |

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

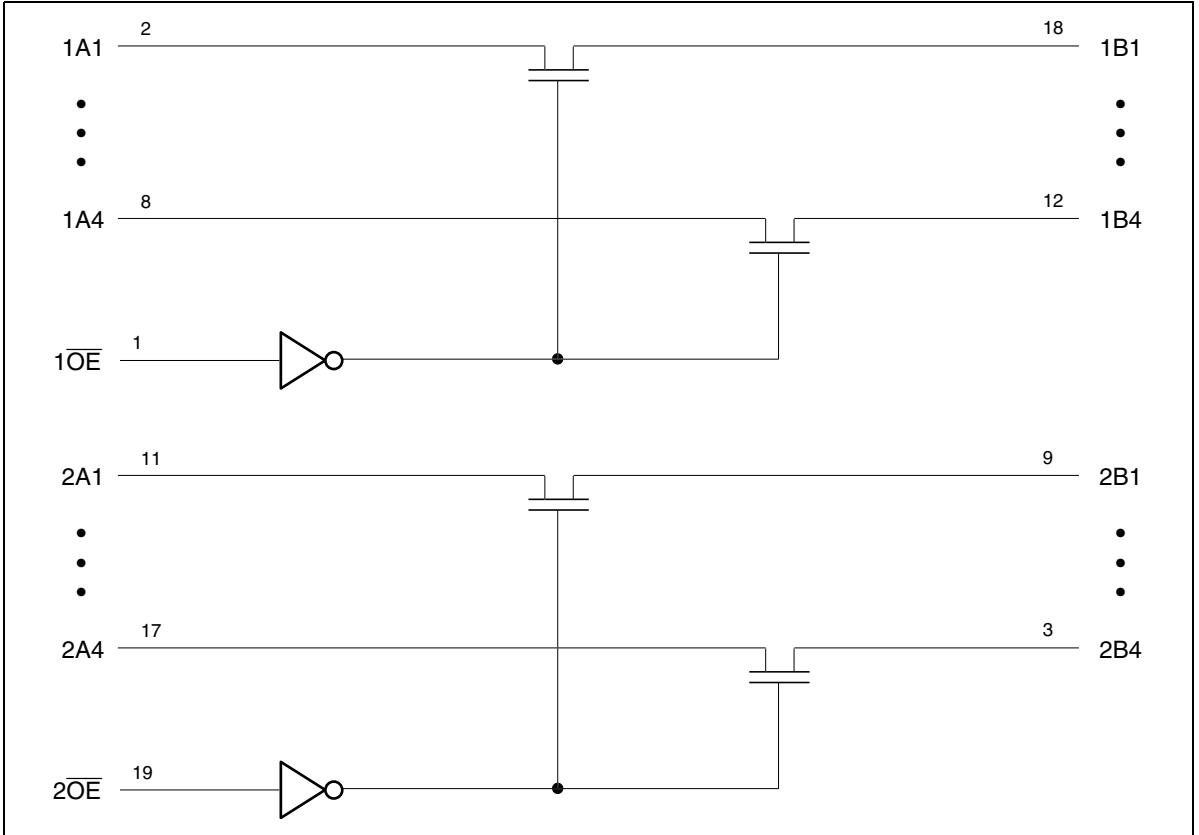
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

| Item | Symbol | Min | Max | Unit | Conditions |
|------------------------------------|-----------------------|-----|-----|------------------|---------------------------|
| Supply voltage range | V_{CC} | 4.5 | 5.5 | V | |
| Input voltage range | V_I | 0 | 5.5 | V | |
| Output voltage range | V_{IO} | 0 | 5.5 | V | |
| Input transition rise or fall rate | $\Delta t / \Delta v$ | 0 | 5 | ns / V | $V_{CC} = 4.5$ to 5.5 V |
| Operating free-air temperature | T_a | -40 | 85 | $^\circ\text{C}$ | |

Note: Unused or floating inputs must be held high or low.

Block Diagram



DC Electrical Characteristics

(Ta = -40 to 85°C)

| Item | Symbol | V _{cc} (V) | Min | Typ ^{*1} | Max | Unit | Test conditions |
|---|------------------|---------------------|-----|-------------------|------|------|--|
| Clamp diode voltage | V _{IK} | 4.5 | — | — | -1.2 | V | I _{IN} = -18 mA |
| Input voltage | V _{IH} | 4.5 to 5.5 | 2.0 | — | — | V | |
| | V _{IL} | 4.5 to 5.5 | — | — | 0.8 | | |
| On-state switch resistance ^{*2} | R _{ON} | 4.5 | — | 5 | 7 | Ω | V _{IN} = 0 V, I _{IN} = 64 mA |
| | | 4.5 | — | 5 | 7 | | V _{IN} = 0 V, I _{IN} = 30 mA |
| | | 4.5 | — | 10 | 15 | | V _{IN} = 2.4 V, I _{IN} = 15 mA |
| Input current | I _{IN} | 0 to 5.5 | — | — | ±1.0 | μA | V _{IN} = 5.5 V or GND |
| Off-state leakage current | I _{OZ} | 5.5 | — | — | ±1.0 | μA | 0 ≤ A, B ≤ V _{cc} |
| Quiescent supply current | I _{CC} | 5.5 | — | — | 3 | μA | V _{IN} = V _{cc} or GND, I _O = 0 mA |
| Increase in I _{CC} per input ^{*3} | ΔI _{CC} | 5.5 | — | — | 2.5 | mA | One input at 3.4 V, other inputs at V _{cc} or GND |

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

1. All typical values are at V_{cc} = 5 V (unless otherwise noted), Ta = 25°C.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.
3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{cc} or GND.

Capacitance

(Ta = 25°C)

| Item | Symbol | V _{cc} (V) | Min | Typ | Max | Unit | Test conditions |
|----------------------------|------------------------|---------------------|-----|-----|-----|------|---|
| Control input capacitance | C _{IN} | 5.0 | — | 3.5 | — | pF | V _{IN} = 0 or 3 V |
| Input / output capacitance | C _{I/O (OFF)} | 5.0 | — | 5 | — | pF | V _O = 0 or 3 V OE = V _{cc} |

Note: This parameter is determined by device characterization is not production tested.

Switching Characteristics

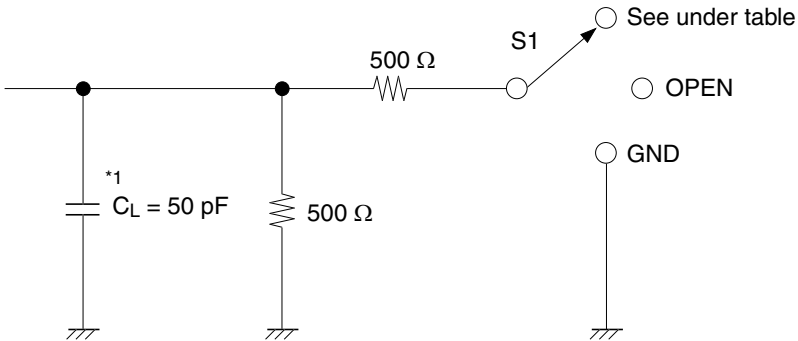
($T_a = -40$ to 85°C)

- $V_{CC} = 5.0 \pm 0.5 \text{ V}$

| Item | Symbol | Min | Max | Unit | Test conditions | FROM (Input) | TO (Output) |
|--------------------------------------|------------------------|-----|------|------|---|------------------------|-------------|
| Propagation delay time ^{*1} | t_{PLH} t_{PHL} | — | 0.25 | ns | $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ | A or B | B or A |
| Enable time | t_{ZH} t_{ZL} | 1.0 | 8.9 | ns | $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ | $\overline{\text{OE}}$ | A or B |
| Disable time | t_{HZ} t_{LZ} | 1.0 | 7.4 | ns | $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ | $\overline{\text{OE}}$ | A or B |

Note: 1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Test Circuit

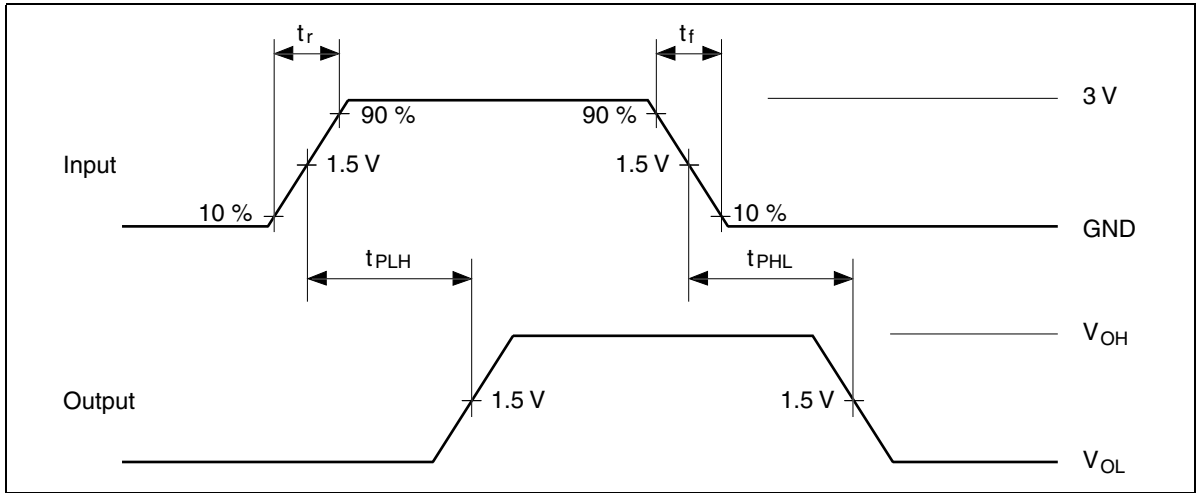


Load circuit for outputs

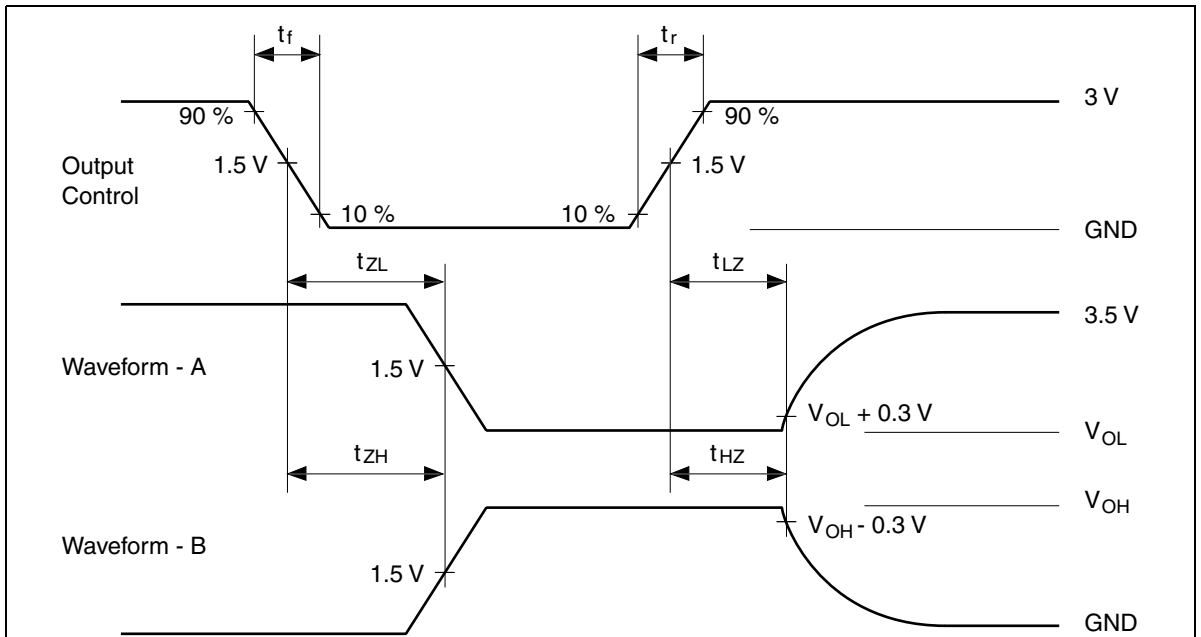
| Symbol | S1 |
|---------------------|------|
| t_{PLH} / t_{PHL} | OPEN |
| t_{ZH} / t_{HZ} | OPEN |
| t_{ZL} / t_{LZ} | 7 V |

Note: 1. C_L includes probe and jig capacitance.

Waveforms - 1



Waveforms - 2

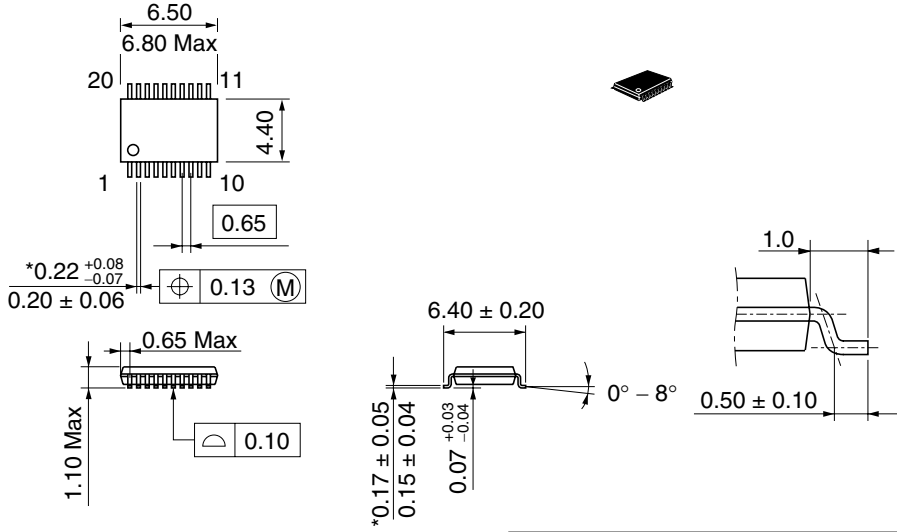


- Notes:
1. All input pulses are supplied by generators having the following characteristics :
 $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of January, 2001

Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | TTP-20DA |
| JEDEC | — |
| EIAJ | — |
| Mass (reference value) | 0.07 g |

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