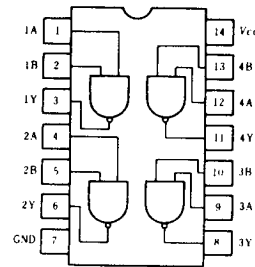


HD74ALS00 ● Quadruple 2-input Positive NAND Gates

■ PIN ARRANGEMENT



(Top View)

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.5\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$	2.5	—	—	V
		$V_{CC}=4.75\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$	2.7	—	—	V
	V_{OL}	$V_{CC}=4.5\text{V}, V_{IH}=2\text{V}, I_{OL}=4\text{mA}$	—	—	0.4	V
		$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, I_{OL}=8\text{mA}$	—	—	0.5	V
Input current	I_{IH}	$V_{CC}=5.5\text{V}, V_I=2.7\text{V}$	—	—	20	μA
	I_I	$V_{CC}=5.5\text{V}, V_I=7\text{V}$	—	—	0.1	mA
	I_{IL}	$V_{CC}=5.5\text{V}, V_I=0.4\text{V}$	—	—	-0.2	mA
Output drive current	I_{OD}	$V_{CC}=5.5\text{V}, V_O=2.125\text{V}$	-10	—	-60	mA
Supply current	I_{CCN}	$V_{CC}=5.5\text{V}, V_I=0\text{V}$	—	0.43	0.85	mA
	I_{CCL}	$V_{CC}=5.5\text{V}, V_I=4.5\text{V}$	—	1.62	3.0	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.5\text{V}, I_I=-18\text{mA}$	—	—	-1.5	V

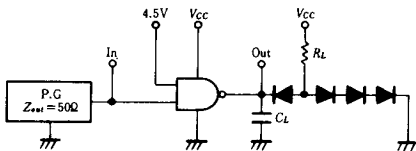
* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

■ SWITCHING CHARACTERISTICS

Item	Symbol	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	$V_{CC}=5\text{V}, T_a=25^\circ\text{C}, R_L=500\Omega, C_L=15\text{pF}$	—	4	—	ns
	t_{PHL}	$V_{CC}=5\text{V}, T_a=25^\circ\text{C}, R_L=500\Omega, C_L=15\text{pF}$	—	5	—	
	t_{PLH}	$V_{CC}=5.0 \pm 0.5\text{V}, T_a=-20 \sim +75^\circ\text{C}, R_L=500\Omega, C_L=50\text{pF}$	3	—	11	
	t_{PHL}	$V_{CC}=5.0 \pm 0.5\text{V}, T_a=-20 \sim +75^\circ\text{C}, R_L=500\Omega, C_L=50\text{pF}$	3	—	11	

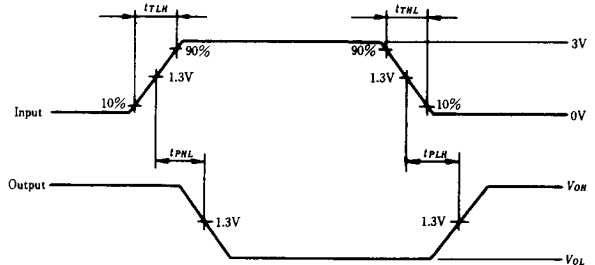
■ TESTING METHOD

Test Circuit



- Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (D).

Waveform



Input pulse: $t_{TLH} \leq 6\text{ns}, t_{THL} \leq 6\text{ns}, \text{PRR} = 1\text{MHz}, \text{duty cycle } 50\%$