HD64530

LAPD Controller

Description

The HD64530 one-chip CMOS communications device supports the LAPD protocol and conforms to the ISDN (integrated services digital network) standard. LAPD is layer 2 of the international ISDN standard specified by CCITT recommendations I.440 and I.441. The HD64530 has a wide range of applications, from ISDN terminals to exchanges.

Because of its asynchronous bus interface, it can also be used with the other processors.

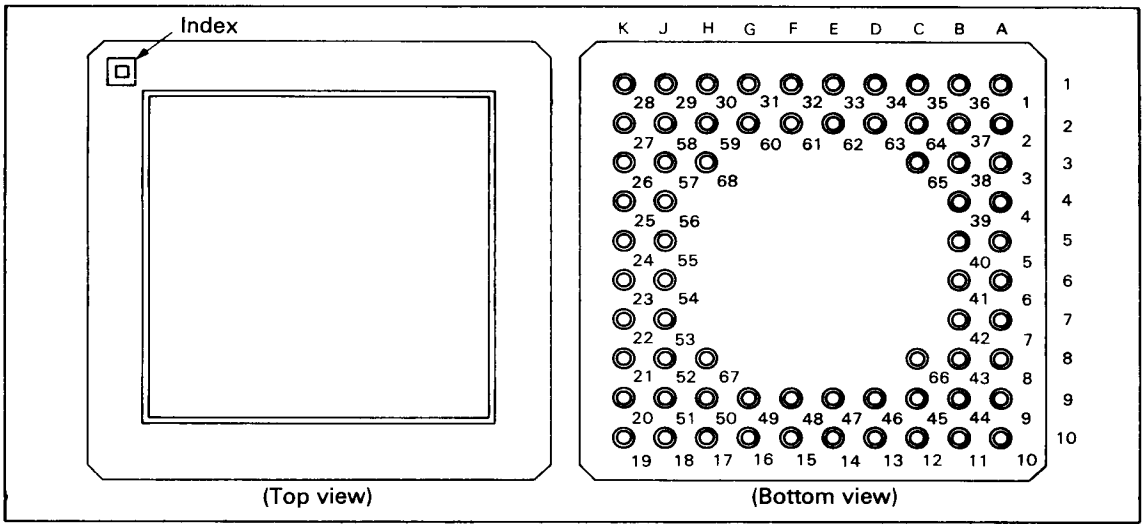
Features

- Supports CCITT recommendation I.440 and I.441 LAPD procedures
  - —Processes ISDN layer 2 protocol (LAPD)
  - —Reduces main processor load, improving system throughput
- Twenty-four simultaneous links
  - —Up to twenty-four LAPD logical links may be established across the one physical link
  - —Internal RAM stores context information for all twenty-four links
- Statistical counters
  - —Forty counters for statistical information: Counters for specific frame types transmitted or received, transmission error, etc.
  - —Reports counter status to host processor
- I.431 passive bus contention control
  - —When operating as a TE on a passive bus, manages D-channel contention by monitoring the layer 1 (I.431) D-channel echo bit
- Selectable mode and parameters
  - —Terminal/network mode, Transparent mode
  - —Link supervision by timers
  - —Parameters for each link
  - —The values of SAPI and parameters N201, K, N200, T200, and T203 are programmable in the HD64530
- Chained transmit/receive data function
  - —Long frames may be stored in multiple data buffers that are chained together and, except for UI and XID frames, may be transmitted or received
  - —Transmitted UI and XID frames are limited to a single buffer in length
- High throughput through original architecture
  - —High performance protocol processing and data transmission
- 8-64 kbps transfer data rate
  Available for basic rate interface & primarily rate interface

Ordering Information

Type No.	Max. Link Speed	Package
HD64530A02Y	64 kbps	68 pin PGA (PC-68)
HD64530A02CP	64 kbps	68 pin PLCC (CP-68)
HD64530RA03Y	2 Mbps	68 pin PGA (PC-68)
HD64530RA03CP	2 Mbps	68 pin PLCC (CP-68)

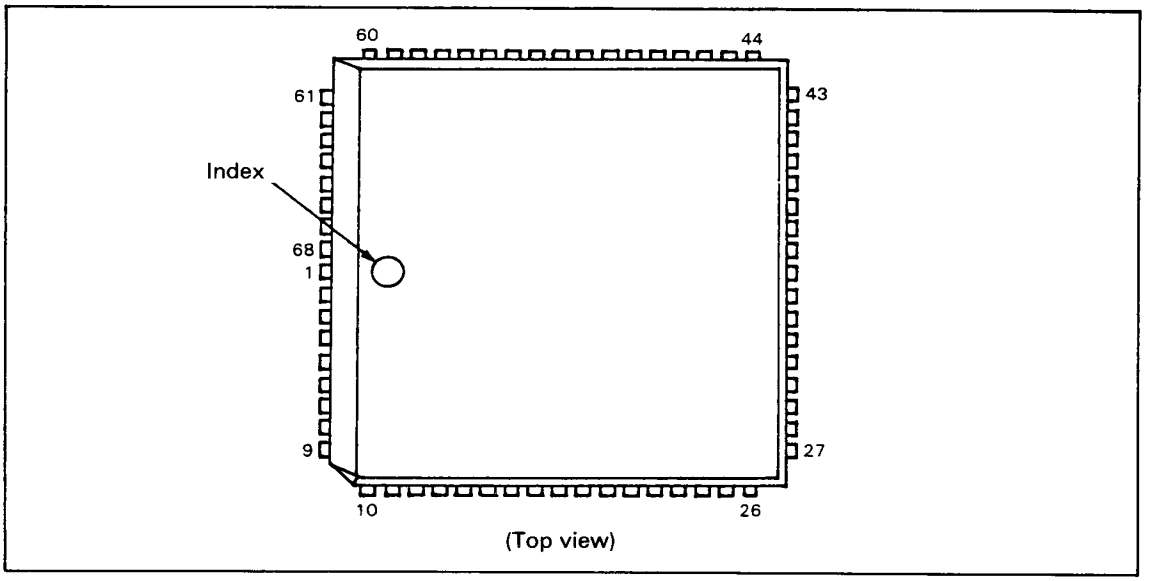
Pin Arrangement (PC-68)



Pin Code	Pin No.	Names	Pin Code	Pin No.	Names	Pin Code	Pin No.	Names
A1	1	$\overline{IRQ}$	C8	66	A_{10}/D_2	H9	50	V_{SS}
A2	2	$S/\overline{U}$	C9	45	A_{13}/D_5	H10	17	A_{21}/D_{13}
A3	3	NUM	C10	12	A_{14}/D_6	J1	29	$\overline{CS}$
A4	4	A_1	D1	34	$R/\overline{W}$	J2	58	TXC
A5	5	V_{SS}	D2	63	$\overline{LDS}$	J3	57	V_{SS}
A6	6	ϕ	D9	46	A_{15}/D_7	J4	56	V_{CC}
A7	7	A_4	D10	13	A_{16}/D_8	J5	55	PI2
A8	8	A_5	E1	33	V_{SS}	J6	54	PO1
A9	9	A_7	E2	62	V_{CC}	J7	53	NUM
A10	10	A_9/D_1	E9	47	V_{SS}	J8	52	V_{CC}
B1	36	$\overline{READY}$	E10	14	A_{17}/D_9	J9	51	V_{CC}
B2	37	$\overline{IACK}$	F1	32	$\overline{DBEN}$	J10	18	A_{23}/D_{15}
B3	38	PF	F2	61	$\overline{DIN}$	K1	28	$\overline{BREQ}$
B4	39	A_2	F9	48	A_{19}/D_{11}	K2	27	TXD
B5	40	V_{CC}	F10	15	A_{18}/D_{10}	K3	26	RXD
B6	41	A_3	G1	31	NC	K4	25	RXC
B7	42	A_6	G2	60	$\overline{AS}$	K5	24	PI1
B8	43	A_8/D_0	G9	49	A_{22}/D_{14}	K6	23	PI0
B9	44	A_{11}/D_3	G10	16	A_{20}/D_{12}	K7	22	PO0
B10	11	A_{12}/D_4	H1	30	$\overline{ABEN}$	K8	21	NUM
C1	35	$\overline{HDS}$	H2	59	$\overline{BACK}$	K9	20	$\overline{RES}$
C2	64	$\overline{AIN}$	H3	68	RXE	K10	19	$\overline{BERR}$
C3	65	NC	H8	67	$\overline{BRTRY}$			

Note: NUM: Not User Mode, NC: No Connection

Pin Arrangement (CP-68)



(Top view)

Pin No.	Pin Code	Pin No.	Pin Code	Pin No.	Pin Code
1	V_{SS}	24	A_8/D_0	47	NUM *
2	V_{CC}	25	A_9/D_1	48	NUM *
3	R/$\overline{W}$	26	A_{10}/D_2	49	PO0
4	$\overline{HDS}$	27	A_{11}/D_3	50	PO1
5	$\overline{LDS}$	28	A_{12}/D_4	51	PIO
6	$\overline{READY}$	29	A_{13}/D_5	52	PI1
7	$\overline{AIN}$	30	A_{14}/D_6	53	PI2
8	$\overline{IRQ}$	31	A_{15}/D_7	54	RXC
9	$\overline{IACK}$	32	A_{16}/D_8	55	RXD
10	NC **	33	V_{SS}	56	V_{SS}
11	S/$\overline{U}$	34	A_{17}/D_9	57	V_{CC}
12	PF	35	A_{18}/D_{10}	58	TXD
13	NUM *	36	A_{19}/D_{11}	59	TXC
14	A_1	37	A_{20}/D_{12}	60	RXE
15	A_2	38	A_{21}/D_{13}	61	$\overline{BREQ}$
16	V_{SS}	39	A_{22}/D_{14}	62	$\overline{BACK}$
17	V_{CC}	40	A_{23}/D_{15}	63	$\overline{CS}$
18	ϕ	41	V_{SS}	64	$\overline{AS}$
19	A3	42	V_{CC}	65	$\overline{ABEN}$
20	A_4	43	V_{CC}	66	NC **
21	A_5	44	$\overline{BRTRY}$	67	$\overline{DIN}$
22	A_6	45	$\overline{BERR}$	68	$\overline{DBEN}$
23	A_7	46	$\overline{RES}$		

* NUM: Not Users Mode
** NC: Non Connection

Function Table

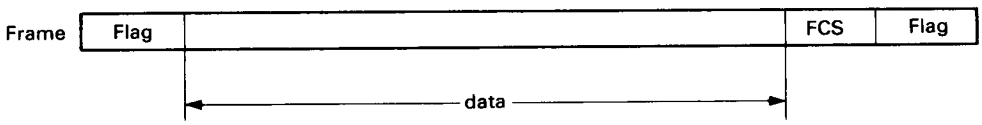
Table 1 summarizes HD64530 functions.

Table 1. HD64530 Function

Feature	Function
Communication protocol	CCITT I.440 and I.441
Line rate (data rate)	8 to 64 kbps, 8 kbps to 2 Mbps (High-speed version)
Number of lines	One full-duplex line
Number of logical links	Up to 24 simultaneous logical links can be set
Operation mode	TE Mode/NT Mode, *Transparent mode (Note) (D channel contention management is included in TE mode)
Selectable parameters (Timers and counters can be selected for each link)	Maximum number of retransmissions (1 to 15) N200
	Maximum number of octets in an information field (1 to 16,383) N201
	Maximum time allowed without acknowledged frames T200 (0.1 to 25.5 seconds, 0.1 second steps)
	Maximum time allowed without frames being exchanged T203 (0.1 to 25.5 seconds, 0.1 second steps)
	Maximum number of outstanding I frames (1 to 127) K
	Timefill between frames (mark/flag)
Diagnostics	Auto-echo
	Local loopback
	Auto echo and local loopback
Peripheral I/O ports	3 inputs, 2 outputs (general-purpose I/O, level detection)
Data encoding	NRZ serial data
Bus interface (asynchronous)	16-bit MPU
Data transfer with memory	DMA
Address space	16 Mbyte
Data bus width	16 bits (multiplexed with address bus)

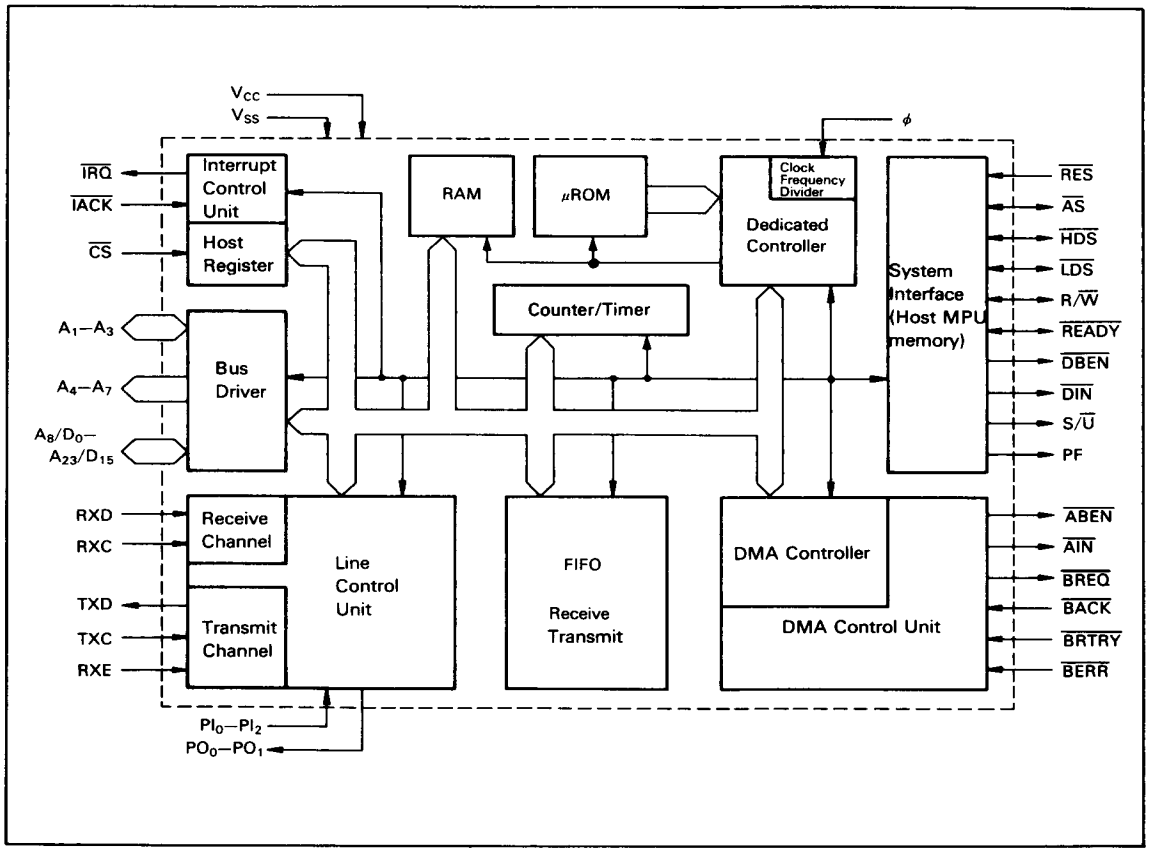
Note: Transparent Mode

Transmit; Transmit the data which is set by host CPU adding flags and FCS.
Receive; Receive all the data between flags and FCS.



Frame format in Transparent Mode

Block Diagram



System Block Configuration

Figure 1 is an example of a system configuration using the HD64530. The HD64530 processes the D channel signal received from the layer 1 interface circuit according to LAPD procedure. The processed result is sent to the host MPU. Transmit data is transferred to the layer 1 interface circuit according to commands from the host MPU.

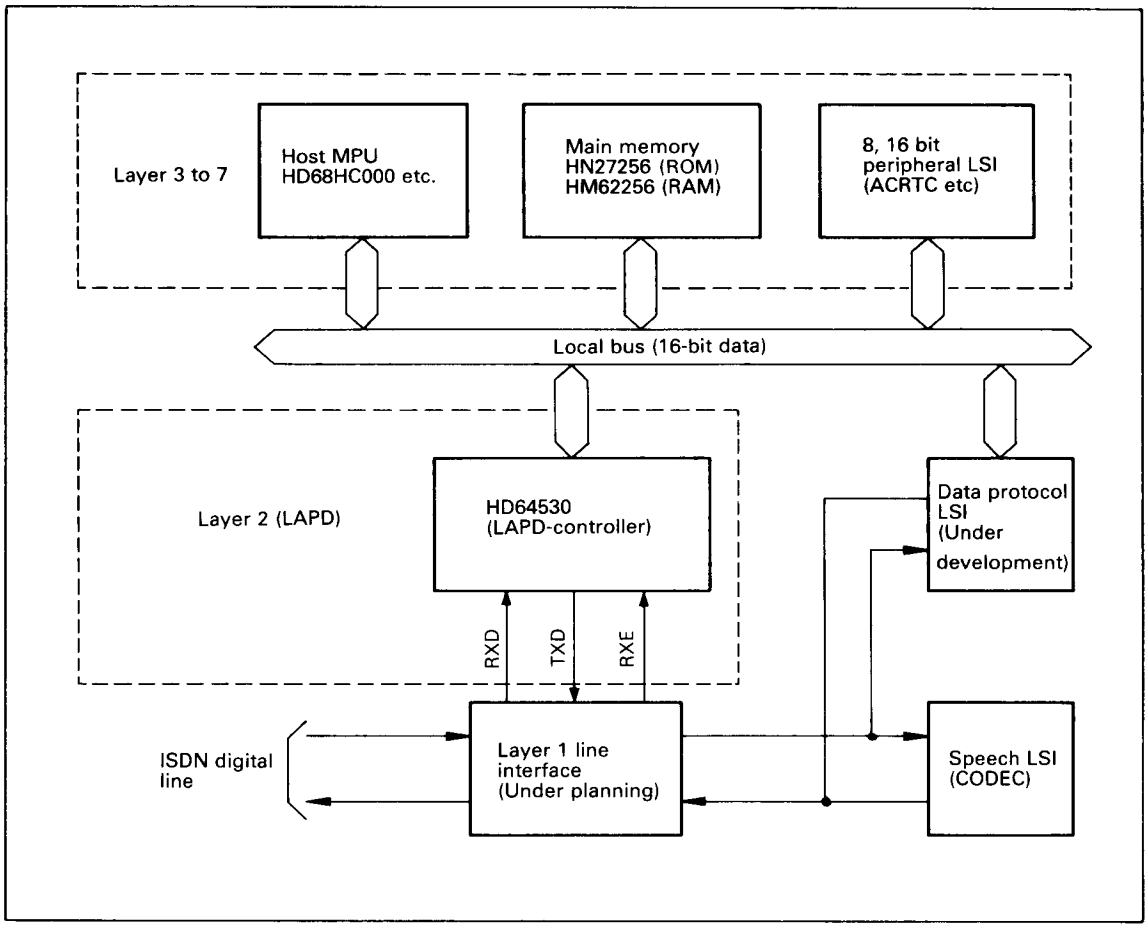


Figure 1. System Configuration Block Diagram