HB56HW165DB-6BL/7BL

1,048,576-word × 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-572(Z)
Preliminary - Rev.0.0
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Description

The HB56HW165DB is a 1M × 64 dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 4 pieces of 16-Mbit DRAM (HM51W18165BLTT) sealed in TSOP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD).

The HB56HW165DB offers Extended Data Out (EDO) Page Mode as a high speed access mode.

An outline of the HB56HW165DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56HW165DB makes high density mounting possible without surface mount technology. The HB56HW165DB provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

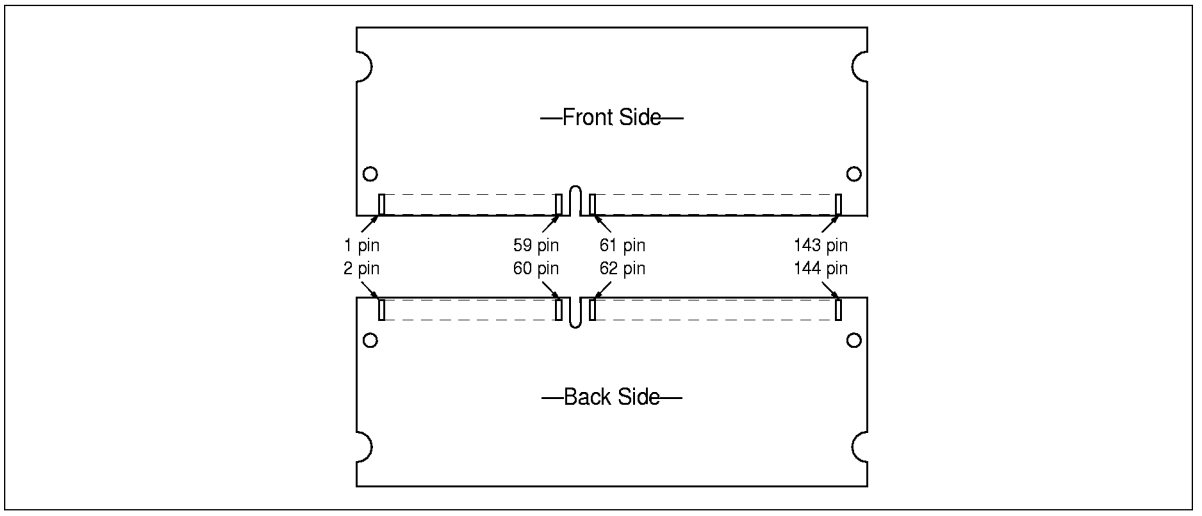
Features

- 144-pin Zig Zag Dual tabs socket type
  - — Lead pitch: 0.80 mm
- Single 3.3 V (±0.3 V) supply
- High speed
  - — Access time: t_{RAC} = 60/70ns (max)
  - — Access time: t_{CAC} = 15/18ns (max)
- Low power dissipation
  - — Active mode: 2.45/2.16W (max)
  - — Standby mode (TTL): 28.8 mW (max)
  - — Standby mode (CMOS): 2.16 mW (max)
- EDO page mode capability
- 1,024 refresh cycle: 128 ms
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh

Ordering Information

Type No.	Access time	Package	Contact pad
HB56HW165DB-6BL	60 ns	Small outline DIMM (144-pin)	Gold
HB56HW165DB-7BL	70 ns	Small outline DIMM (144-pin)	Gold

Pin Arrangement



Pin Arrangement

Front Side				Back side			
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	73	$\overline{OE}$	2	V_{SS}	74	NC
3	DQ0	75	V_{SS}	4	DQ32	76	V_{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V_{CC}	10	DQ35	82	V_{CC}
11	V_{CC}	83	DQ16	12	V_{CC}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V_{SS}	20	DQ39	92	V_{SS}
21	V_{SS}	93	DQ20	22	V_{SS}	94	DQ52
23	$\overline{CE0}$	95	DQ21	24	$\overline{CE4}$	96	DQ53
25	$\overline{CE1}$	97	DQ22	26	$\overline{CE5}$	98	DQ54
27	V_{CC}	99	DQ23	28	V_{CC}	100	DQ55
29	A0	101	V_{CC}	30	A3	102	V_{CC}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	NC
35	V_{SS}	107	V_{SS}	36	V_{SS}	108	V_{SS}
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	NC	40	DQ41	112	NC
41	DQ10	113	V_{CC}	42	DQ42	114	V_{CC}
43	DQ11	115	$\overline{CE2}$	44	DQ43	116	$\overline{CE6}$
45	V_{CC}	117	$\overline{CE3}$	46	V_{CC}	118	$\overline{CE7}$
47	DQ12	119	V_{SS}	48	DQ44	120	V_{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V_{SS}	127	DQ27	56	V_{SS}	128	DQ59
57	NC	129	V_{CC}	58	NC	130	V_{CC}
59	NC	131	DQ28	60	NC	132	DQ60
61	NC	133	DQ29	62	NC	134	DQ61
63	V_{CC}	135	DQ30	64	V_{CC}	136	DQ62
65	NC	137	DQ31	66	NC	138	DQ63
67	$\overline{WE}$	139	V_{SS}	68	NC	140	V_{SS}
69	$\overline{RE0}$	141	SDA	70	NC	142	SCL
71	NC	143	V_{CC}	72	NC	144	V_{CC}

Pin Description

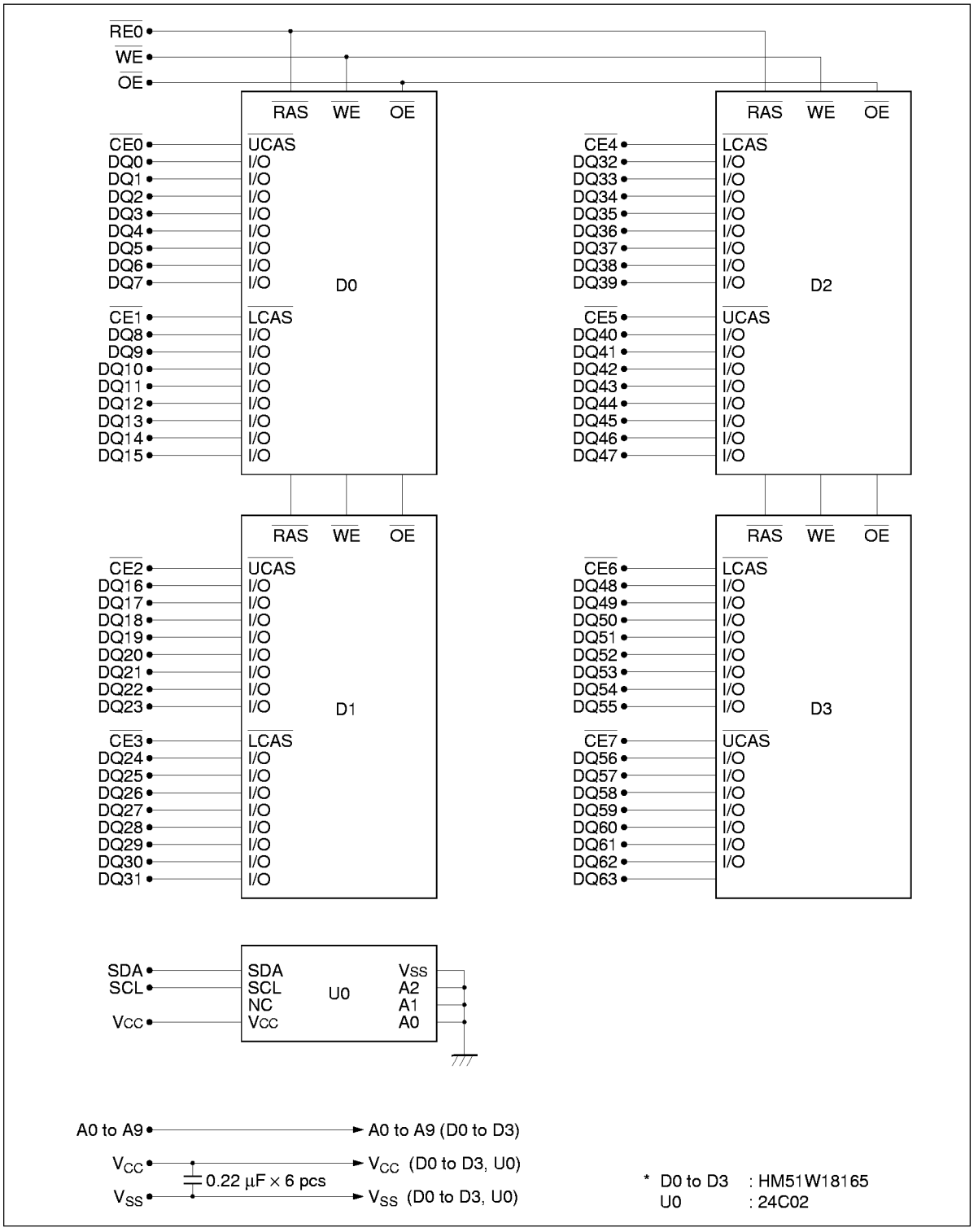
Pin Name	Function
A0 to A9	Address Input: A0 to A9 — Row Address: A0 to A9 — Column Address: A0 to A9 — Refresh Address: A0 to A9
DQ0 to DQ63	Data-in/Data-out
$\overline{RE0}$	Row Address Strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE7}$	Column Address Strobe ($\overline{CAS}$)
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
SDA	Serial Data for PD
SCL	Serial Clock for PD
NC	Non Connection

Serial PD Matrix

Byte Number	Function Described		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Note
0	Number Serial PD Bytes		0	0	0	0	1	1	0	1	13
1	Serial Memory		0	0	0	0	1	0	0	0	256 Bytes
2	Fundamental Memory Type		0	0	0	0	0	0	1	0	EDO
3	Number of Rows		0	0	0	0	1	0	1	0	10
4	Number of Columns		0	0	0	0	1	0	1	0	10
5	Number of Banks		0	0	0	0	0	0	0	1	1
6	Data Width		0	1	0	0	0	0	0	0	64
7	Data Width (continued)		0	0	0	0	0	0	0	0	0 (+)
8	Voltage Interface		0	0	0	0	0	0	0	1	LVTTL (3.3V)
9	$\overline{RAS}$ Access Time	60 ns	0	0	1	1	1	1	0	0	
9	$\overline{RAS}$ Access Time	70 ns	0	1	0	0	0	1	1	0	
10	$\overline{CAS}$ Access Time	15 ns	0	0	0	0	1	1	1	1	
10	$\overline{CAS}$ Access Time	18 ns	0	0	0	1	0	0	1	0	
11	Error Detection/Corraction		0	0	0	0	0	0	0	0	None
12	Refresh Period		1	0	0	0	0	1	0	1	Self Refresh (125 µs)

Note: Serial-PD Datas are not protected.
1: High Level (Serial Data)
0: Low Level (Serial Data)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	4	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V)

		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test condition**	**Note**
Operating current	I_{CC1}	—	680	—	600	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	8	—	8	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	0.6	—	0.6	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	680	—	600	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	20	—	20	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	680	—	600	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	740	—	660	mA	t_{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh)	I_{CC10}	—	1.6	—	1.6	mA	CMOS interfase Dout = High-Z CBR refresh: t_{RC} = 125 µs t_{RAS} ≤ 0.3 µs	4
Self refresh mode current	I_{CC11}	—	1	—	1	mA	CMOS interfase $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V Dout = High-Z	
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC}-0.2V, 0V ≤ V_{IL} ≤ 0.2 V

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	40	pF	1
Input capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	48	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	22	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) *1, *2, *18, *19

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	48	—	58	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7
Refresh period (4,096 cycles)	t_{REF}	—	128	—	128	ms	

Read Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	15	—	15	ns	
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	15	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	18	—	ns	

Write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	ns	15

Read-Modify-write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	136	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	t_{OEH}	15	—	18	—	ns	

Refresh Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	ns	

EDO Page Mode Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	ns	
Output data hole time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time refferred $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	ns	

EDO Page Mode Read-Modify-write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read-modify-write cycle time	t_{HPRWC}	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	ns	14

Refresh Cycle

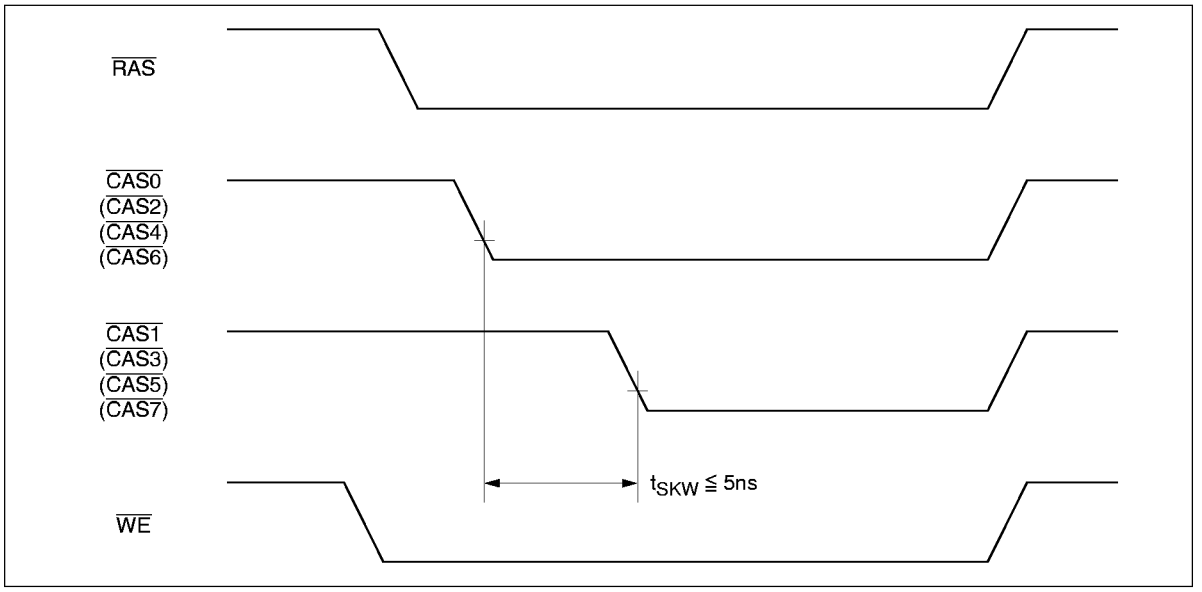
		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ Pulse width (self-refresh)	t_{RASS}	100	—	100	—	µs	
$\overline{RAS}$ precharge time (self-refresh)	t_{RPS}	110	—	130	—	ns	
$\overline{CAS}$ hold time (self-refresh)	t_{CSH}	-50	—	-50	—	ns	

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max)- t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics onry; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min) or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); $t_{OEH} < t_{OEH}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.

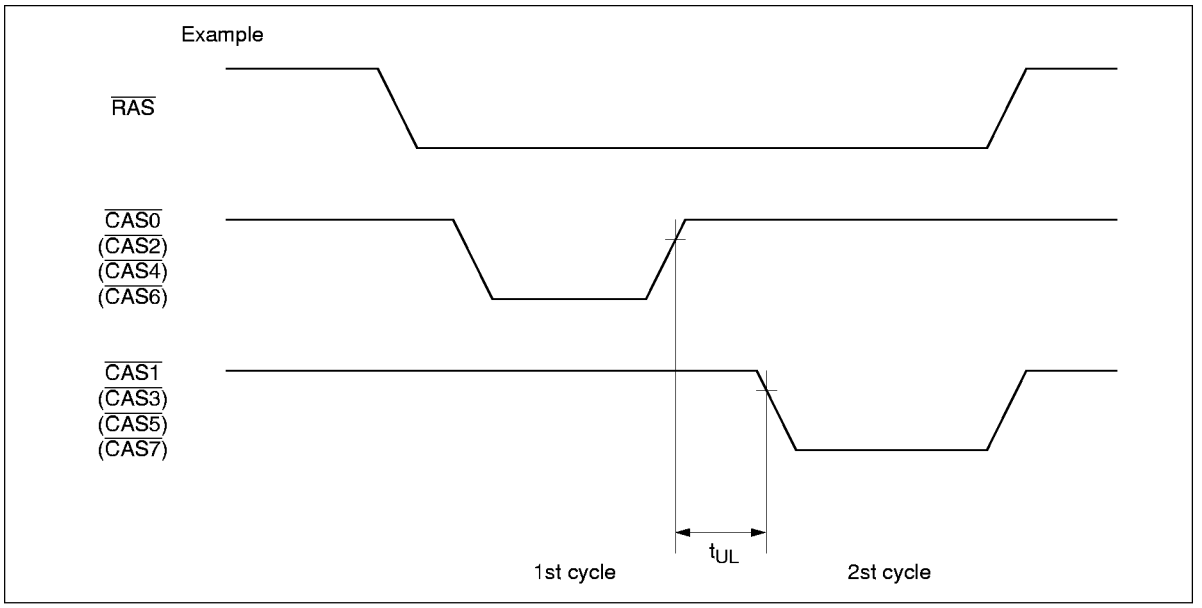
Notes concerning 2$\overline{\text{CAS}}$ control

(1) In one memory cycle, activate both of 2$\overline{\text{CAS}}$s ($\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ (or $\overline{\text{CAS2}}$, 4, 6 and $\overline{\text{CAS3}}$, 5, 7)) or only one of them or neither of them.

(2) To activate both of 2$\overline{\text{CAS}}$s in an early write cycle or a page mode early write cycle, please keep t_{SKW} (skew between $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ (or $\overline{\text{CAS2}}$, 4, 6 and $\overline{\text{CAS3}}$, 5, 7)) 5 ns or less.



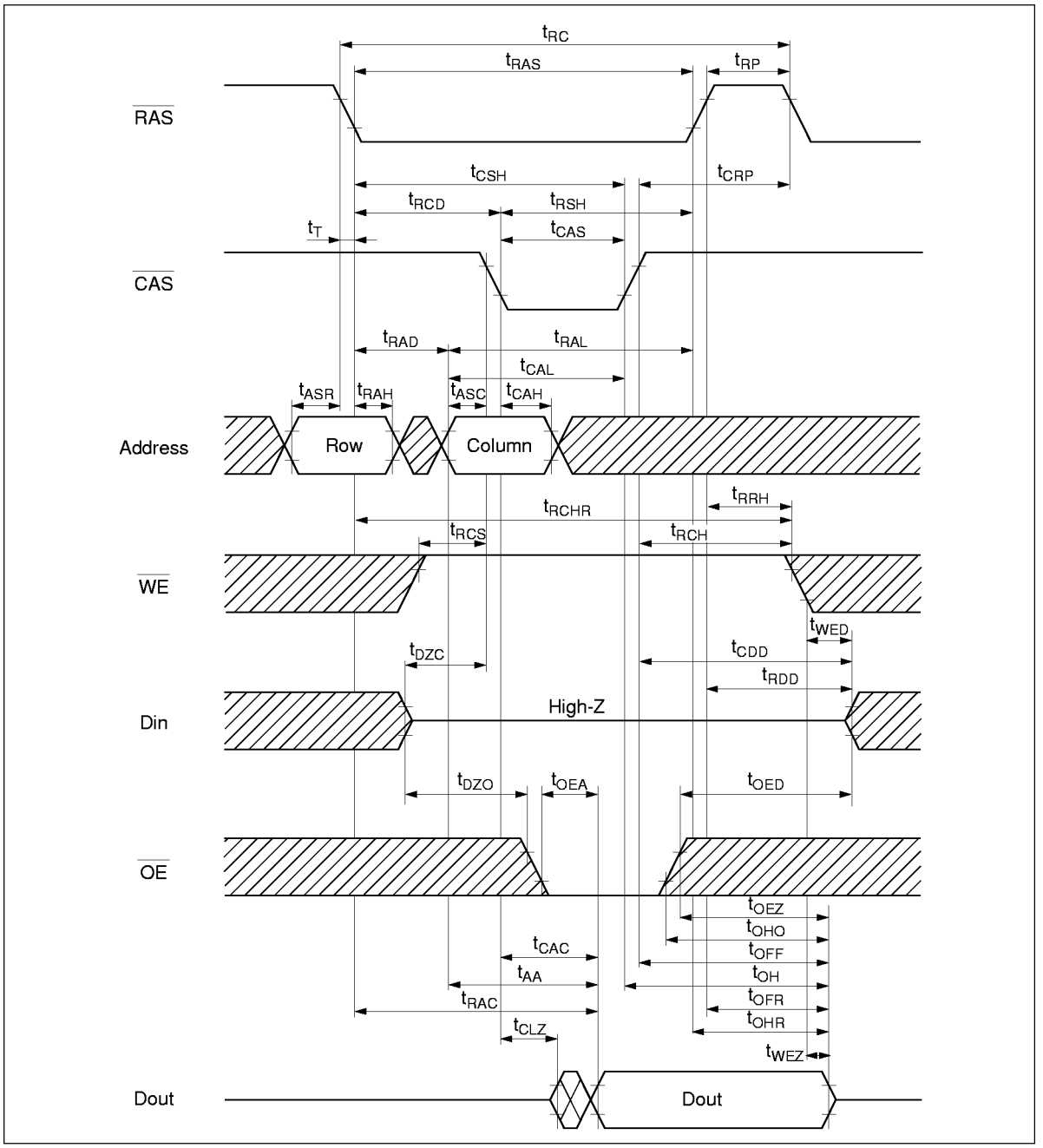
(3) If the different $\overline{\text{CAS}}$s are activated in the consecutive page cycles, t_{UL} the period that both $\overline{\text{CAS}}$s are high, should be keep t_{CP} spec (t_{CP} min ≤ t_{UL}).



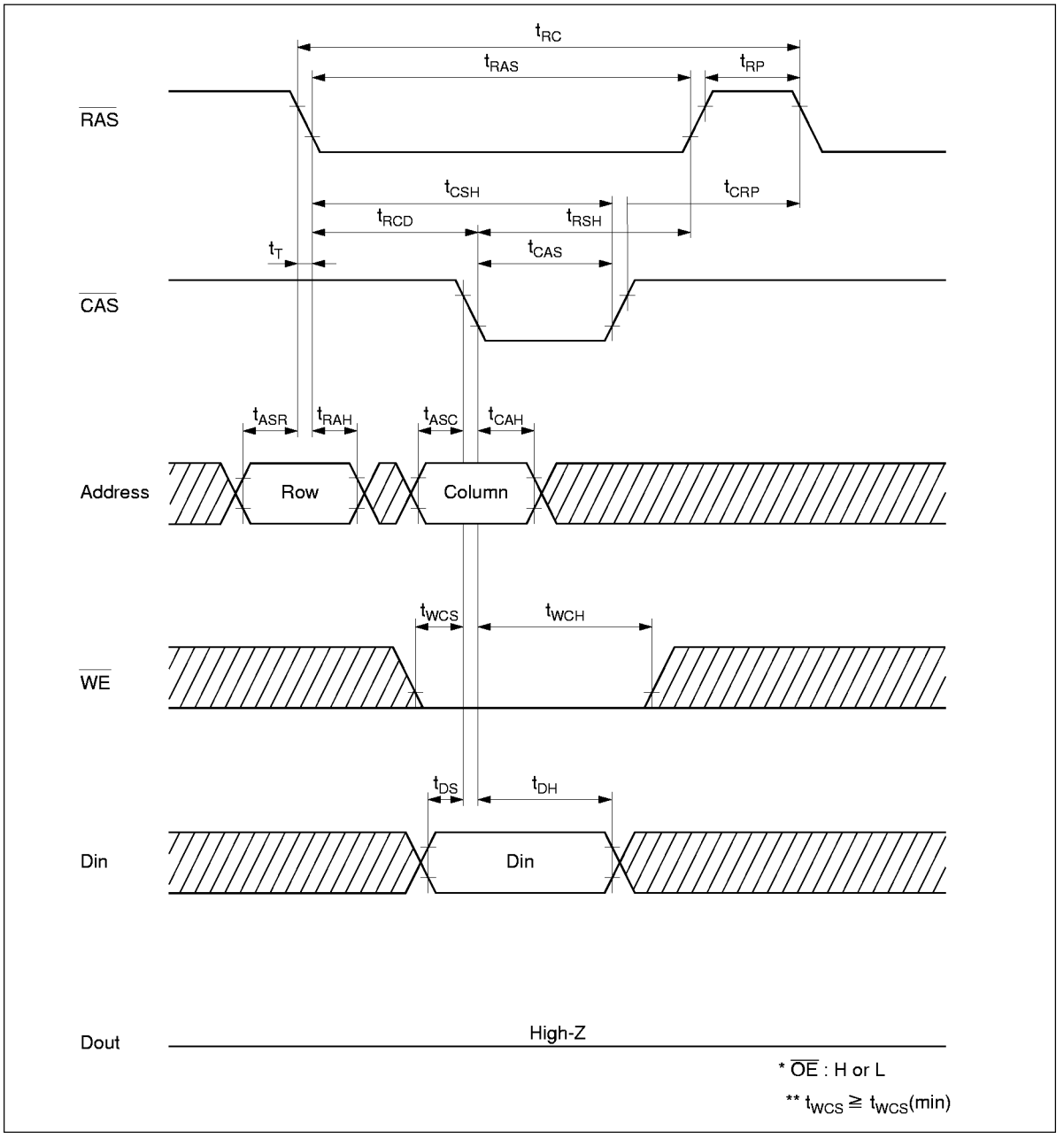
Timing Waveform

Note : //////: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))
XXX: Invalid Dout

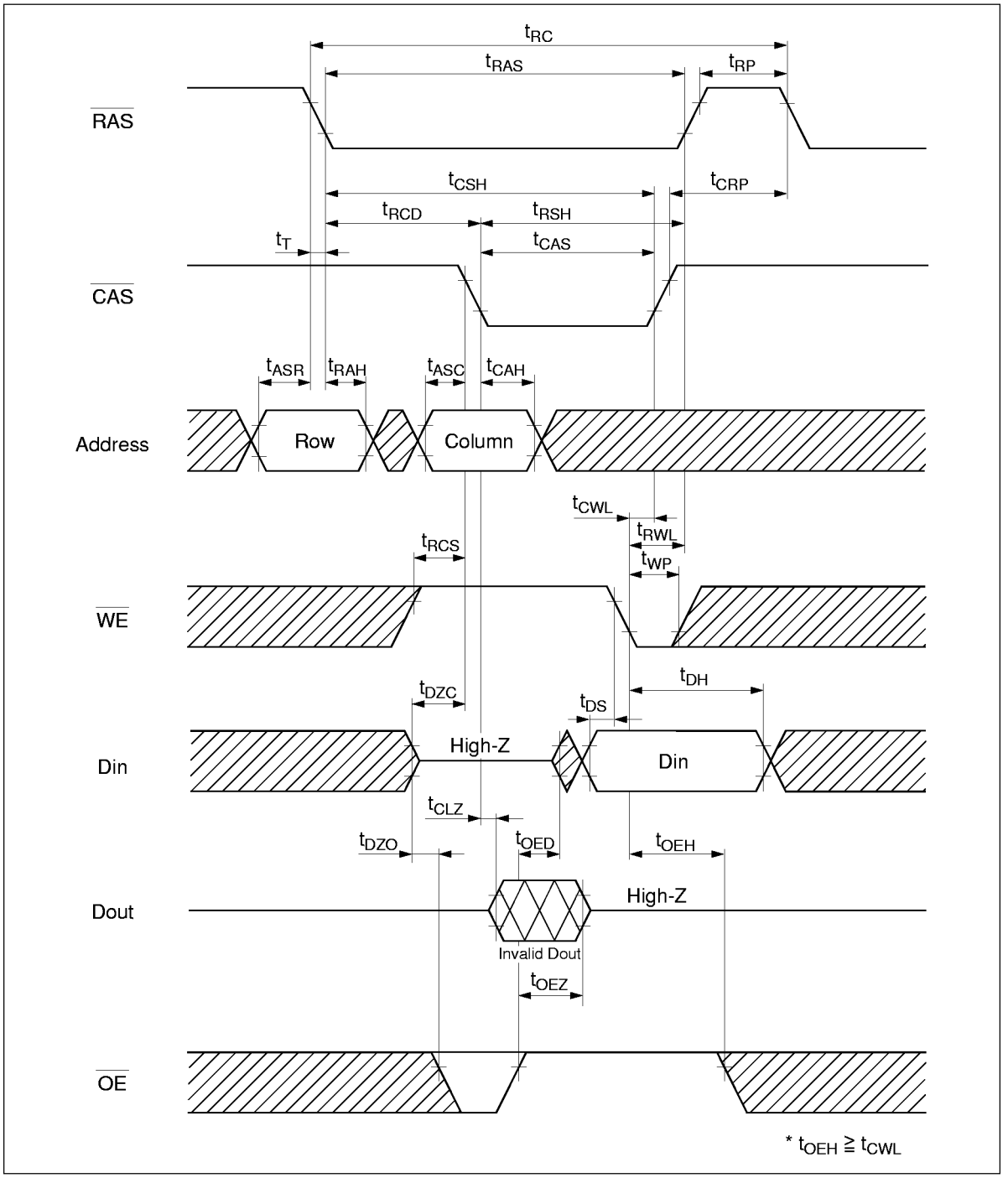
Read Cycle



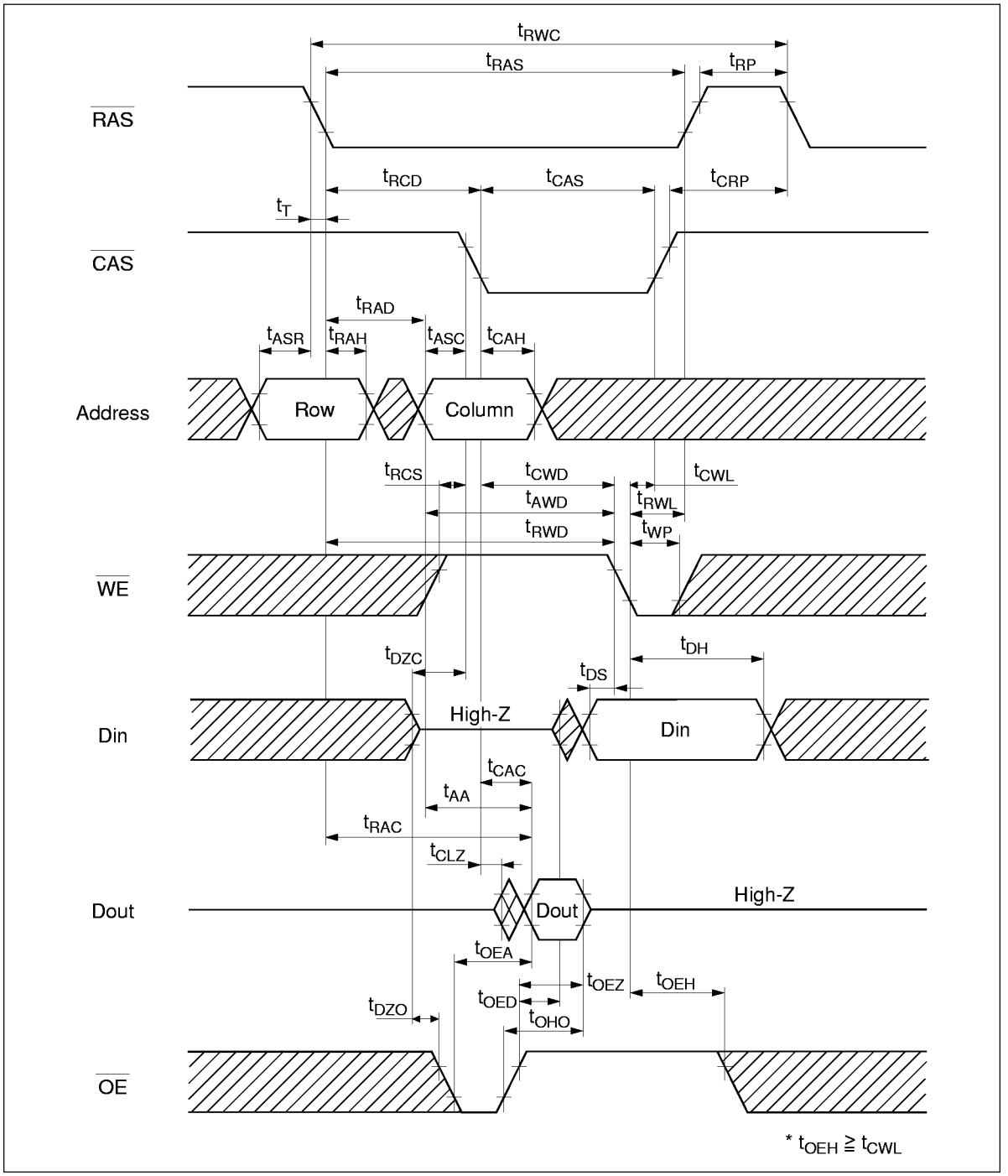
Early Write Cycle



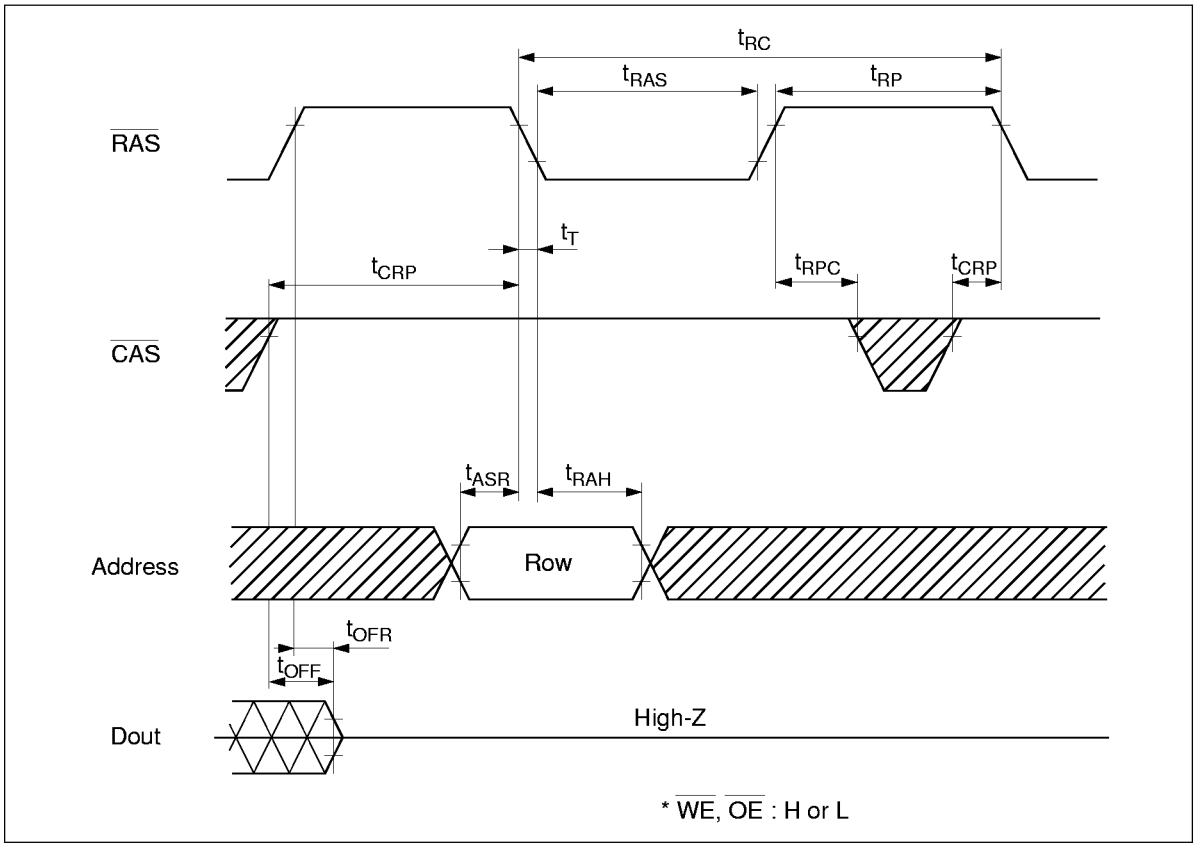
Delayed Write Cycle



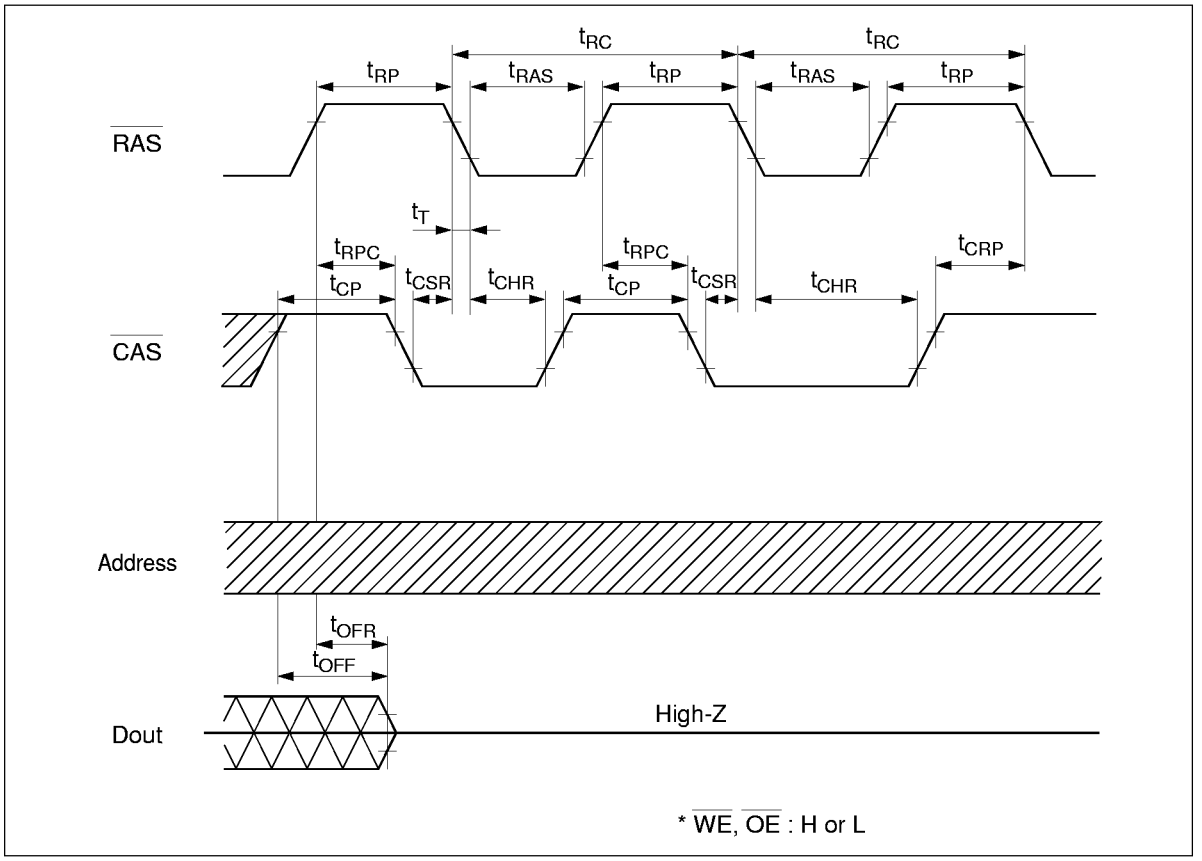
Read-Modify-Write Cycle



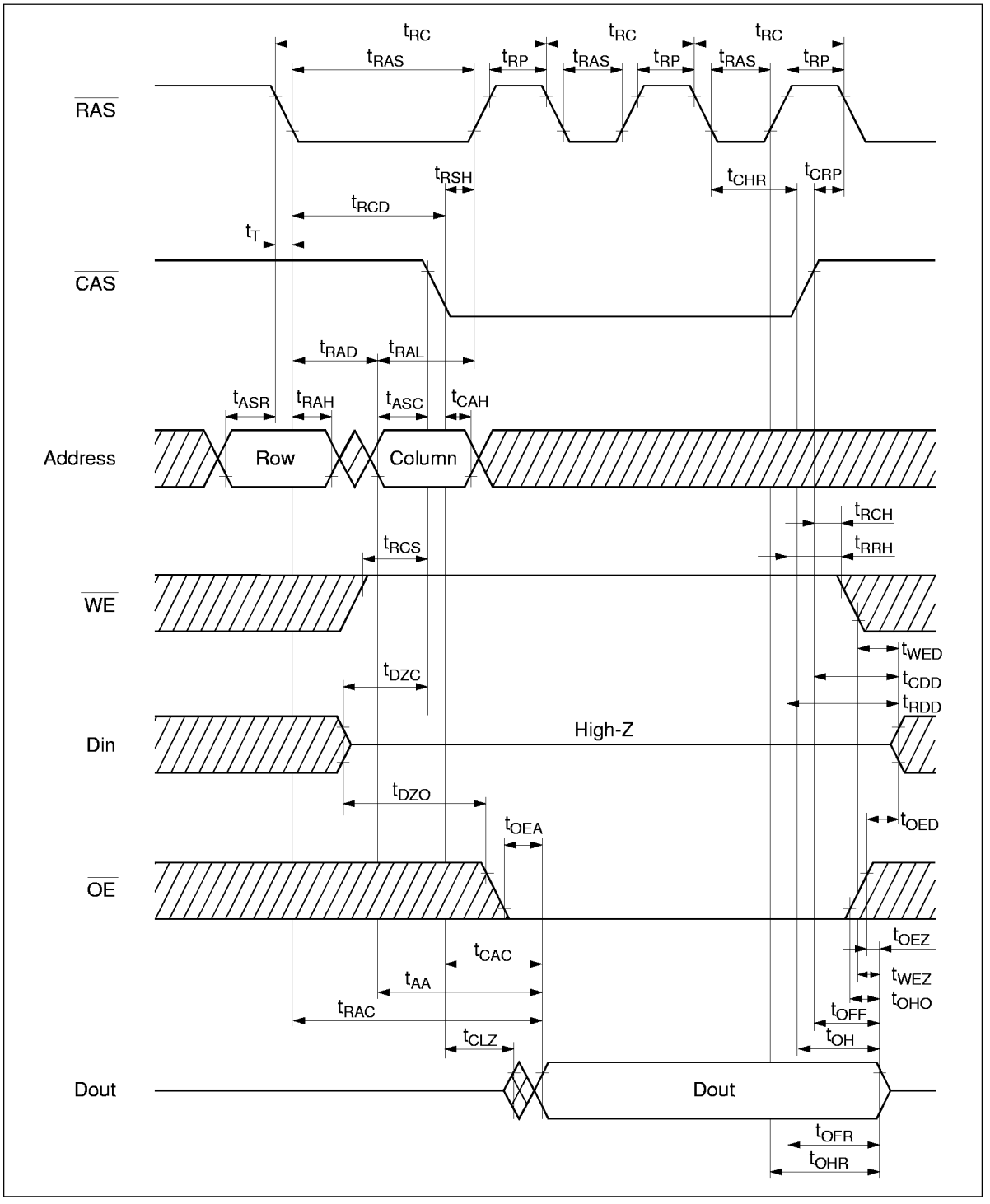
$\overline{\text{RAS}}$-Only Refresh Cycle



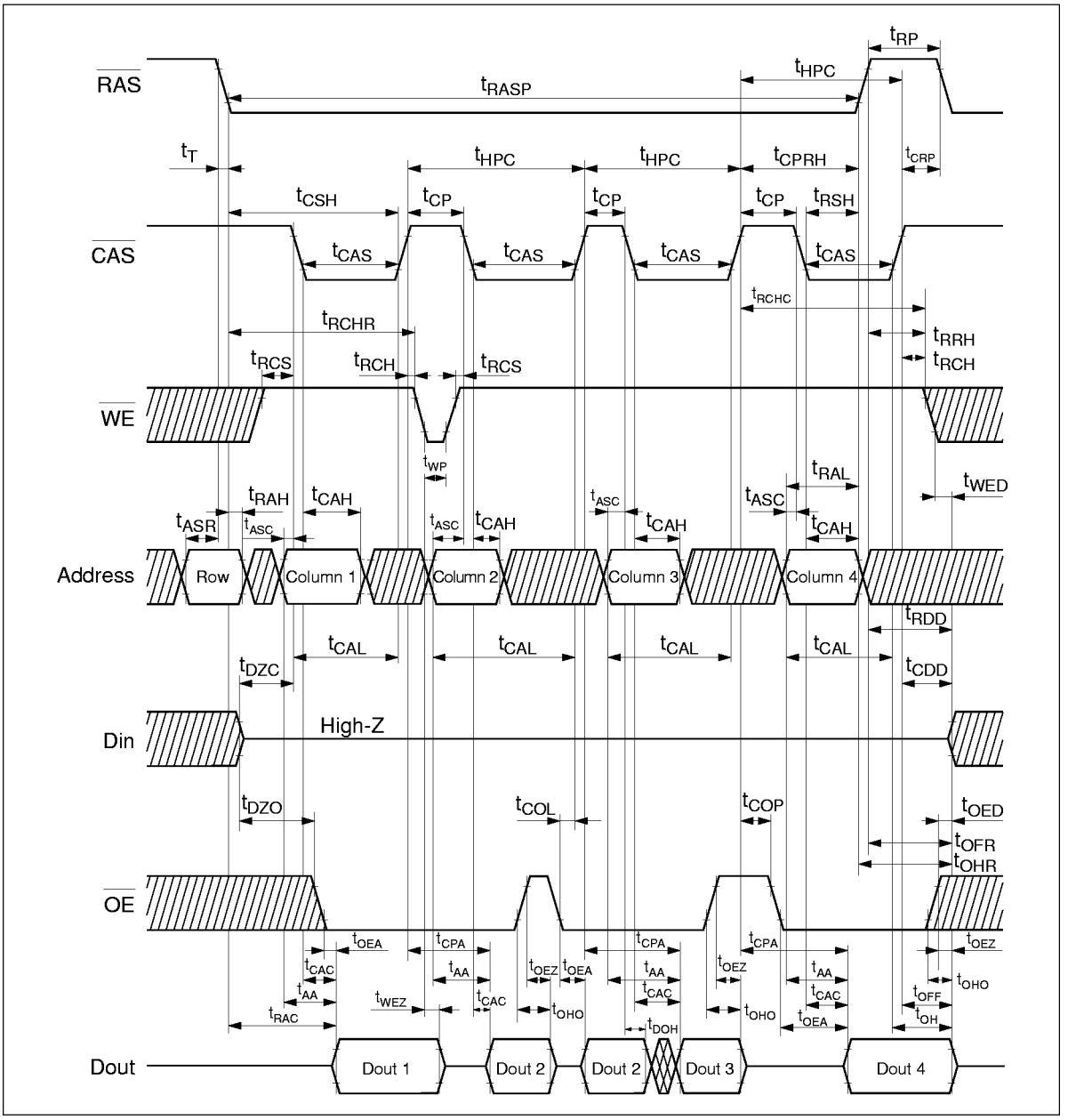
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



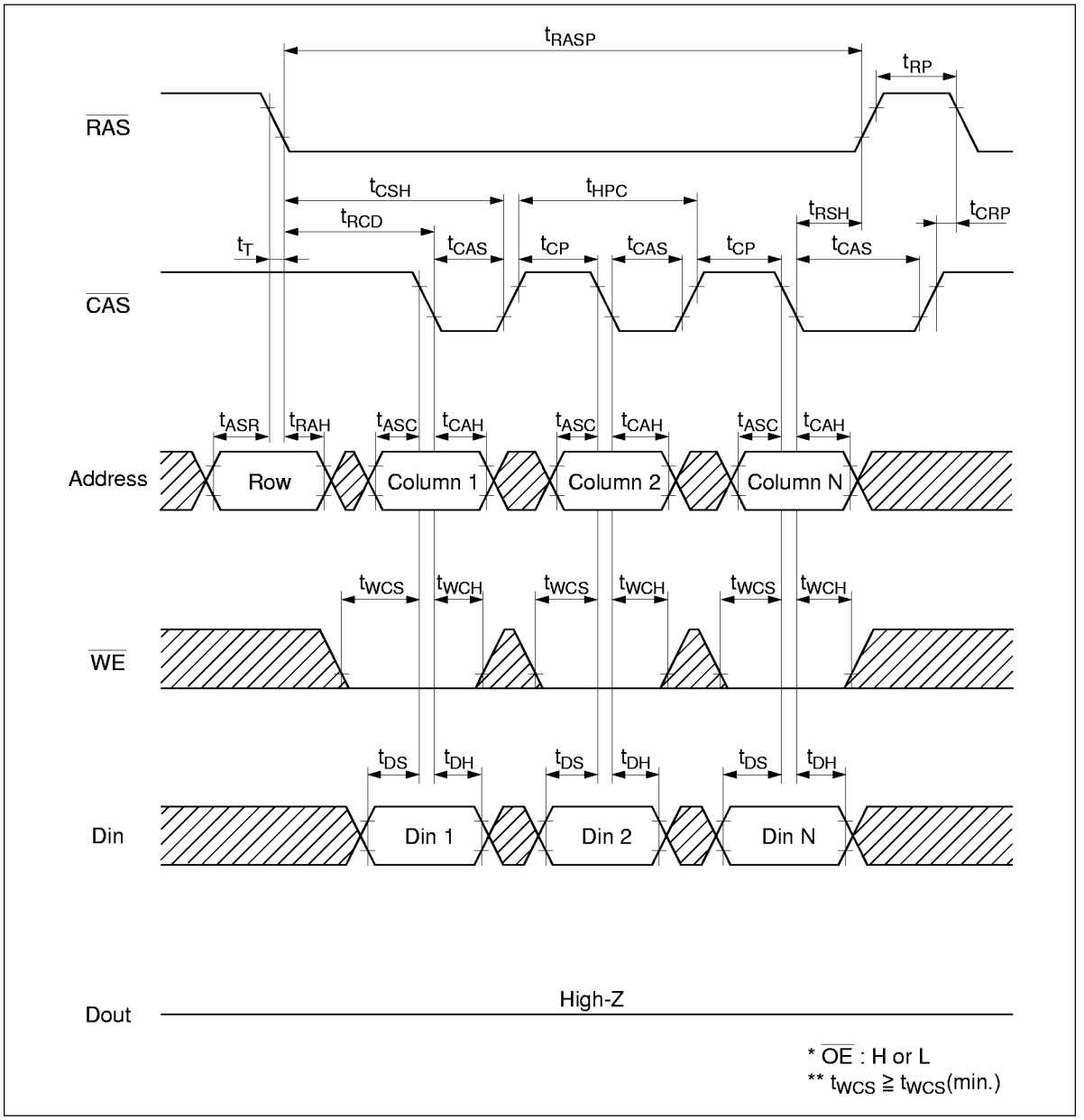
Hidden Refresh Cycle



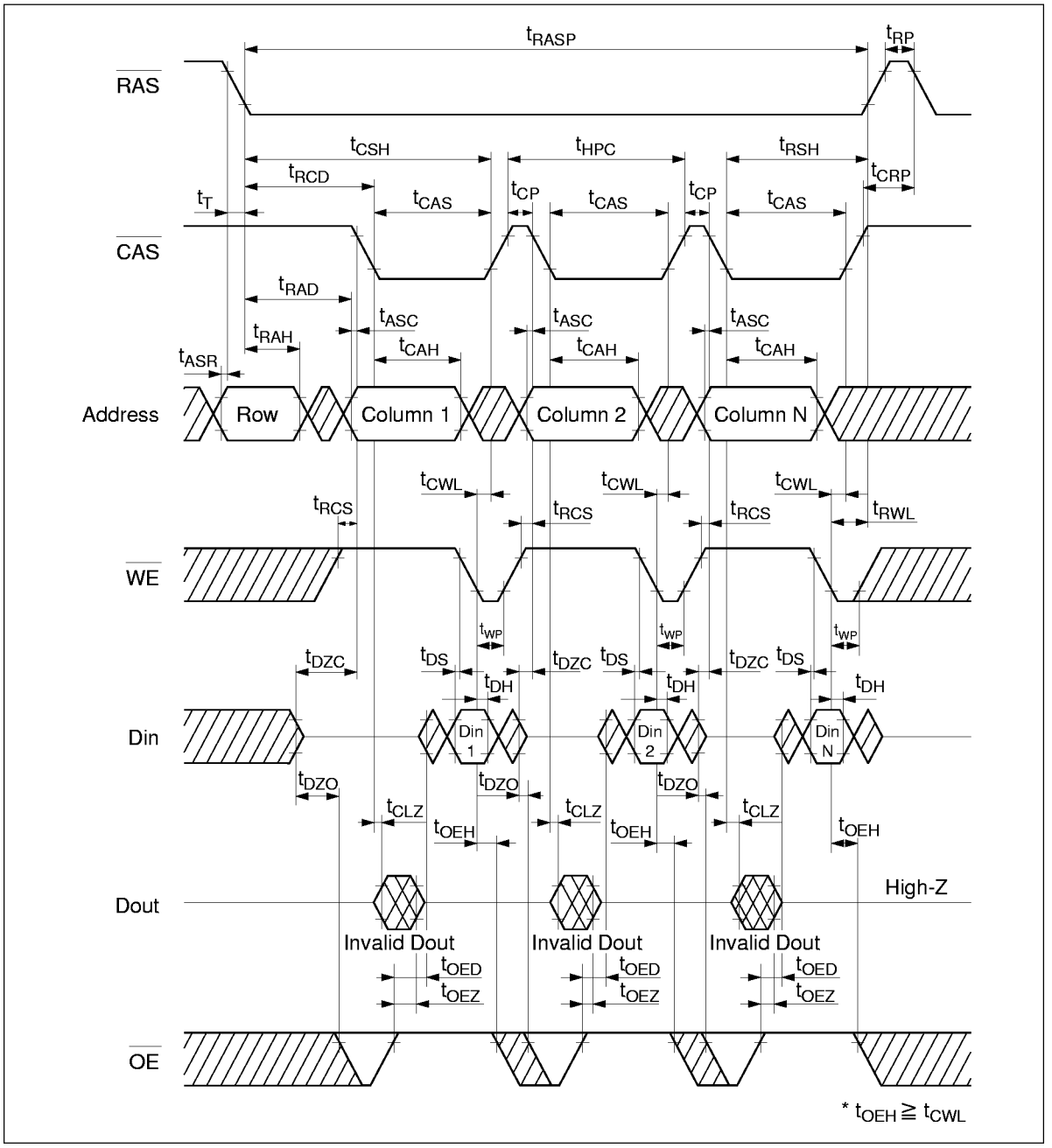
EDO Page Mode Read Cycle



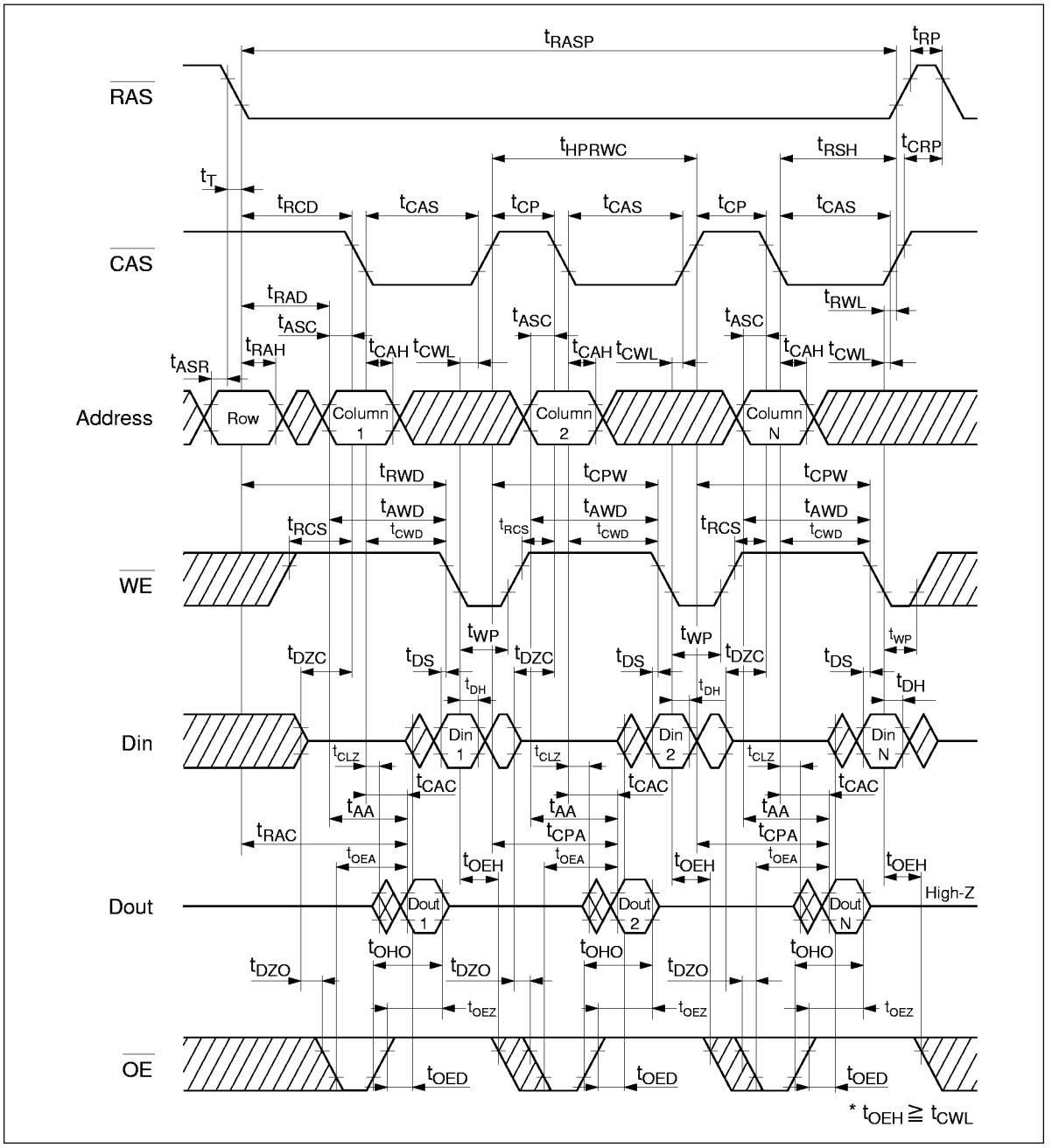
EDO Page Mode Early Write Cycle



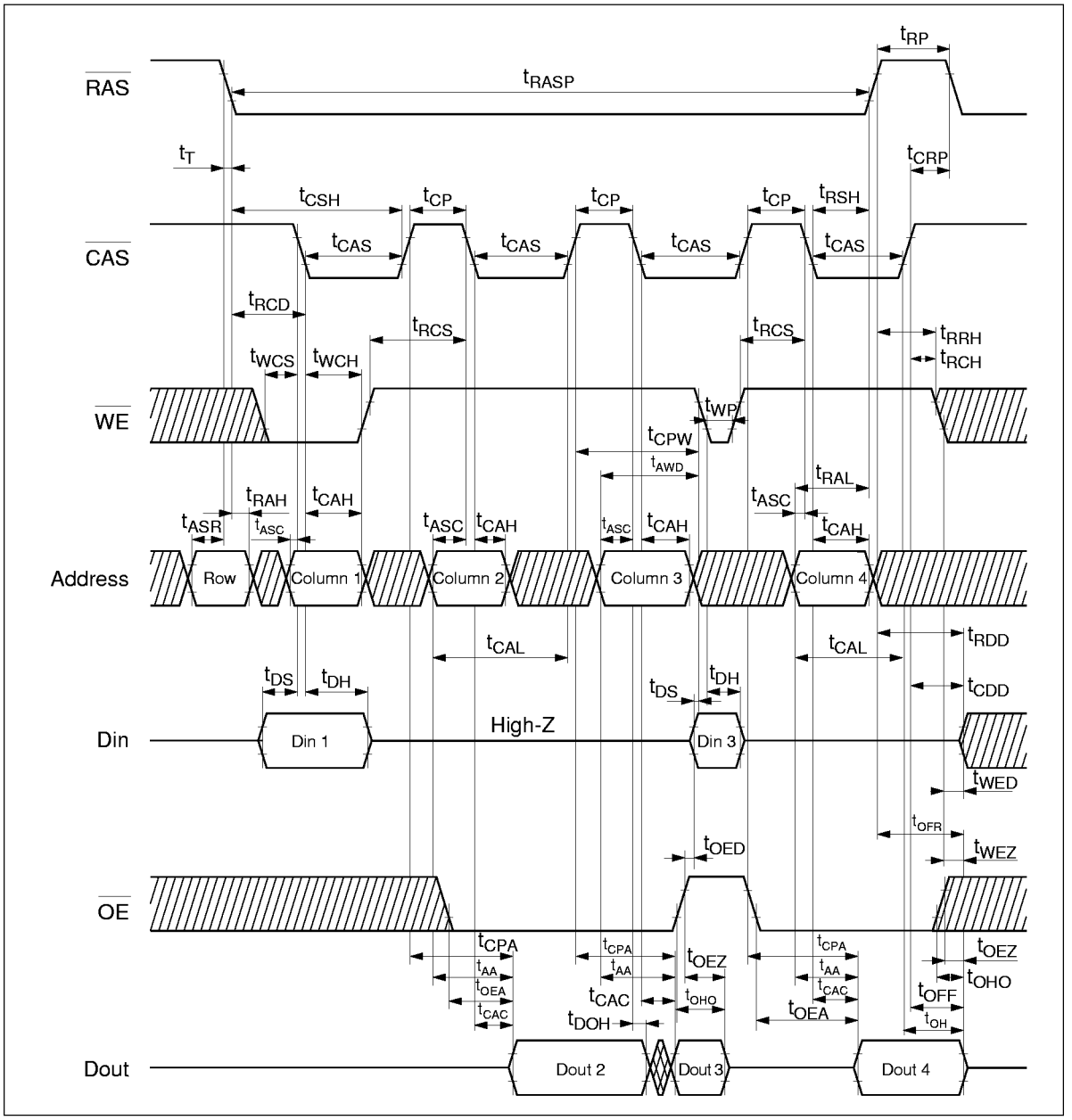
EDO Page Mode Delayed Write Cycle



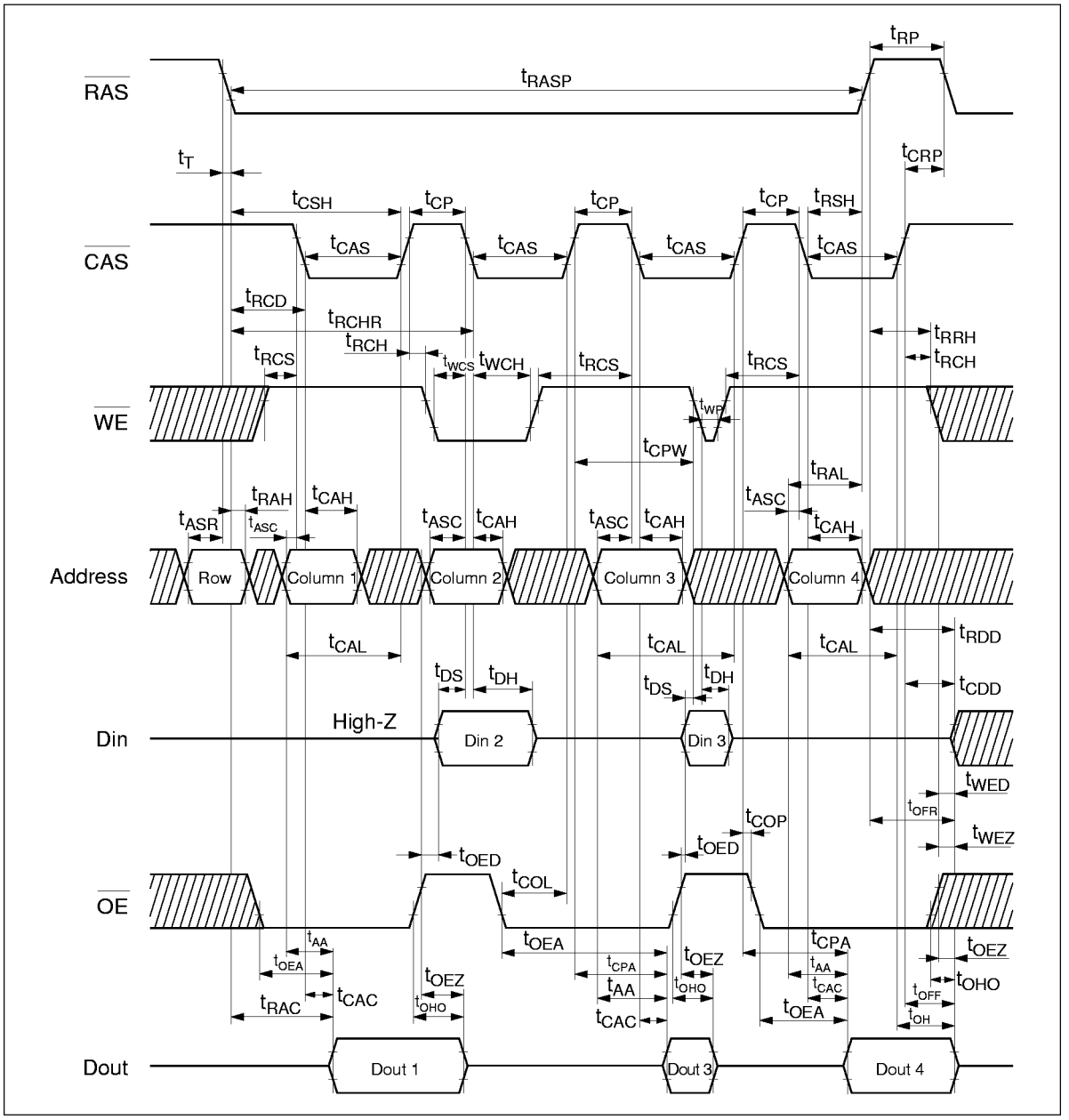
EDO Page Mode Read-Modify-Write Cycle



EDO Page Mode Mix Cycle (1)



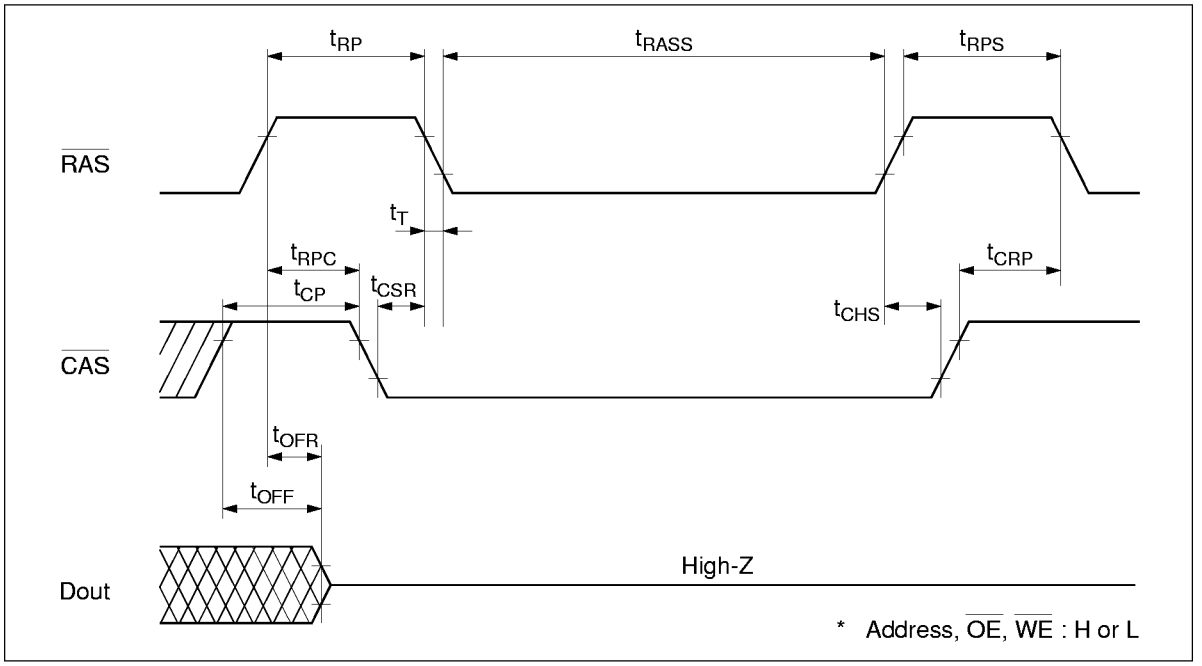
EDO Page Mode Mix Cycle (2)



Self Refresh Cycle

The low self refresh current is achieved by introducing extremely long intermal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, 10 µs ≤ t_{RASS} ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} ≥ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
3. If you rse distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.



Physical Outline

Unit: mm/inch