

## 4-Mbit (256K x 16) Static RAM

### Features

- **Temperature Ranges**
  - Industrial:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
  - Automotive-A:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
  - Automotive-E:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62147CV25, CY62147CV30, and CY62147CV33**
- **Ultra-low active power**
  - Typical active current: 1.5 mA @  $f = 1\text{ MHz}$
  - Typical active current: 8 mA @  $f = f_{\text{max}}$
- **Ultra low standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$ , and  $\overline{\text{OE}}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball VFBGA and non Pb-free 44-pin TSOPII**
- **Byte power-down feature**

### Functional Description<sup>[1]</sup>

The CY62147DV30 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features ad-

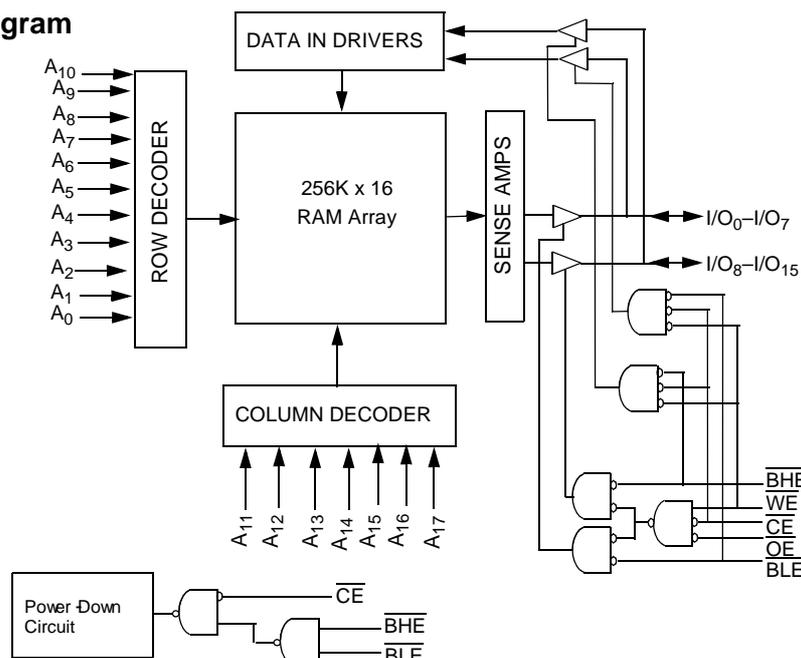
vanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{\text{CE}}$  HIGH or both  $\overline{\text{BLE}}$  and  $\overline{\text{BHE}}$  are HIGH). The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ), is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62147DV30 is available in a 48-ball VFBGA, 44 Pin TSOPII packages.

### Logic Block Diagram

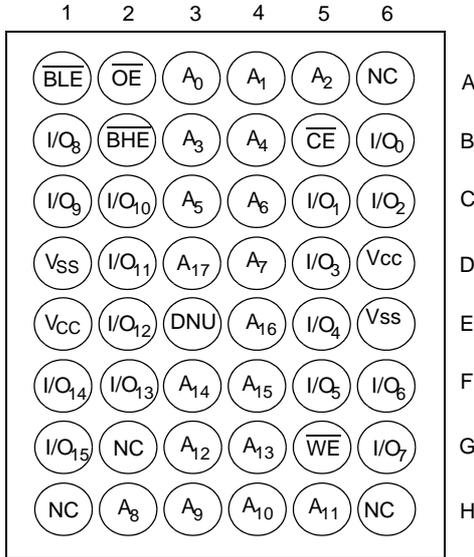


#### Note:

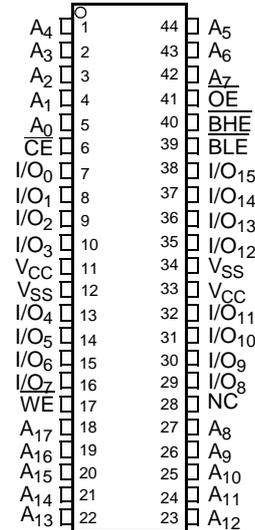
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration<sup>[2, 3, 4]</sup>

VFBGA (Top View)



44 TSOP II (Top View)



Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)		Speed (ns)	Power Dissipation						
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)		
					f = 1MHz		f = f <sub>max</sub>				
Min.	Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.			
CY62147DV30LL	Industrial	2.2V	3.0	3.6	45	1.5	3	10	20	2	8
CY62147DV30LL	Industrial	2.2V	3.0	3.6	55	1.5	3	8	15	2	8
CY62147DV30L	Auto-E										25
CY62147DV30LL	Industrial	2.2V	3.0	3.6	70	1.5	3	8	15	2	8
CY62147DV30LL	Auto-A										8

Notes:

- NC pins are not internally connected on the die.
- DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.
- Pins H1, G2, and H6 in the VFBGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.3V to + V<sub>CC(MAX)</sub> + 0.3V

DC Voltage Applied to Outputs in High-Z State<sup>[6,7]</sup>..... -0.3V to V<sub>CC(MAX)</sub> + 0.3V

DC Input Voltage<sup>[6,7]</sup> ..... -0.3V to V<sub>CC(MAX)</sub> + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

**Operating Range**

Device	Range	Ambient Temperature [T <sub>A</sub> ] <sup>[9]</sup>	V <sub>CC</sub>
CY62147DV30L	Automotive-E	-40°C to +125°C	2.20V to 3.60V
CY62147DV30LL	Industrial	-40°C to +85°C	
	Automotive-A	-40°C to +85°C	

**Electrical Characteristics (Over the Operating Range)**

Parameter	Description	Test Conditions	-45			-55/-70			Unit
			Min.	Typ. <sup>[5]</sup>	Max.	Min.	Typ. <sup>[5]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA, V <sub>CC</sub> = 2.20V	2.0			2.0			V
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> = 2.70V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA, V <sub>CC</sub> = 2.20V			0.4			0.4	V
		I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.70V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3V	1.8		V <sub>CC</sub> + 0.3V	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3V	2.2		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	-0.3		0.6	V
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Ind'l	-1	+1	-1		+1	μA
			Auto-A <sup>[9]</sup>			-1		+1	μA
			Auto-E <sup>[9]</sup>			-4		+4	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	Ind'l	-1	+1	-1		+1	μA
			Auto-A <sup>[9]</sup>			-1		+1	μA
			Auto-E <sup>[9]</sup>			-4		+4	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , V <sub>CC</sub> = V <sub>CCmax</sub>		10	20		8	15	mA
		f = 1 MHz, I <sub>OUT</sub> = 0 mA CMOS levels		1.5	3		1.5	3	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.60V	Ind'l	LL	8			8	μA
			Auto-A <sup>[9]</sup>	LL				8	
			Auto-E <sup>[9]</sup>	L					
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V	Ind'l	LL	8			8	μA
			Auto-A <sup>[9]</sup>	LL				8	
			Auto-E <sup>[9]</sup>	L					

**Notes:**

- 6. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
- 7. V<sub>IH(max.)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- 8. Full device AC operation assumes a 100-μs ramp time from 0 to V<sub>CC(min)</sub> and 200-μs wait time after V<sub>CC</sub> stabilization.
- 9. Auto-A is available in -70 and Auto-E is available in -55.

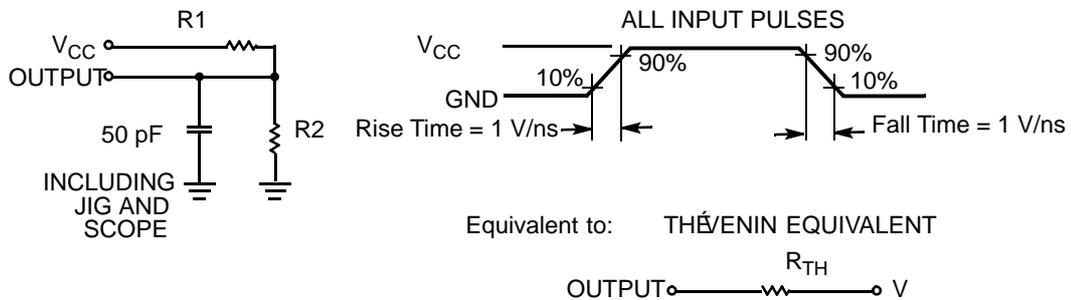
**Capacitance** (for all packages)<sup>[10]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Thermal Resistance**<sup>[10]</sup>

Parameter	Description	Test Conditions	VFBGA	TSOP II	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	72	75.13	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		8.86	8.95	°C/W

**AC Test Loads and Waveforms**<sup>[10]</sup>

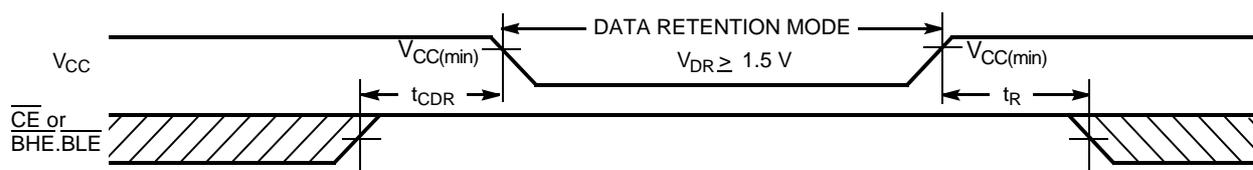


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	L (Auto-E)		15	μA
			LL (Ind'I/Auto-A)		6	
t <sub>CDR</sub> <sup>[10]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[12]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform**<sup>[13]</sup>



**Notes:**

- 10. Tested initially and after any design or process changes that may affect these parameters.
- 11. Test condition for the 45-ns part is a load capacitance of 30 pF.
- 12. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100 μs or stable at V<sub>CC(min.)</sub> ≥ 100 μs.
- 13. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

**Switching Characteristics** Over the Operating Range<sup>[14]</sup>

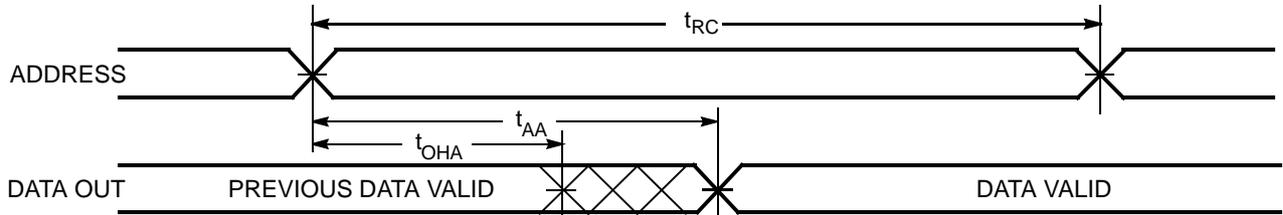
Parameter	Description	45 ns <sup>[11]</sup>		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	45		55		70		ns
t <sub>AA</sub>	Address to Data Valid		45		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		45		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[15]</sup>	5		5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[15, 16]</sup>		15		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[15]</sup>	10		10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[15, 16]</sup>		20		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		45		55		70	ns
t <sub>DBE</sub>	$\overline{BLE/BHE}$ LOW to Data Valid		45		55		70	ns
t <sub>LZBE</sub>	$\overline{BLE/BHE}$ LOW to Low Z <sup>[15]</sup>	10		10		10		ns
t <sub>HZBE</sub>	$\overline{BLE/BHE}$ HIGH to HIGH Z <sup>[15, 16]</sup>		15		20		25	ns
<b>Write Cycle<sup>[17]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	45		55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	40		40		60		ns
t <sub>AW</sub>	Address Set-up to Write End	40		40		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		40		45		ns
t <sub>BW</sub>	$\overline{BLE/BHE}$ LOW to Write End	40		40		60		ns
t <sub>SD</sub>	Data Set-up to Write End	25		25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[15, 16]</sup>		15		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[15]</sup>	10		10		10		ns

**Notes:**

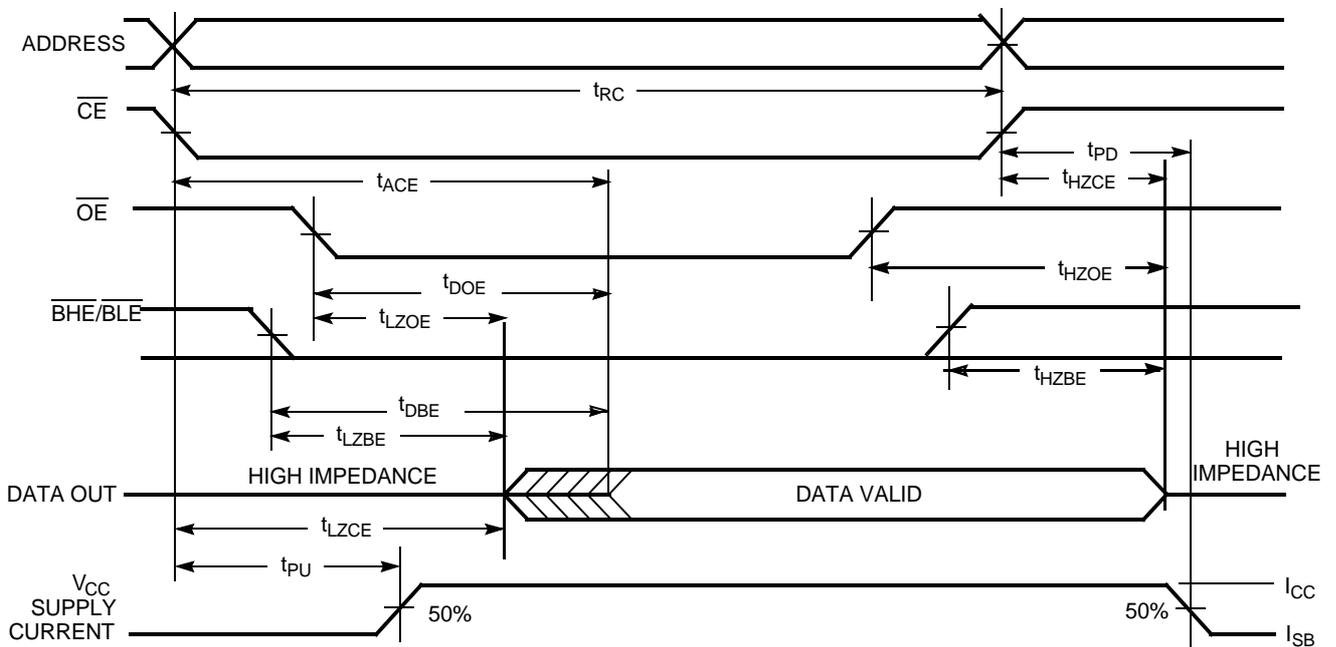
14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
15. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
16. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
17. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ , BHE and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

Read Cycle 1 (Address Transition Controlled)<sup>[18, 19]</sup>



Read Cycle No. 2 (OE Controlled)<sup>[19, 20]</sup>

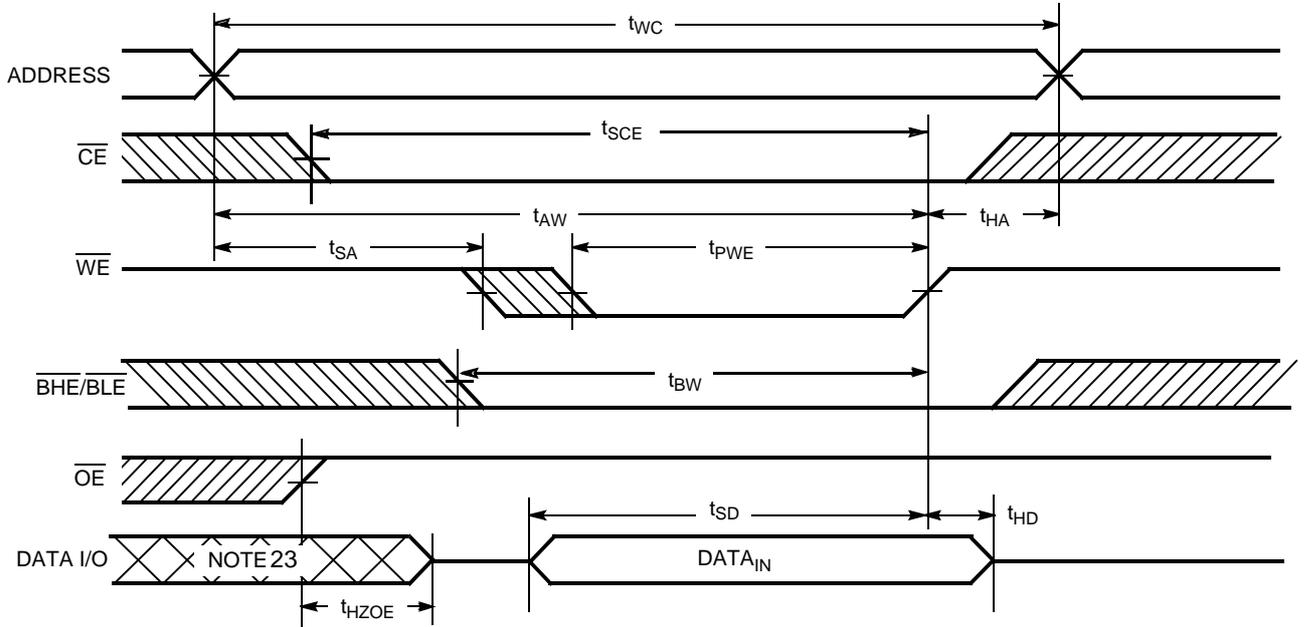


**Notes:**

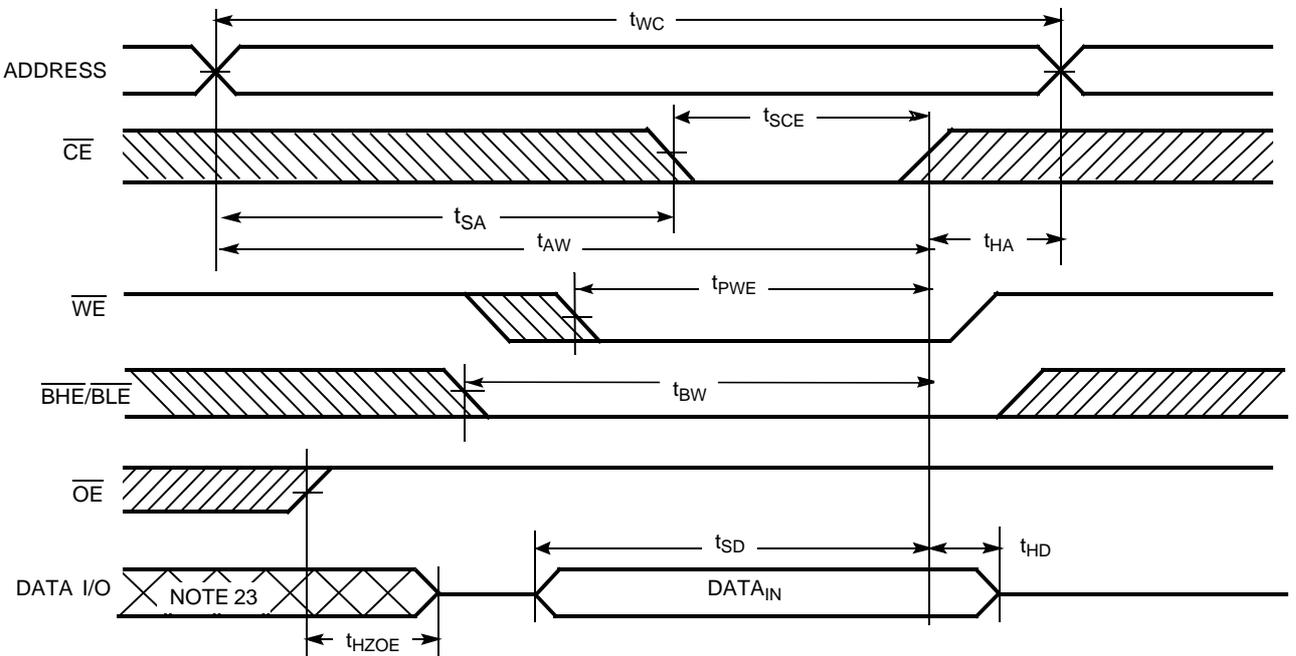
- 18. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
- 19.  $\overline{WE}$  is HIGH for read cycle.
- 20. Address valid prior to or coincident with  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[17, 21, 22]</sup>



Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[17, 21, 22]</sup>

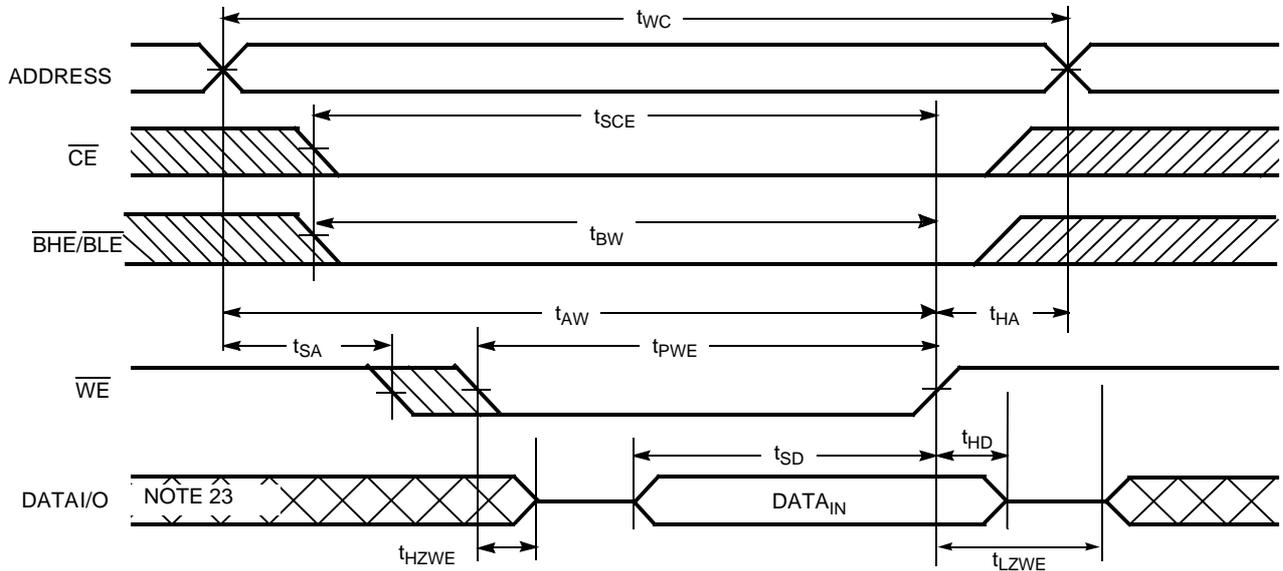


Notes:

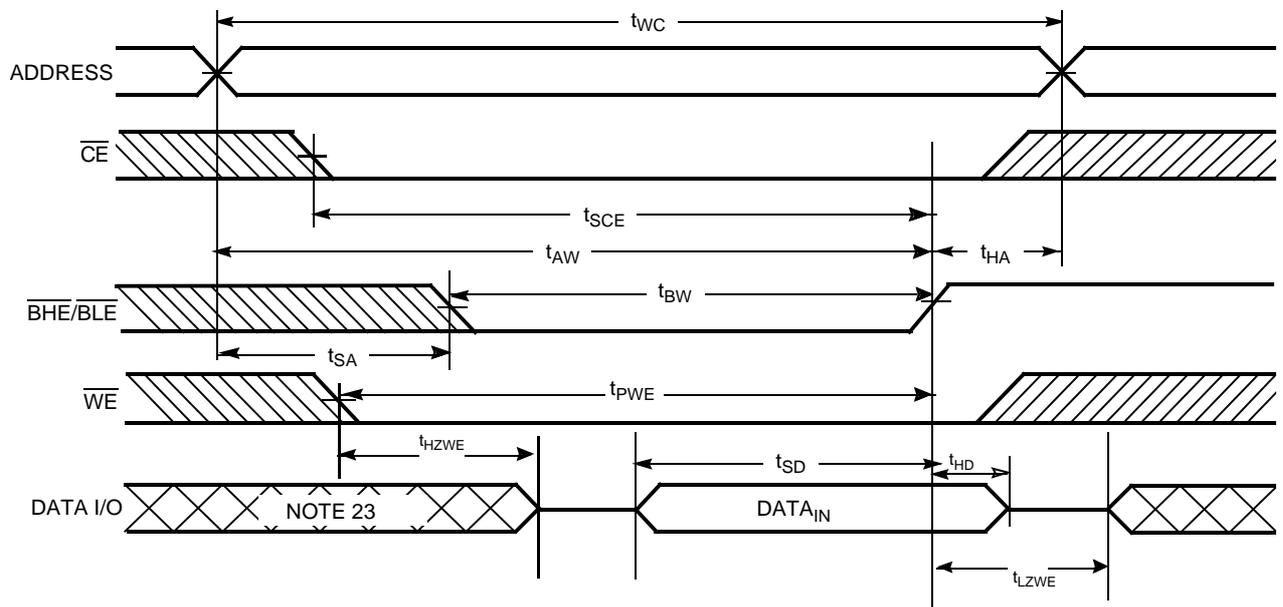
- 21. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 22. If CE goes HIGH simultaneously with  $WE = V_{IH}$ , the output remains in a high-impedance state.
- 23. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[22]</sup>



Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[22]</sup>



**Truth Table**

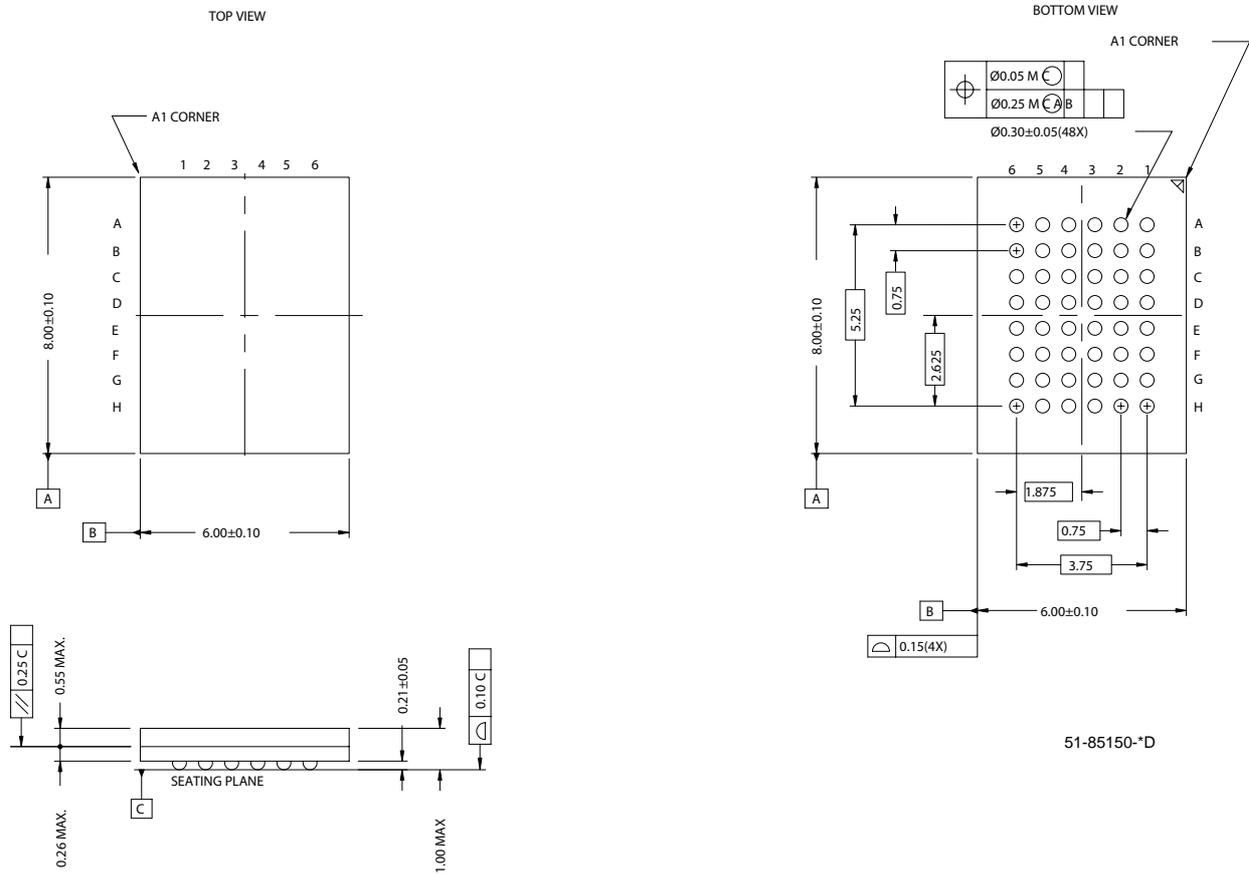
CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
L	H	L	L	L	Data Out (I/O <sub>0</sub> -I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	L	H	L	Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> ); I/O <sub>8</sub> -I/O <sub>15</sub> in High Z	Read	Active (I <sub>CC</sub> )
L	H	L	L	H	Data Out (I/O <sub>8</sub> -I/O <sub>15</sub> ); I/O <sub>0</sub> -I/O <sub>7</sub> in High Z	Read	Active (I <sub>CC</sub> )
L	H	H	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	L	H	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	L	X	L	L	Data In (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	L	X	H	L	Data In (I/O <sub>0</sub> -I/O <sub>7</sub> ); I/O <sub>8</sub> -I/O <sub>15</sub> in High Z	Write	Active (I <sub>CC</sub> )
L	L	X	L	H	Data In (I/O <sub>8</sub> -I/O <sub>15</sub> ); I/O <sub>0</sub> -I/O <sub>7</sub> in High Z	Write	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147DV30LL-45BVXI	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	Industrial
	CY62147DV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	
55	CY62147DV30LL-55BVI	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA	Industrial
	CY62147DV30LL-55BVXI		48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	
	CY62147DV30LL-55ZSXI	51-85087	44-pin TSOP II (Pb-free)	Automotive-E
	CY62147DV30L-55BVXE	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	
	CY62147DV30L-55ZSXE	51-85087	44-pin TSOP II (Pb-free)	
70	CY62147DV30LL-70BVI	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA	Industrial
	CY62147DV30LL-70BVXA		48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	Automotive-A

Package Diagram

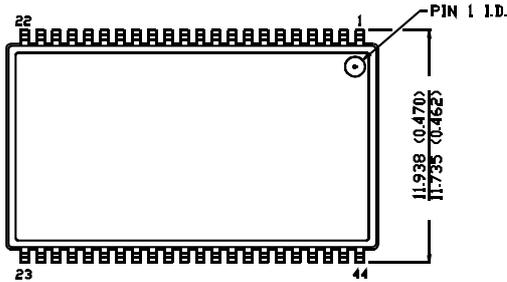
48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



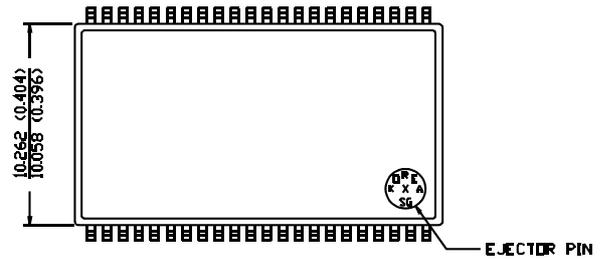
Package Diagram (continued)

44-Pin TSOP II (51-85087)

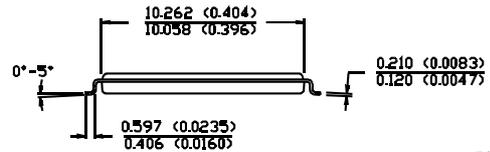
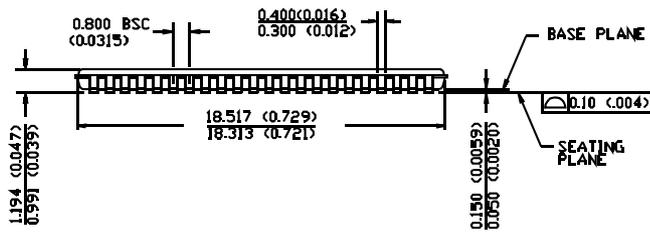
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-\*A

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**Document History Page**

Document Title:CY62147DV30 MoBL <sup>®</sup> 4-Mbit (256K x 16) Static RAM Document Number: 38-05340				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	127481	06/17/03	HRT	New Data Sheet
*A	131010	01/23/04	CBD	Changed from Advance to Preliminary
*B	213252	See ECN	AJU	Changed from Preliminary to Final Added 70 ns speed bin Modified footnote 7 to include ramp time and wait time Modified input and output capacitance values to 10 pF Modified Thermal Resistance values on page 4 Added "Byte power-down feature" in the features section Modified Ordering Information for Pb-free parts
*C	257349	See ECN	PCI	Modified ordering information for 70-ns Speed Bin
*D	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #10 on page #4 Added Pb-free package ordering information on page # 9 Changed 44-lead TSOP-II package name on page 11 from Z44 to ZS44 Standardized Icc values across 'L' and 'LL' bins
*E	330365	See ECN	AJU	Added Automotive product information
*F	498575	See ECN	NXR	Added Automotive-A range Added note# 9 on page# 3 Updated ordering information table