AT27C512R

T-46-13-29

Features

- Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC and OTP PLCC
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with AT27C512

512K (64K x 8) UV Erasable CMOS EPROM

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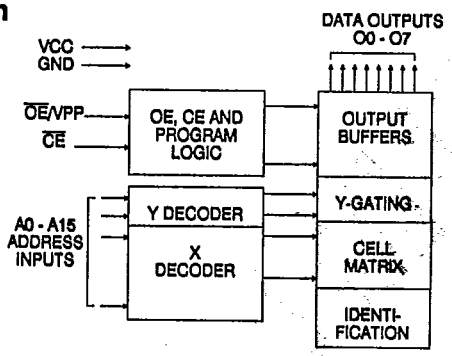
Preliminary

Block Diagram



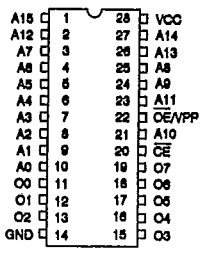
Description

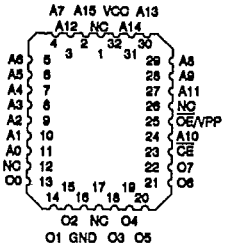
The ATMEL 27C512R chip is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

The AT27C512R meets or exceeds all specifications for the AT27C512. ATMEL's 1.2 micron scaled CMOS technology additionally provides lower active power consumption, and significantly faster programming. Power consumption is typically only 8mA in Active Mode and less than 10µA in Standby.

Pin Configurations

PIN NAMES	
A0 - A15	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable
NC	No Connect





Note: PLCC package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C512R comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), and 32-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

ATMEL's 27C512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X[1]	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Rapid Program[2]	V_{IL}	V_{PP}	Ai	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Product Identification[4]	V_{IL}	V_{IL}	A9 = V_H[3] A0 = V_{IH} or V_{IL} A1-A15 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to Programming Characteristics. 3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -2.0V to +7.0V[1]
Voltage on A9 with Respect to Ground ..... -2.0V to +14.0V[1]
V_{PP} Supply Voltage with Respect to Ground ..... -2.0V to +14.0V[1]
Integrated UV Erase Dose ..... 7258 W•sec/cm^2

Notes: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Erasure Characteristics

The entire memory array of the AT27C512R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C512R			
		-12	-15	-20	-25
Operating Temperature (case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC}+0.1V			10	µA
I_{SB}	V_{CC}[1] Standby Current	I_{SB1} (CMOS)	Com.		100	µA
		$\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0V	Ind.,Mil.		200	µA
		I_{SB2} (TTL)	Com.		2	mA
		$\overline{CE}$ = 2.0 to V_{CC}+1.0V	Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V

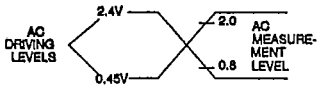
Note: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation

				AT27C512R							
				-12		-15		-20		-25	
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC}[4]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}	Com.		120		150		200		250	ns
			Ind.,Mil.		120		150		200		250	ns
t_{CE}[3]	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}			120		150		200		250	ns
t_{OE}[3,4]	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}			50		60		75		100	ns
t_{DF}[2,5]	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			45		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}			0		0		0		0	ns

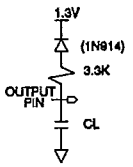
Notes: 2,3,4, and 5 - see AC Waveforms for Read Operation.

Input Test Waveforms and Measurement Levels



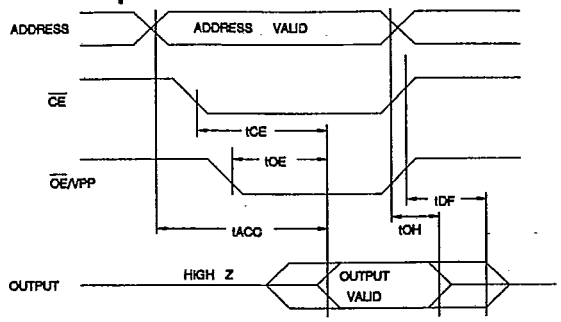
t_R, t_F < 20ns (10% to 90%)

Output Test Load



Note: C_L = 100pF including jig capacitance.

A.C. Waveforms for Read Operation[1]

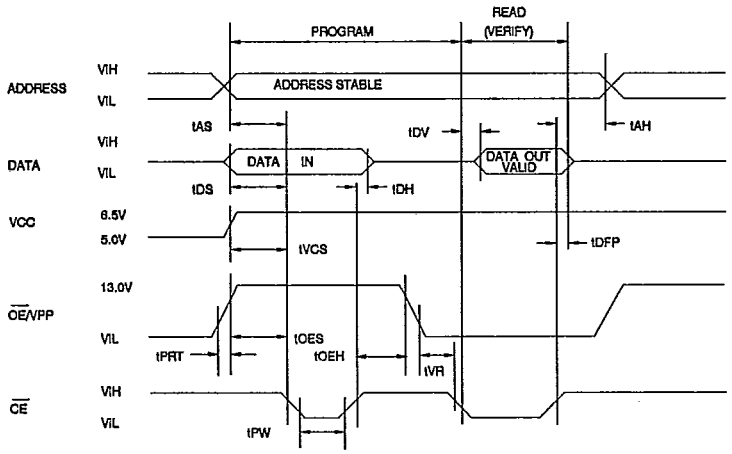


Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Pin Capacitance(f = 1MHz T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V
Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.				

Programming Waveforms[1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL} = 2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH} = -400µA$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%)	20ns
Input Pulse Levels	0.45V to 2.4V
Input Timing Reference Level	0.8V to 2.0V
Output Timing Reference Level	0.8V to 2.0V

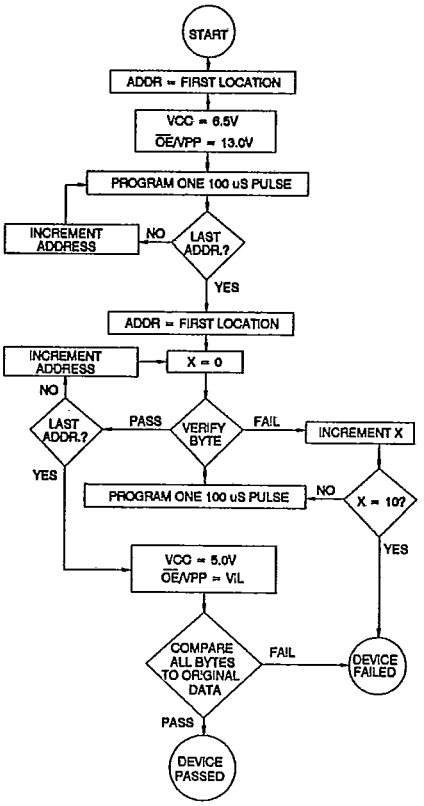
Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven - see timing diagram.
3. Program Pulse width tolerance is 100µs ± 5%.

ATMEL's 27C512R Integrated Product Identification Code:

Codes	Pins	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer		0	0	0	0	1	1	1	1	0	1E
Device Type		1	0	0	0	0	1	1	0	1	0D

Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
120	20	0.1	AT27C512R-12DC AT27C512R-12LC	28DW6 32LW	Commercial (0°C to 70°C)
120	25	0.2	AT27C512R-12DI AT27C512R-12LI	28DW6 32LW	Industrial (-40°C to 85°C)
			AT27C512R-12DM AT27C512R-12LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512R-12DM/883 AT27C512R-12LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	20	0.1	AT27C512R-15DC AT27C512R-15LC AT27C512R-15PC AT27C512R-15JC AT27C512R-15TC	28DW6 32LW 28P6 32J 28T	Commercial (0°C to 70°C)
150	25	0.2	AT27C512R-15DI AT27C512R-15LI AT27C512R-15PI AT27C512R-15JI AT27C512R-15TI	28DW6 32LW 28P6 32J 28T	Industrial (-40°C to 85°C)
			AT27C512R-15DM AT27C512R-15LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512R-15DM/883 AT27C512R-15LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C512R-20DC AT27C512R-20LC AT27C512R-20PC AT27C512R-20JC AT27C512R-20TC	28DW6 32LW 28P6 32J 28T	Commercial (0°C to 70°C)
200	25	0.2	AT27C512R-20DI AT27C512R-20LI AT27C512R-20PI AT27C512R-20JI AT27C512R-20TI	28DW6 32LW 28P6 32J 28T	Industrial (-40°C to 85°C)
			AT27C512R-20DM AT27C512R-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512R-20DM/883 AT27C512R-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	20	0.1	AT27C512R-25DC AT27C512R-25LC AT27C512R-25PC AT27C512R-25JC AT27C512R-25TC	28DW6 32LW 28P6 32J 28T	Commercial (0°C to 70°C)
250	25	0.2	AT27C512R-25DI AT27C512R-25LI AT27C512R-25PI AT27C512R-25JI AT27C512R-25TI	28DW6 32LW 28P6 32J 28T	Industrial (-40°C to 85°C)
			AT27C512R-25DM AT27C512R-25LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512R-25DM/883 AT27C512R-25LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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Package Type	
28DW6	28 Lead, 0.6", Windowed Cerdip
32J	32 Lead, Plastic J-Lead Chip Carrier
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier
28P6	28 Lead, 0.6" Wide, Plastic Dual-In-Line
28T	28 Lead, Wide Footprint, Plastic Gull Wing SOIC