Supertex inc.

AN04

Gate Protected

Preliminary

8 Channel MOSFET Array
Monolithic N-Channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = 100V Max	I_{DSS}** @ V_{DS} = 250V Max	Order Number / Package		
					18-Lead Plastic DIP	Plastic SOW-20*	Die†
160V	350Ω	25mA	1nA	—	AN0416NA	AN0416WG	AN0416ND
200V	300Ω	25mA	—	—	AN0420NA	—	AN0420ND
300V	300Ω	25mA	—	—	AN0430NA	—	AN0430ND
320V	350Ω	25mA	—	1nA	AN0432NA	AN0432WG	AN0432ND
400V	350Ω	25mA	—	—	AN0440NA	AN0440WG	AN0440ND

* Same as SO-20 with 300 mil wide body.
** Average current per channel, measured with all eight channels connected in parallel.
† MIL visual screening available

Features

- ☐ ESD Gate Protection
- ☐ Low drain to source leakage for AN0416 and AN0432
- ☐ 160-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Free from secondary breakdown

Applications

- ☐ High impedance/low leakage measurements for Bare Board Testers
- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

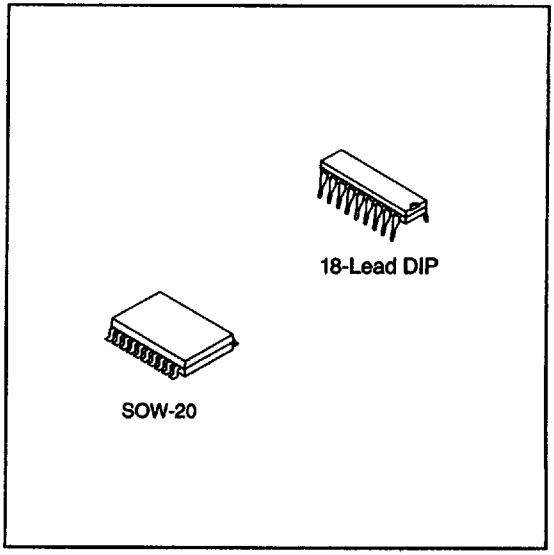
* Distance of 1.6 mm from case for 10 seconds.

General Description

The Supertex AN04 series of high voltage arrays is a ruggedized ESD gate protected version of the Supertex AN01 series. These multichannel arrays meet the EIA ESD standard of 2000V, 100pF capacitor in series with a 1.5KΩ resistor. They are designed to provide interface between CMOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AN0416 and AN0432 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for automatic test equipment.

Package Options



Thermal Characteristics

Package	I_D(continuous)*	I_D(pulsed)*	Power Dissipation @T_C=25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 lead plastic	30mA	75mA	1.5W	135	83	30mA	75mA
SOW - 20	30mA	75mA	1.4W	110	89	30mA	75mA

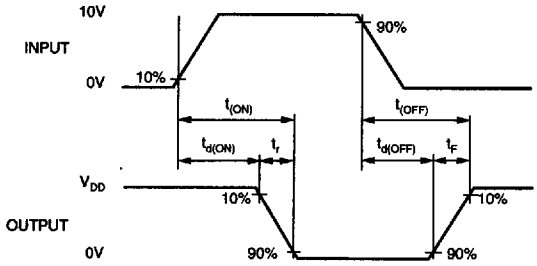
* I_D (continuous) is by max rated T_j

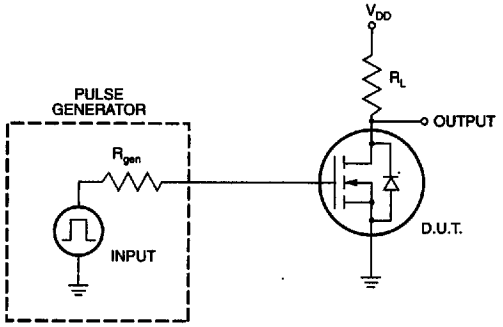
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AN0416	160			V	I_D = 100µA, V_{GS}= 0V
		AN0420	200				
		AN0430	300				
		AN0432	320				
		AN0440	400				
$V_{GS(th)}$	Gate Threshold Voltage		2		5	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5		mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage	AN0420 AN0430 AN0440			10	nA	V_{GS} = ±20V, V_{DS} = 0V (3)
		AN0416 AN0432			1	nA	V_{GS} = ±20V, V_{DS} = 0V (3)
I_{DSS}	Zero Gate Voltage Drain Current	AN0420			1	uA	V_{GS} = 0, V_{DS} = Max Rating (3)
		AN0430 AN0440			1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A =125°C (3)
		AN0416			1	nA	V_{GS} = 0V, V_{DS} = 100V (3)
					2	µA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A=125°C (3)
		AN0432			1	nA	V_{GS} = 0V, V_{DS} = 250V (3)
					2	µA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C(3)
$I_{D(ON)}$	ON-State Drain Current		25			mA	V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source	AN0420 AN0430			300	Ω	V_{GS} = 10V, I_D = 10mA
	ON-State Resistance	AN0416 AN0432 AN0440			350	Ω	V_{GS} = 10V, I_D = 10mA
$\Delta R_{DS(ON)}$	Charge in $R_{DS(ON)}$ with Temperature			0.8		%/°C	V_{GS} = 10V, I_D = 10mA
G_{FS}	Forward Transconductance		4.0	8.0		m℧	ΔV_{GS} = 1V, I_D =10mA
C_{ISS}	Input Capacitance			8.0	12.0	pF	V_{DS} = 25V, V_{GS} = 0V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			5.0	8.0		
C_{RSS}	Reverse Transfer Capacitance			1.3	2.4		
$t_{d(ON)}$	Turn-ON Delay Time			5.0		ns	V_{DD} = 25V, I_D = 10mA, R_{GEN} = 25Ω
t_r	Rise Time			5.0			
$t_{d(OFF)}$	Turn-OFF Delay Time			8.0			
t_f	Fall Time			5.0			
V_{SD}	Diode Forward Voltage Drop				1.3	V	V_{GS} = 0V, I_{SD} = 50mA

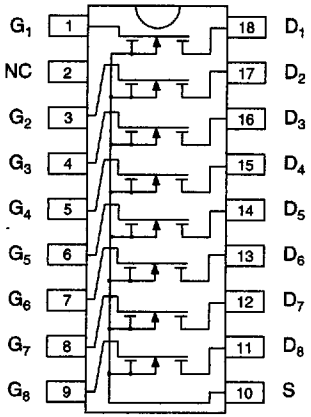
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.
3. Average current per channel, measured with all 8 channels connected in parallel.

Switching Waveforms and Test Circuit

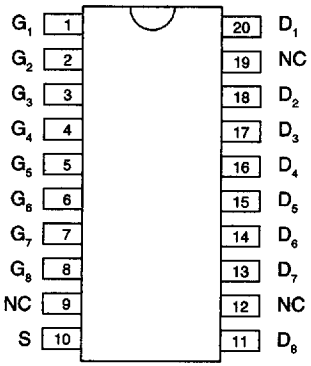




Pin Configuration and Schematic



top view
18-pin DIP



top view
SOW - 20