PRODUCT SPECIFICATION

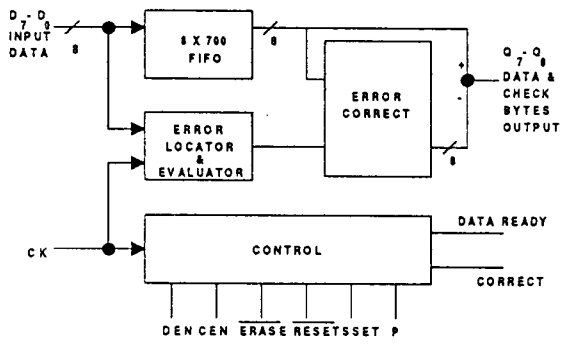
AHA4310
AHA4510
AHA4810
AHA4010

HIGH SPEED, PROGRAMMABLE, REED-SOLOMON ECC CODECS

1.0 INTRODUCTION

The Advanced Hardware Architectures AHA4310 and AHA4510, AHA4810, and AHA4010 are members of the AHA PerFEC™ family of very high performance, single-chip, Reed-Solomon Forward Error Correction (FEC) Encoder/Decoders. These device use a single phase clock to synchronize all chip functions and do not require an external microprocessor or data buffer. They are very easy to use and yet provide a very sophisticated and powerful means of detecting and correcting errors in data transfer systems. The AHA4310, AHA4510, AHA4810, and the AHA4010 use patented, low power, dual-metal CMOS technology and design techniques to achieve the highest available performance and density.

4x10 Block Diagram



FEATURES AND BENEFITS

VERY HIGH PERFORMANCE
- On-the-fly Error/Erasure Correction
- Programmable to correct t=1-10 errors
- Operate as either encoder or decoder
- Low power consumption (550 mW max.)
- Single-phase master clock

HIGH CHANNEL UTILIZATION

EXCELLENT BURST ERROR CORRECTING CODE

CORRECTION ABILITY
- AHA4310 -- up to 6 bytes/block @ 15 MHz
- AHA4510 -- up to 10 bytes/block @ 15 MHz
- AHA4810 -- up to 16 bytes/block @ 10 MHz
- AHA4010 -- up to 20 bytes/block @ 10 MHz
- Block "uncorrectable" flag provided
- Correction time is constant

FULL STAND ALONE OPERATION
- No microprocessor required
- No external buffer required

FLEXIBLE, USER PROGRAMMABLE OPERATION
- Variable block length (from 10t+15 to 255)
- Variable correction threshold
- Variable number of check bytes

CAN OPERATE ON MIXED BLOCK LENGTHS
- Block lengths may be changed dynamically

ABILITY TO OUTPUT CORRECTION STATUS BYTES
- Error totals, type, and correction status flag

68 PIN PLCC PACKAGE (STANDARD)

ALL AHA4x10 DEVICES ARE PIN COMPATIBLE

2.0 DC ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	*Parameter*	*Min.*	*Max.*	*Units*
Vdd	Supply Voltage	-0.3	5.5	V
Vi	Voltage at Digital Inputs	-0.3	Vdd+0.3	V
Vo	Voltage at Digital Outputs	-0.3	Vdd+0.3	V
Ii	Current into Digital Inputs	-10.0	10.0	mA
Io	Current into Digital Outputs	-10.0	10.0	mA
Tst	Storage Temperature	-65	150	Deg. C

Recommended Operating Conditions

Symbol	*Parameter*	*Min.*	*Max.*	*Units*	*Test Conditions*
Vdd	Supply Voltage	4.5	5.5	V	
Top	Operating Temperature	0	+70	Deg. C	Commercial Grade Devices
Top	Operating Temperature	-55	+125	Deg. C	Military Grade Devices
Vi	Input Voltage	0	Vdd	V	
Idd	Supply Current		100	mA	Outputs Unloaded

DC Electrical Characteristics

Symbol	*Parameter*	*Min.*	*Max.*	*Units*	*Test Conditions*
Vih	Input High Voltage	2.0	Vdd	V	
Vil	Input Low Voltage	Vss	0.8	V	
Iil	Input Leakage	-10.0	10.0	uA	
Voh	Output High Voltage	2.4	Vdd	V	Ioh = 0.4 mA
Vol	Output Low Voltage	Vss	0.4	V	Iol = -3.2 mA
Ioh	Output High Current (Source Current)		0.4	mA	Voh = 2.4 V
Iol	Output Low Current (Sink Current)		-3.2	mA	Vol = 0.4 V
P	Power Dissipation		550	mW	Outputs Loaded
Ioz	High Impedance Leakage		10	uA	

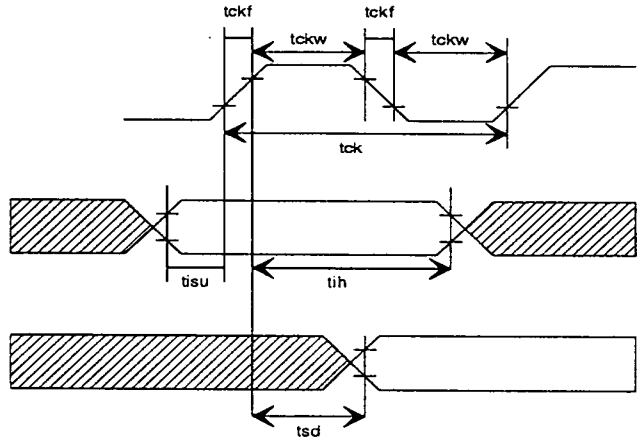
3.0 AC ELECTRICAL SPECIFICATIONS

AC Electrical Specifications

Symbol	*Parameter*	*Min.*	*Max.*	*Units*	*Test Conditions*
tck	Clock Cycle Time	100		ns	Note 1
tckr	Clock Rise Time		3	ns	Note 2
tckf	Clock Fall Time		3	ns	Note 3
tckw	Clock Pulse Width	44		ns	Note 1,4
tisu	Data/Control In Set Up	10		ns	Note 5
tih	Data/Control In Hold	0		ns	Note 6
tsd	Data/Control Out Delay		25	ns	CL=50pF Note 7

Notes:

1. Measures from valid Vil to valid Vil.
2. Measured from valid Vil to valid Vih.
3. Measured from valid Vih to valid Vil.
4. Measured from valid Vih to valid Vih.
5. Measured from valid Vil or Vih to invalid Vil (rising clock edge).
6. Measured from valid Vih (rising clock edge) to valid Vih or Vil.
7. Measured from valid Vih (rising clock edge) to valid Voh or Vol.



4.0 INPUT/OUTPUT CIRCUIT SCHEMATICS

Fig. 4a Input circuit Schematic

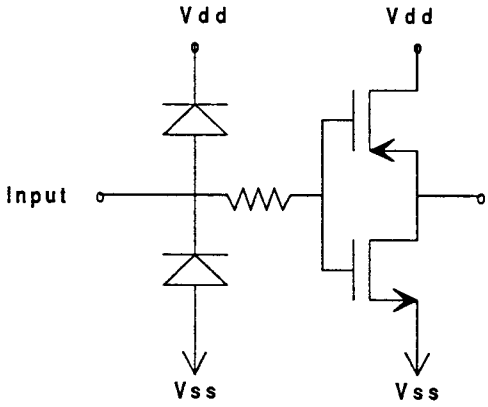
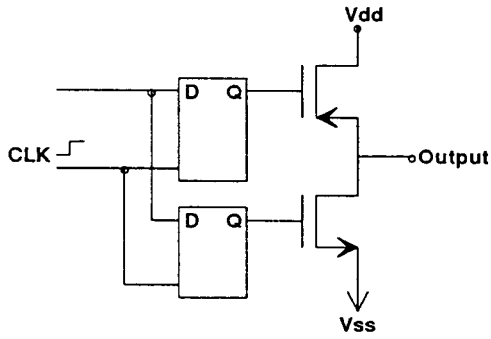


Fig. 4b Output circuit schematic



All inputs are protected against static discharge. All outputs are latched, synchronous with the rising edge of CK.

5.0 SIGNAL DESCRIPTIONS AND PINOUT INFORMATION

Parameter Definition

CEN (Pin 2) — Correction Enable. Assertive - HIGH. When this input is asserted, the device performs corrections on the message block. When CEN is LOW the device does not perform corrections but continues to report status if initialized to do so.

DEN (Pin 1) — Data Enable. Assertive - HIGH. This input is used to signal the difference between data bytes and check bytes in both the encoder and the decoder

CK (Pin 20) — Master Clock. All inputs and outputs are synchronized by the rising edge of CK.

ERASE — Erasure Indicator. Assertive LOW. For the decoder, this input is used to flag erroneous input bytes. For the encoder, *ERASE* is used to mark the position of the "dummy" fill bytes to be "corrected" and used for check byte insertion.

P4-P0 or P3-P0 — Parity Select Bus. This determines the value of (P) which is the maximum number of check bytes that the device will use in correction before flagging the message block as uncorrectable. Normally set to 2t. P4 is the most significant for the AHA4810 and AHA4010. P3 is the most significant for the AHA4310 and AHA4510. Note: P4 is NC for the AHA4310 and AHA4510.
Pins: (7-P4, 4-P3, 5-P2, 6-P1, 11-P0 Note: Pin 7 is NC on the AHA4510)

RESET — System Reset. Assertive - LOW. Reset timing(Pin 12) is critical to the initialization of the device.

SSET (Pin 47) — Set Status Reporting. Assertive - HIGH. If this signal is HIGH during reset then the decoder will be programmed to output two status bytes with each message block. SSET must not be set HIGH when using the device as an encoder or check bytes will be overwritten by status bytes.

CONTROL OUTPUTS

CORRECT (Pin 21) — Message Block Correct. Assertive HIGH. When P=2t, this output indicates the status of the decoded message block (HIGH indicates Block Correct, LOW indicates too many errors to correct). When P <> 2t then the meaning of this decoder output is defined by the table in Section 9.3.

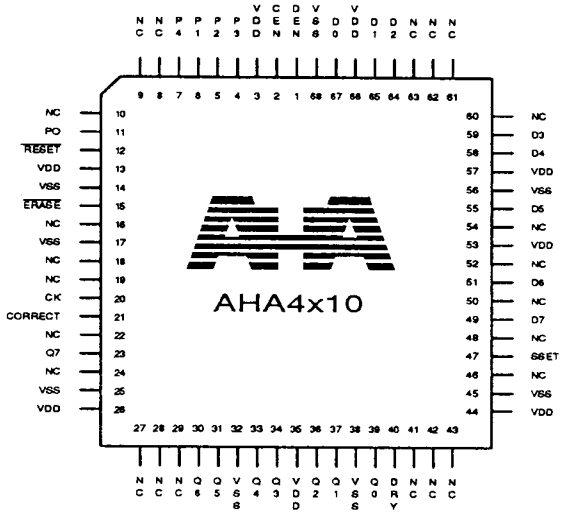
DRY (Pin 40) — Data Ready. Assertive HIGH. This output (from either the encoder or the decoder) is held HIGH for data bytes and held LOW for check bytes.

DATA BUS INPUTS/OUTPUTS

D7-D0 — Data Input Bus. Bit 7 is the most significant.
Pins: (67-D0, 65-D1, 64-D2, 59-D3, 58-D4, 55-D5, 51-D6, 49-D7)

Q7-Q0 — Data Output Bus. Bit 7 is the most significant.
Pins: (39-Q0, 37-Q1, 36-Q2, 34-Q3, 33-Q4, 31-Q5, 30-Q6, 23-Q7)

6.0 CONNECTION DIAGRAM



7.0 FUNCTIONAL DESCRIPTION

The AHA4310, AHA4510, AHA4810, and AHA4010 Reed-Solomon codecs (coder/decoder) are members of the AHA PerFEC™ family of high speed forward error correction (FEC) devices. These are single chip, two-layer metal, CMOS devices, and each can operate as a stand alone encoder or decoder with no external buffer or microprocessor required. The delay required for each block of a given length to pass through these devices is fixed, and does not vary with the location or the number of errors received. This delay (or latency) is 2N + 10t + 33 for the AHA4310 and AHA4510 and is 2N + 10t + 34 for the AHA4810 and AHA4010, where N is the block length and t is the number of correctable errors per block.

In their most powerful mode, where incorrect bytes are flagged by external circuitry, these devices can correct as many as 2t bytes in error in a message block as long as 255 bytes, where 2t equals the number of check bytes added to the message block by the Reed-Solomon encoder. If no error detection is available, these devices can detect and correct up to t bytes in error, in a block as long as 255 bytes.

The Reed-Solomon codes used by these devices and by other members of the AHA PerFEC™ family, are among the most powerful binary EDAC (Error Detection and Correction) codes known. Compared with other codes, RS codes require relatively few "overhead" parity check bytes to be added to the data stream to achieve a high degree of error detection and correction. Since these devices deal with bytes (or symbols) rather than with individual bits, when a byte is in error it does not matter how many bits within the byte are corrupted; it is counted as one error.

The Reed-Solomon code is defined over the finite field GF(2^8). The field defining primitive polynomial is $p(x) = x^8 + x^7 + x^2 + x + x^0$ and the generator polynomial, dependent on the variable t, is given by:

$$G(x) = \prod_{i=120}^{119+2t} (x - \alpha^i)$$

where $t \in \{1,1.5,2,2.5,...10\}$ for the AHA4010.

These codecs can correct bytes under two different conditions. In one condition, the erroneous byte is in a known position within the block; the position may have been flagged by a bad parity bit, a signal dropout detector, or any external error detection method. The erroneous byte position is indicated by the *ERASE* input on the device. The erroneous bytes whose positions have been identified by external circuitry, (via the *ERASE* input) are termed "erasures". In many cases however, there is no external method for detecting erroneous bytes; these bytes are termed "errors". Errors are defined as erroneous bytes whose location are unknown (ie. there was no corresponding *ERASE* input for these bytes.)

Correcting "erasures" takes only half as much of the correction capability of the RS EDAC code as it takes to correct "errors", since the position information is already known for "erasures". The correction ability of the code is bounded as:

$2t \geq \#\text{ erasures} + 2(\#\text{ errors})$

Valid block lengths (N) are defined by the relationship:

$10t + 15 \leq N \leq 255.$

A complete message block can therefore range from a minimum of 25 bytes to a maximum of 255 bytes (including the check bytes.) There must be at least 2 check bytes per block, therefore a minimum message block will consist of 23 data bytes and 2 check bytes.

For these devices there can be no more than 2t check bytes in a block. The maximum useful data block is (255-2t) data bytes. It would be possible to increase the number of data bytes to 253, with only 2 check bytes, but this would severely limit the correction capability.

These devices may be used with intermixed message block lengths if proper guidelines are followed. There may only be two different block lengths understood by the device at one time. After the first block of greater length has passed through the device, then the delay required for each succeeding message block to pass through will be that of the greater block length. Also, a shorter length block may not directly follow another shorter length block, without a greater length block intervening. However, greater length blocks may follow each other. This is discussed in more detail in Section 8.4.

7.1 DATA FLOW

For the following discussion, refer to the block diagram on page 1.

Data enters the device, via the D7-D0 inputs, on the rising edge of CK. This data then takes two separate paths: path 1 into the FIFO, and path 2 into the Error Locator and Evaluator.

The purpose of the FIFO is to hold the incoming message data block (or blocks) which will have error correction applied (if necessary) by the Error Correct circuitry, before being output.

The purpose of the Error Locator and Evaluator is to generate the polynomials used to find and correct any erroneous bytes. These polynomials are then transferred to the Error Correction circuit where the error equations are solved. The error information is then shifted out, in step with the corresponding data contained in the FIFO. The errors are then subtracted from the original message to leave corrected data, which is output on the Q7-Q0 bus on the rising edge of CK.

The control circuitry takes care of the timing required for initialization and coordination of the various chip functions. It also generates the external timing and control signals for determining the difference between data and check bytes, as well as signalling whether the outgoing data block is correct. This circuitry also monitors the *ERASE* input and tags any erasures.

7.2 CORRECTION PARAMETERS

Parameter Definition

2t	The total number of check bytes used (for both detection and correction). Since these devices are programmable, t may vary from 1 to 10 in increments of 1/2 for the AHA4010. For the AHA4510, t may vary from 1 to 5 in increments of 1/2. Thus, 2t for the AHA4510 may be any integral number from 2 to 10.
N	The total number of bytes in one message block including data and check bytes. N must be at least 10t + 15 and no more than 255.
K	The number of data bytes in one message block. (K = N - 2t)

P The threshold for determining uncorrectability of a data block, and the number of check bytes allocated for correction-only purposes (and not for detection). When the number of errors exceeds the threshold set by P, then the block is flagged uncorrectable and the CORRECT output pin goes LOW. If P is set properly, it is possible to have > t errors and be guaranteed to correct the error. P only affects the CORRECT output pin.

e The number of "errors" in a received message block. An error is defined as an erroneous byte whose correct value and position within the message block are both unknown.

E The number of "erasures" in a received message block. An erasure is defined as an erroneous byte whose position is known within the message block. When an erroneous byte is detected by external circuitry, the *ERASE* input pin is brought LOW to mark the position.

e+(E/2) A measure of the burden of correction being placed on the capabilities of the device, for that message block.

8.0 BASIC OPERATION

The AHA4010 and the AHA4510 are designed such that they perform the same exact operations whether they are being used as an encoder or as a decoder. When erasures are flagged (by the *ERASE* input) they are corrected (if possible). For the decoder this means that any erasures (bytes known to be corrupted during transmission) are corrected back to the original data bytes. For the encoder this means that "dummy" check bytes (appended by the user and flagged by the *ERASE* input) are "corrected" to become real check bytes, ready for transmission. So, in actuality, these devices are decoders that can also perform as encoders due to the mathematical properties of RS codes and the way in which check bytes are computed.

8.1 INITIALIZATION

Certain architectural and mathematical properties of these devices are not hardwired and must be set during the initialization control sequence. These properties include:

1. The overall message block length (N)
2. The number of data bytes (K)
3. The total number of check bytes (2t)
4. The number of check bytes allocated for correction-only (P)
5. Whether the first two check byte output positions are used for status bytes or check bytes (SSET)

These devices (used as an encoder or decoder) must be initialized before normal operation can begin. There are two distinct phases of the initialization process. In phase-one, the values of P and SSET are initialized. In phase-two, the first message block through the device is used to set the values of N, K, and 2t.

The phase-one sequence consists of at least 4 clocks in which *RESET* is held LOW followed by at least 2 clocks during which *RESET* is held HIGH. *RESET* must then remain HIGH for all subsequent operations or an unwanted initialization control sequence will ensue. The desired values of SSET and P0-P4 (or P0-P3 for the AHA4510) must be maintained as shown in Fig. 8A. DEN must be held LOW during the entire 6 clock sequence or unintended processing of spurious messages may occur.

The rising edge of DEN at the end of the phase-one initialization sequence marks the beginning of the first message block which is phase-two of the initialization process. During the passage of this first message block, DEN has the role of initializing the parameters of N, K, and 2t. DEN has a different function on all subsequent blocks until an initialization sequence is begun once again. As the first message block passes through the device, DEN is held high for K clocks and then LOW for 2t clocks. DEN going high again marks the first byte of the second block and implies the end of the phase-two initialization sequence. DEN has thus defined 2t, K, and N for all subsequent blocks until another initialization sequence is performed or until a second message block length is defined (see Section 8.4).

CEN must remain high throughout the entire phase-two initialization block for initialization to occur properly. However, CEN is not examined during the phase one initialization sequence.

Fig. 8a Initialization control sequence timing.

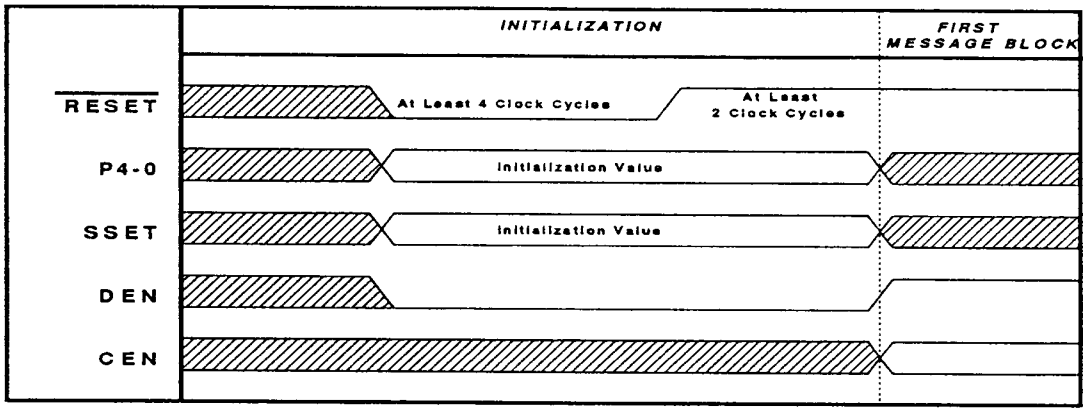
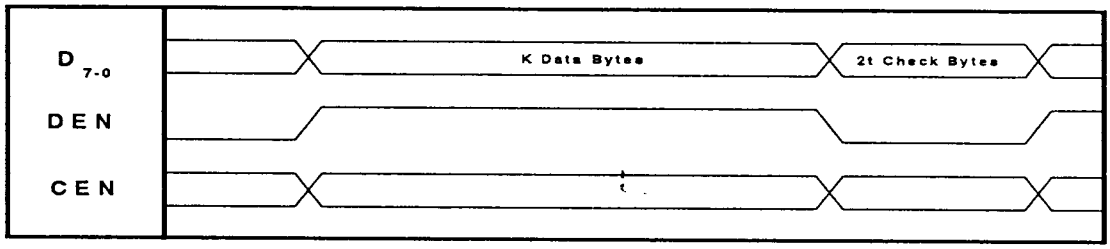


Fig. 8b Message block input timing.



8.2 BASIC INPUT OPERATION FOR ENCODING OR DECODING

After the first message block has passed through the encoder or decoder (and therefore initialization is complete), all subsequent message blocks will follow the timing pattern shown in Fig. 8b. DEN defines the number of data and check bytes for all subsequent message blocks and must remain HIGH when the data bytes are being input and LOW when the check bytes are input. If the number of data bytes defined by the DEN timing differs from the most recent message block, then a redefinition of message block length parameters is occurring. This is described further in section 8.4.

8.3 CORRECTION SUPPRESSION

CEN must remain HIGH throughout the entire message block for correction computations to continue, for both encoding and decoding. If CEN remains LOW throughout an entire message block, then that block will not be corrected as it passes through. However, errors will still be detected and, if the device is currently set to output status bytes, then the number of errors (E and e+E), along with the CA flag, will be output. CEN must transition on LOW-to-HIGH transitions of DEN only. If CEN transitions during a message block, the output is indeterminate. This timing is illustrated in Fig. 8b.

The delay or latency for one message block to pass through the AHA4010 for a maximum length block and t=10 is: (2N + 10t + 34) = 644 clock cycles.

The delay or latency for one message block to pass through the AHA4510 for a maximum length block and t=5 is: (2N + 10t + 33) = 593 clock cycles.

8.4 INTERMIXING MESSAGE BLOCK LENGTHS

The encoder or decoder can operate on up to two different message block lengths at one time. The duration of DEN dynamically determines the values of K and N for each message block. After initialization, if the timing of DEN changes, then the device will acquire a second definition of K and N corresponding to a second message block length. However, 2t remains the same for all message blocks after initialization. The DEN waveform for all blocks must conform to the DEN timing defined in Fig. 8b.

The message block latency, or delay through the device, will be equal to that of the longest of the two defined block lengths.

The device can reliably operate on only two sets of message block length parameters. Introducing a third DEN waveform timing pattern, and therefore a third set of K and N values, is an operational error and results in indeterminate operation of the device.

When the device has acquired two sets of message block length parameters, as many of the longer-length-blocks may be processed, one after the other, as desired. However, a shorter-length-block must not be followed by a second shorter-length-block. At least one longer-length-block must intervene between shorter-length-blocks.

The following message block sequence is valid:

... S-L-B ... G-L-B ... S-L-B ... G-L-B ... G-L-B ...(S-L-B's are all followed by G-L-B's.)

The following message block sequence is invalid:

G-L-B ... S-L-B ... S-L-B ...(An S-L-B cannot follow an S-L-B)

9.0 OPERATION AS AN ENCODER

When the device is used as an encoder the correction status is not meaningful since the it is not performing corrections. Nor would it be meaningful to interpret the two optional status bytes as check bytes. Therefore, the initialization control sequence must not select the option of outputting status. SSET must be held LOW during the 6 clock, phase one, $\overline{RESET}$ sequence, for encoding to function properly.

When a message block is being input to the encoder, the bytes are clocked into the D7-D0 inputs on the rising edge of CK. The user must appended a number of "dummy" bytes equal to the number of check bytes (2t) that will be added by the encoder. These user-added bytes may be any arbitrary value since they are only used to "hold" a space for the check bytes. The encoder will "correct" these "dummy" bytes into check bytes. The $\overline{ERASE}$ input is used in this situation to indicate the dummy bytes used for check byte calculation. (Note that this device is always acting as a decoder, but due to the mathematical properties of Reed-Solomon codes and the way these devices were designed, they can also act as encoders - when the "dummy" bytes are corrected they become encoded check bytes.) CEN must be set HIGH and SSET must be set LOW throughout the entire message block including the dummy check bytes.

The timing for $\overline{ERASE}$ during an encoding operation is identical to the timing for DEN (see Fig 9a).

9.1 ENCODED DATA OUTPUT

After passing through the encoder, the encoded message block is output at Q7-Q0. The DRY (Data Ready) output stays HIGH for all data bytes and goes LOW for all check bytes, thus defining the meaning of these bytes to the external logic. The timing of this operation is shown in Fig. 9b.

Fig. 9a Encoding input timing.

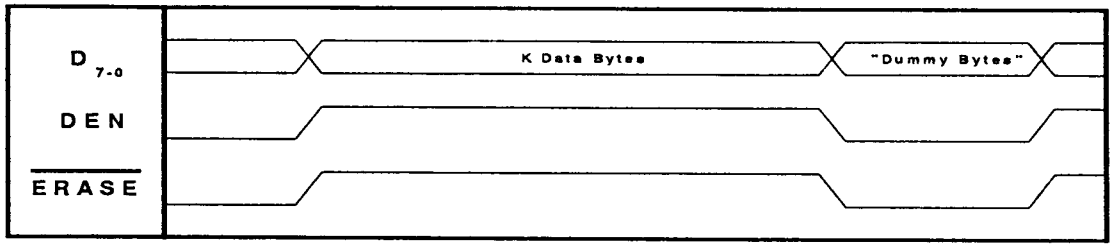
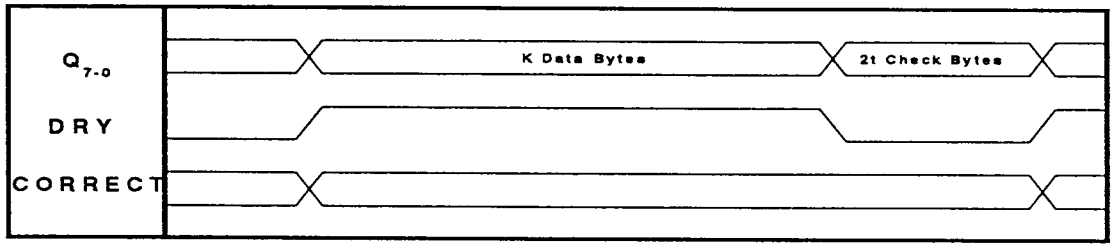


Fig. 9b Encoding output timing.



10.0 OPERATION AS A DECODER

When operating as a decoder, the device clocks in the encoded message block from the D7-D0 input bus on the rising edge of CK. The device then computes polynomials for this data using a high performance Reed-Solomon coding algorithm, and then proceeds to use the calculated polynomials to correct any errors, if possible. These polynomials are a series of complex equations that will indicate not only the position of incorrect bytes but will also produce the necessary information to correct them. (For further information on the Reed-Solomon coding process, refer to AHA Applications Note ***Primer: Reed-Solomon Error Correcting Codes,*** which describes this operation in detail.) The timing of the decoding operation is defined in Figure 10a, for both input and output.

The action taken by the decoder with respect to a given message block is determined in all cases by the magnitude of the errors received (e+(E/2)). The device reports it's action via the CORRECT output pin. If P = 2t, a HIGH output on the CORRECT pin indicates that the message block being output is correct; a correction operation was successfully performed if necessary. A LOW output (when P = 2t) indicates that a correction was not performed because there were too many errors. In situations where P has been chosen to be not equal to 2t, the meaning of the CORRECT output is more difficult to define. The exact meaning of the CORRECT output, under all conditions, is determined using the table in section 10.3.

During decoding, erroneous bytes in known positions (flagged by a bad parity bit, a signal dropout detector, or any other external error detection method) are indicated by pulling the *ERASE* input low during these bytes. More information regarding erasures is given in section 7.0 Functional Description.

10.1 OPTIONAL STATUS BYTES

The optional status bytes, that may be output at the end of a message block, indicate the number of erasures and errors encountered and may used to determine the exact function of the CORRECT output, when P 2t. The status bytes are defined as shown below in Fig. 10a. The timing of these status bytes is shown in Figs. 10d and 10e.

Fig. 10a Optional status bytes.

FIRST STATUS BYTE								SECOND STATUS BYTE							
$\overline{CA}$	E							e+E							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Fig. 10b Decoder input timing.

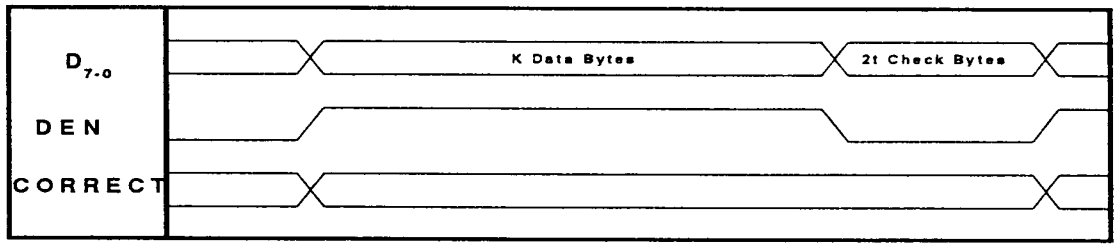


Fig. 10c Decoder output timing.

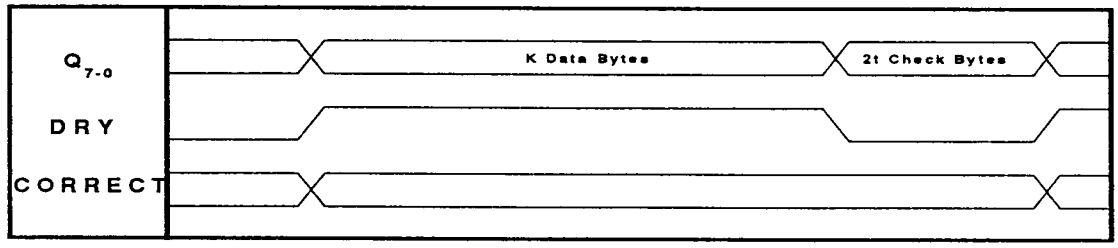


Fig. 10d Status/Check byte output with SSET high.

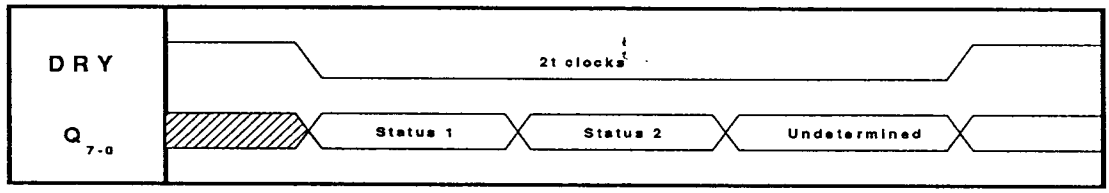
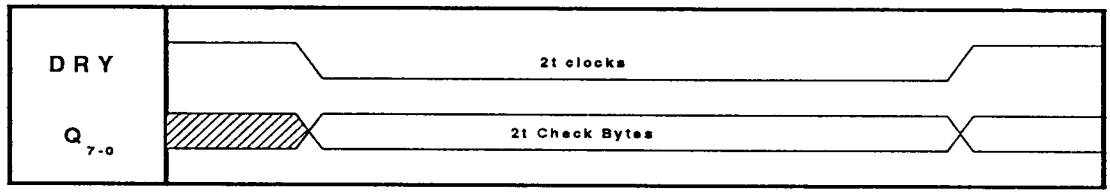


Fig. 10e Status/Check byte output with SSET low.



In the first status byte, bits 0 through 6 are a binary count of the number of erasures encountered for a given message block (ie. the number of bytes that were flagged by the external $\overline{ERASE}$ input). CA (Correction Attempted) is a one-bit active LOW flag indicating that a correction was attempted. CA goes LOW when: $(2e+E) \leq 2t$. Therefore, anytime CA is HIGH, the message block should be retransmitted since there were probably too many errors to reliably correct. Also, if P = 2t, then CA will always be LOW when the CORRECT output pin is HIGH, and HIGH when CORRECT is LOW.

In the second status byte, bits 0 through 7 are a binary count of the total number of erroneous bytes encountered (errors + erasures).

10.2 DETERMINING DECODER PERFORMANCE BOUNDARIES

P and t are both independently selectable by the user during the initialization control sequence. The various configurations of P and t are described as follows:

P > 2t This is not a sensible choice since this implies that more check bytes are allocated for (correction-only) purposes than there are total check bytes (for both correction and detection). This would result in flagging all data blocks as incorrect; the CORRECT output would remain LOW, under all circumstances.

P = 2t This configuration maximizes the ability to correct errors, particularly if (t) itself has been chosen to be its maximum value of 10 (for the AHA4010). This is the usual choice.

P < 2t This increases the relative level of error detection capability; (relative to the level of error correction capability). This situation will cause the CORRECT output to flag a message block as uncorrectable at an error level below that which the code is capable.

10.3 DECODER ACTION SUMMARY

The following table is a complete summary of the action taken by the AHA4010 and AHA4510 under various specifications of t, P, and e+(E/2):

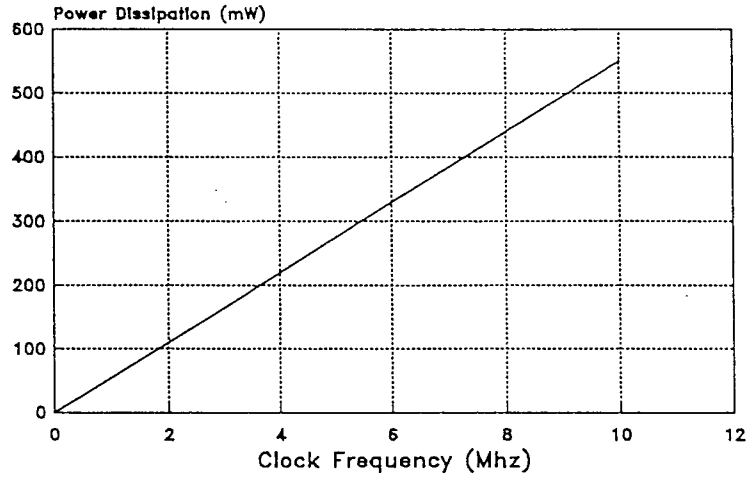
Case	*Error Tally*	*Correct Line*	*Action Taken*	*Remarks*
P > 2t	Irrelevant	LOW	No Correction	Nonsense Case (CA=1)
P = 2t	G ≤ t	HIGH	Block Corrected	Optimum Situation (CA=0)
	G > t	LOW	No Correction	Too Many Errors; Neither Correctable Nor Detectable. See Note 1. (CA=1)
P < 2t	G ≤ P/2	HIGH	Block Corrected	Desired Situation (CA=0)
	P/2 < G ≤ t	LOW	Block Corrected	Block Reported as Uncorrectable, but Error Pattern Guaranteed to be Detectable (CA=0)
	t < G < 2t-P/2	LOW	No Correction	Same as above, except (CA=1)
	2t-P/2 < G	LOW	No Correction	Too Many Errors; Neither Correctable Nor Detectable. See Note 1. (CA=1)

In this table G = e+(E/2) = The "burden of correction" placed on the device.

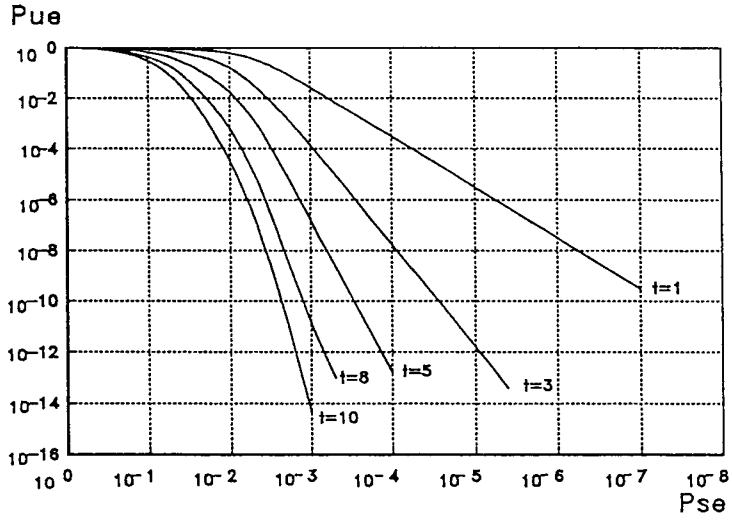
Note 1: if 2t < E, then all erasures will be ignored and an attempt will be made to correct the errors that remain. This is useful in situations where ERASE is used to mark entire blocks as having potential errors even though there may be a high percentage of correct information within the marked block.

11.0 CHARACTERISTIC CURVES

11.1 POWER DISSIPATION VS. CLOCK FREQUENCY



11.2 CODE PERFORMANCE CURVES



The above curve shows the probability of a symbol error (Pse) versus the probability of an uncorrectable block error (Pue) for block size of N = 255. They show the ability of various levels of Reed-Solomon error correction to restore the integrity of the corrupted data. For example, using 255 byte blocks, if 1 out of 1000 of the received bytes have one or more bit errors, RS correction with t=5 will restore the data to 1 error in 2 million blocks (510 million bytes). The input byte error rate corresponds to an input block error rate of 1 in 4.

12.0 PACKAGING

PLCC Dimensions

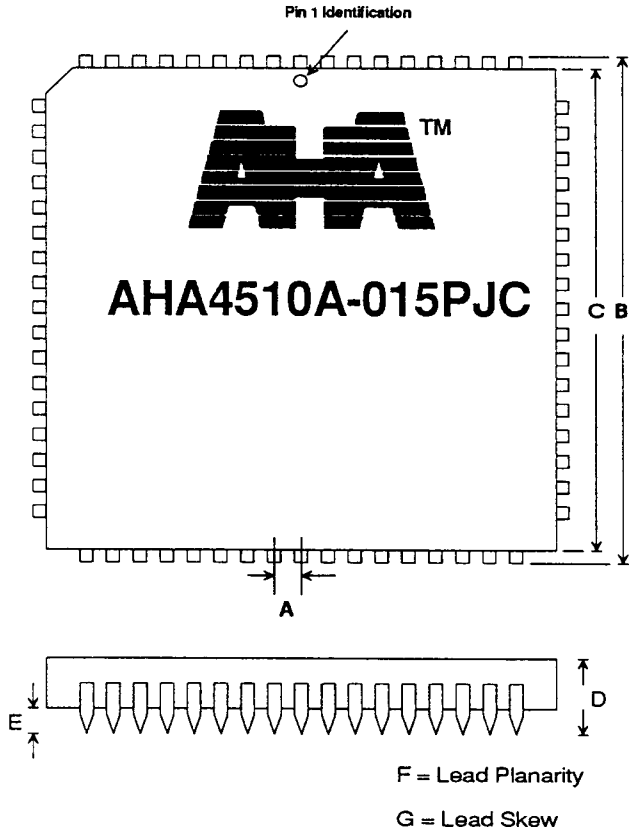
Inches (Millimeters)

A	B max	C max	D max	E min	F ±	G ±
.050 (1.27)	.995 (25.27)	.954 (24.23)	.180 (4.57)	.020 (0.51)	.002 (0.051)	.0035 (0.089)

Shipping Tubes

Pin Count	Standard Qty/Tube
68	18

Packaging



Complete Package Drawing Available Upon Request.

13.0 THERMAL CHARACTERISTICS

Thermal Characterization *

68 PLCC

Air Velocity M/s (ft/min)	Θ ΔT=30°	Max Power (watts) T = 70° T_j=110°	Max Power (watts) T =70° T_j=85°
0 (0)	48	0.8	0.3
1 (197)	37	1.2	0.4
3 (591)	31	1.3	0.5

** Measured package values. In actual usage conditions, max power may vary as much as + 20%, -30%, depending upon die size, package mounting, and system placement. Adjustments for specific conditions and alternate lead counts can be made. Please contact your Account Manager of Packaging Support Engineer.*

T_{amb} = Ambient temperature at part surface.
T_j = Allowable junction temperature based upon silicon process.

PLCC Materials and Specifications

Standard:

- Stamped lead frame
- Olin 151 copper alloy
- Spot silver
- RTV chip coating
- Solder dip lead finish

Measurement Conditions:

- 0.40 cm^2 die size.
- 70°C ambient.
- Sea level air pressure.
- No parts on the back side of the board.
- Unimpeded laminar airflow at measured package surface.

14.0 ORDERING INFORMATION

14.1 AVAILABLE PARTS

PART NUMBER	DESCRIPTION
AHA4310A-015PJC	RS ECC Integrated Circuit (t=3) 15 MHz
AHA4510A-015PJC	RS ECC Integrated Circuit (t=5) 15 MHz
AHA4810A-010PJC	RS ECC Integrated Circuit (t=8) 10 MHz
AHA4010A-010PJC	RS ECC Integrated Circuit (t=10) 10 MHz

14.2 PART NUMBERING

AHA	4010	A -	010	P	J	C
Manufacturer	Device Number	Revision Level	Speed Designation	Package Material	Package Type	Test Specification

Device Number:

4310 (t = 3)
4510 (t = 5)
4810 (t = 8)
4010 (t = 10)

Package Material Codes:

P Plastic

Package Type Codes

J J - Lead Chip Carrier

Test Specifications

C Commercial 0°C to +70°C

Detailed test information is available on request.

15.0 TECHNICAL PUBLICATIONS AVAILABLE

The following may be obtained by contacting the AHA Technical Publications department.

- **Primer: Reed-Solomon Error Correcting Codes** - ANRS01
- **Interleaving for Burst Error Correction** - ANRS02
- **AHA4x10 Product Brief** - PB4x10
- **AHA4600 T=16 CCSDS Device Set** - PS4600
- **AHA5101/5121 QIC™ Tape Formatter/Controller** - PB5101
- **AHA3101 Data Compression Coprocessor** - PB3101