AVPro® 5002R
Dual SCART A/V Switch

DATA SHEET

SEPTEMBER 2008

DESCRIPTION

The AVPro® 5002R device is an audio/video switching IC that supports an input/output port, an input only port, and an output only port. The device includes multiplexers that allow the inputs to be routed to the outputs in various configurations. Additional outputs are provided to drive an external RF modulator. The video outputs of the multiplexers are buffered to drive 150Ω loads. The audio outputs are buffered to provide 2 Vrms output. The 5002R has features optimized for Canal+ satellite receiver applications, but it can also be used in other applications that require control of multiple audio and video sources.

FEATURES

- Two SCART connections (Auxiliary, TV)
- Video section
  - Integrated output drivers
  - RGB, SVHS, composite outputs
  - Programmable RGB gain
- Audio section
  - Dual mode volume control
    0 or 6 dB gain, plus 0 to -63 dB attenuation (1 dB step)
  - Programmable gain on DAC input channels
- Serial port control of switching I²C bus
- 64-lead LQFP, 48 QFN package options

BLOCK DIAGRAM

Rev 2.1
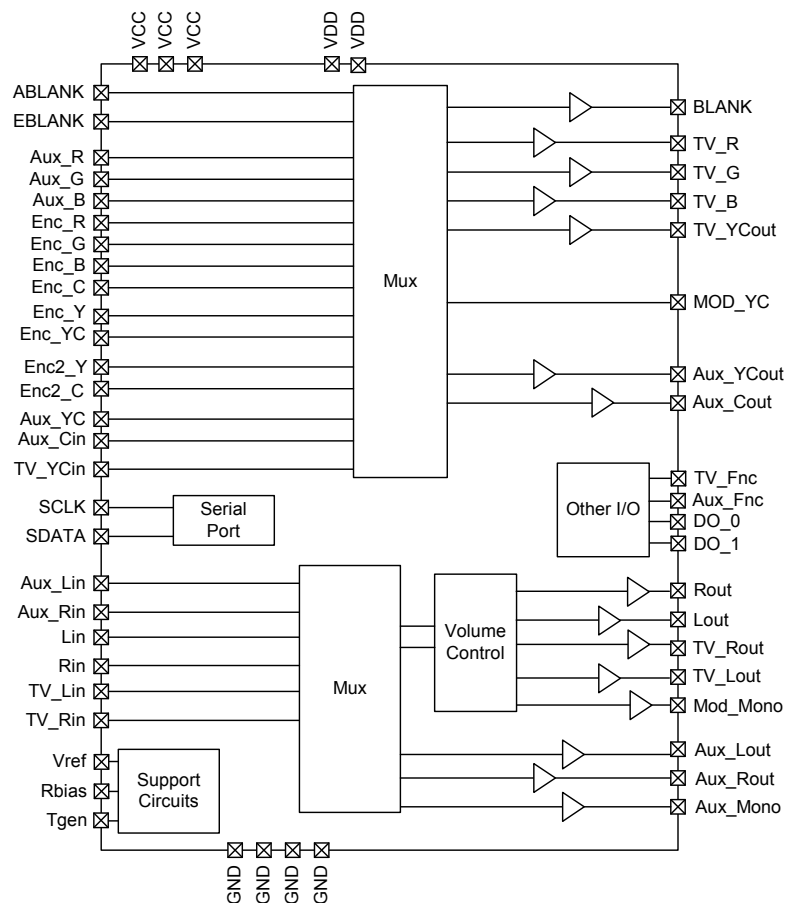
Functional Description

The 5002R is an audio/video switching device. The device integrates both audio and video drivers so that it can directly drive the SCART interface. All programmable functions of the device are controlled through a standard I^{2}C serial interface and a set of internal registers.

The device will interface to an external video encoder that provides six video outputs. In addition, the 5002R includes two programmable digital outputs and provides inputs for the TV SCART audio/video.

SCART Video Switching

The device is designed to accept video signals from an auxiliary SCART connector, TV SCART connector, and an external video encoder/DAC device. The devices include a set of analog multiplexers that receive video signals from these sources and allow routing of the signals to the various video outputs. The video output drivers have a nominal gain of 2 V/V to allow for a series resistance of 75Ω prior to the 75Ω termination. A block diagram of the video switching function is provided in Figure 1. Details of the register settings are provided in the section titled "Serial Port Register Tables".
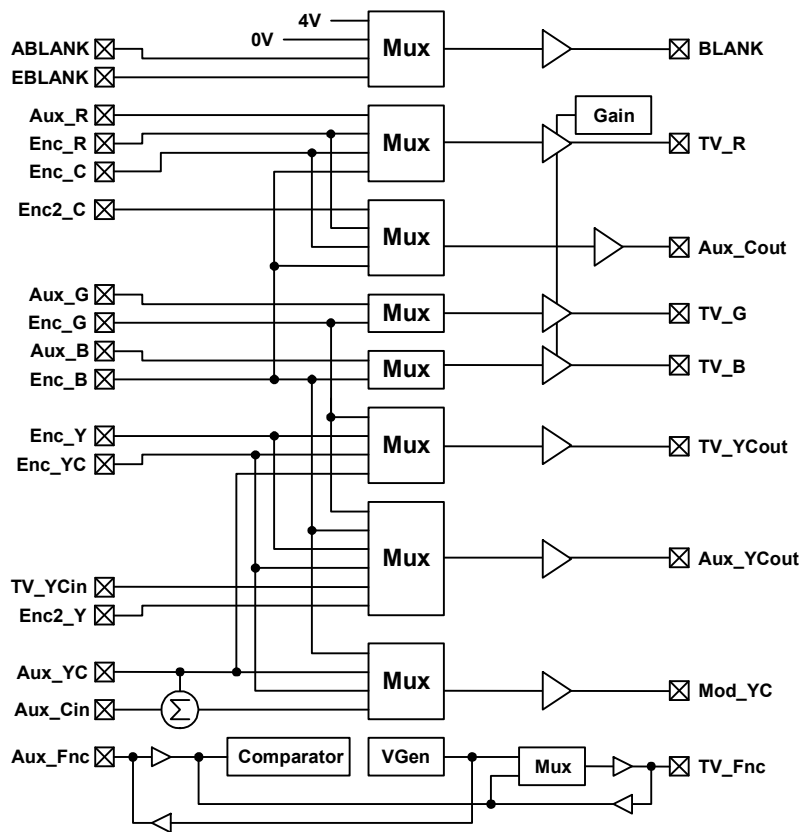

FIGURE 1: 5002R VIDEO SWITCHING BLOCK DIAGRAM

Note: Aux_Cin, Enc2_Y and Enc2_C are not available on the 48QFN package option.

TV RGB Outputs

The device accepts RGB video signals from two sources. The *Aux_R*, *Aux_G*, *Aux_B* input pins are typically connected to the auxiliary SCART connector. The *Enc_R*, *Enc_G*, *Enc_B* input pins are connected to the RGB outputs of an external video encoder device. These outputs are used as a video source for the TV SCART pins *TV_R*, *TV_G*, and *TV_B*. The RGB video source is selected by setting the lower three (3) bits of serial port Register 1. When these bits are set to xxxxx000, the RGB source will be the encoder. When these bits are set to xxxxx001, the source will be the auxiliary port. The TV RGB outputs can be muted independently from the TV composite outputs. Setting Bit 6 of Register 1 low (0) will allow normal operation. Setting Bit 6 high (1) will set the TV RGB outputs to the blank level.

RGB Gain: The gain of the RGB outputs can be adjusted to one of four different levels. Bits 4 and 5 in Register 2 set the gain of the RGB output amplifiers according to the following table:

Bit 5	Bit 4	RGB Amplifier Gain
0	**0**	**Gain = 2 V/V = A_0**
0	1	Gain = A_0 - 10%
1	0	Gain = A_0 - 20%
1	1	Gain = A_0 - 30%

DC Restore: The device will generate a DC restore level on each video output based on timing referenced to a horizontal sync pulse. When the sync pulse is detected, the DC restore circuit will act to position the blank level to 1.2V at the respective RGB output pins and the respective composite output pins (0.6V at the respective RGB and composite video output load). The device can be programmed to look for the horizontal sync pulse on all of the RGB input pins or on the associated composite video input pin (*Aux_YC* for the auxiliary port or *Enc_YC* for the external encoder). Bit 7 of Register 1 determines the horizontal sync source. At power-up, this bit defaults to a low (0) state, which programs the device to look for sync detect on the RGB input signals. In this mode, the device can detect a horizontal sync on any of the three RGB input signals. When Bit 7 is set to a high (1) state, the device will look for a sync detect from the signal on either the *Aux_YC* or *Enc_YC* pin depending on which source is selected.

Blanking: The signal on the *Blank* output pin is determined by the state of two MSBs in Register 2 according to the following table:

Bit 7	Bit 6	*Blank* source
0	**0**	**BLANK = ABLANK**
0	1	BLANK = EBLANK
1	0	BLANK = 0V
1	1	BLANK = 4V @ IC output pin

The user must insure that the source of the *Blank* output is the same as the source for the RGB outputs, i.e. *ABLANK* is selected when the auxiliary RGB is active and *EBLANK* is selected when the encoder RGB is active.

TV Composite Output

The device provides inputs for two composite video sources that can be switched to the TV SCART composite video pin, *TV_YCout*. The *Aux_YC* input pin is typically connected to the "Video In" pin (pin 20) on the auxiliary SCART connector. The *Enc_YC* input pin is typically connected to the "YC" or "CVBS" output from the external video encoder device. Selection of the video source for the TV composite output is accomplished when the RGB video source is selected (see the register tables). When Register 1 is set to xxxxx000, the Encoder input is selected and when set to xxxxx001, the Auxiliary input is selected.

TV SVHS Output Mode

The device supports SVHS video format. The SVHS mode is selected for the TV SCART using the lower three (3) bits of Register 1(except for SVHS Enc 4 mode). When the SVHS mode is selected, the *TV_YCout* pin will provide the luminance signal output from the selected source. The chroma output will be provided on the *TV_R* pin. The video source for SVHS mode can be either the auxiliary port or the encoder port. When the auxiliary port is selected as the video source, the video on *Aux_R* will be provided at the *TV_R* output pin and the *Aux_YC* video will be provided at the *TV_YCout* pin.

The device will support SVHS mode for four encoder interface formats. The first encoder interface format accepts chroma signals on the *Enc_C* pin and luminance signals on the *Enc_Y* pin. This is designated "SVHS, Enc 1" mode. The second format will receive chroma information on the *Enc_B* pin and luminance information on *Enc_G*. This format is designated "SVHS, Enc 2". The third format will receive chroma information from the *Enc_R* pin and luminance information from the *Enc_G* pin. This mode is designated "SVHS, Enc 3" on the serial port register table. For these three modes, audio will come from the *Lin/Rin* inputs. The fourth format is designated "SVHS Enc 4" (not available in the 48QFN package option). It is selected by setting register one to xx110xxx. Chroma information is received on the Enc2_C input pin.

luminance is received on the *Enc2_Y* input pin. For this

mode only, audio will come from the *TV_Lin/TV_Rin* inputs, and the video will have chroma output on *Aux_Cout*, and luminance output on *Aux_YCout*.

When the SVHS mode is selected, the DC restore on the *TV_R* pin will average to approximately 1.7 VDC at the output pin. The DC restore circuit will act to position the blank level to 1.2V at the *TV_YCout* video output pin. The *TV_G* and *TV_B* outputs will be set to 0 VDC when the SVHS mode is active.

RF Modulator Output

The device provides an output, *Mod_YC*, to drive an external RF modulator. The *Mod_YC* output is a unity gain amplifier designed to drive a 1kΩ load or higher. When the device is operating in the RGB mode, the signal on the *Mod_YC* output will follow the same source as the *TV_YCout* output.

When the device is in the SVHS mode, the *Mod_YC* output can be driven by several sources depending on the SVHS video source. These various options are detailed in the serial port register table.

One case that requires additional detail is the auxiliary SVHS mode. In the SVHS mode, the *Aux_YC* video input will only provide luminance information. Composite video for the modulator output must be generated by summing this luma information with the chroma information from the auxiliary port. The input pin labeled *Aux_Cin* is used for this purpose. The *Aux_Cin* input pin is AC coupled to the same source that provides the input signal to *Aux_R*. An internal summing node combines the video signal on *Aux_Cin* (chroma) with the video signal on *Aux_YC* (luma) to generate a composite video signal. In the auxiliary SVHS mode, this signal is provided at the *Mod_YC* pin.

TV Composite Video Mute

The TV composite video outputs can be muted by programming the lower three (3) bits in Register 1. The power-up default condition is xxxxx111, (Auxiliary RGB source) which sets the TV composite video outputs to 0 VDC and switches the TV audio outputs to *Aux_Lin/Aux_Rin*. Setting these bits to xxxxx110 (Encoder RGB source) will also mute the TV composite video outputs and switch the TV audio outputs to *Lin/Rin*.

Auxiliary Composite Output

The auxiliary port includes a composite video output pin (*AUX_YCout*) that is typically connected to the "Video Out" pin (pin 19) on an auxiliary SCART connector. Bits 3-5 in Register 1 determine the source for the *AUX_YCout* pin as well as for the *Aux_Cout*. See register table.

Auxiliary SVHS Output Mode

In the SVHS mode, Pin 15 on the auxiliary SCART connector provides chroma information. To support this, the auxiliary port on the 5002R includes a chroma input pin (*Aux_Cin*) that is externally AC coupled to Pin 15 on the auxiliary SCART connector.

The device also includes an output pin (*Aux_Cout*) that provides a chroma output to Pin 15 (RED) on the auxiliary SCART connector. When connected with the Aux_R and Aux_Cin pins, this forms a bi-directional port as shown in the diagram below:
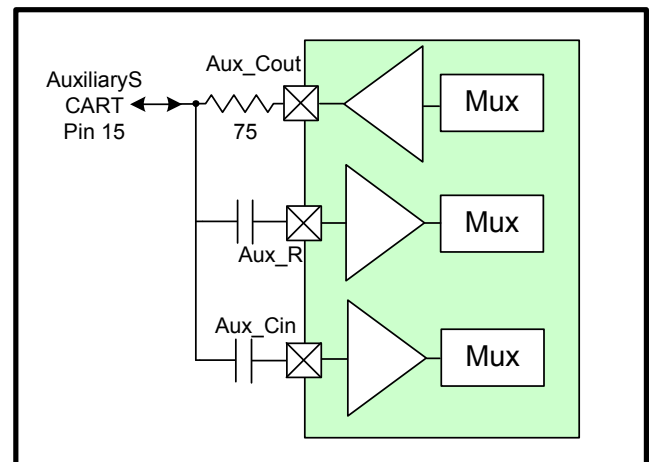
BI-DIRECTIONAL PIN CIRCUIT

Using this configuration, the device will support SVHS mode for four encoder interface formats. The first encoder interface format will receive chroma information from the *Enc_C* pin and luminance information from the *Enc_Y* pin. This format is designated "SVHS, Enc 1". The second format will receive chroma information on the *Enc_B* input and luminance information on *Enc_G*. This format is designated "SVHS, Enc 2". The third format will receive chroma information from the *Enc_R* pin and luminance information from the *Enc_G* pin. This mode is designated "SVHS, Enc 3" on the serial port register table. For these three modes, audio will come from the *Lin/Rin* inputs. The fourth format is designated "SVHS Enc 4" (not available in the 48 QFN option). Chroma information is received on the *Enc2_C* input pin and the luminance is received on the *Enc2_Y* input pin. For this mode only, audio will come from the *TV_Lin/TV_Rin* inputs.

When the SVHS mode is selected, the DC restore on the *Aux_Cout* pin will average to approximately 1.7 VDC at the pin (0.85 at the video output load). The DC restore on the *Aux_YCout* pin will set the blank level to 1.2 V at the IC pin or approximately 0.6 V across the video output load.

The RGB mode of operation requires special consideration. The output driver on the Aux_Cout pin acts as part of the load for the RED signal on pin 15 of the SCART connector. Register 1 must be set to x0011001 to select the auxiliary SCART as the RGB source for the TV outputs and selects the external video encoder as the source for the Auxiliary SCART connector. This provides an output impedance of about 0Ω on the Aux_Cout pin. This setting also allows the Enc_C pin to pass through the Aux_Cout pin. **Due to this, the outputs of the external video encoder must be disabled to prevent corruption of the incoming RED video signal.**

Auxiliary Video Mute

All auxiliary video outputs can be simultaneously disabled by programming Bits 3-5 in Register 1. The power-up default condition is xx111xxx, which sets all auxiliary video outputs to 0 VDC and switches the auxiliary audio outputs to *Lin/Rin*.

Function Switching

The device provides functions switching pins for both the Auxiliary (*Aux_Fnc*) and TV (*TV_Fnc*) SCART ports. Both of these pins are bi-directional. The direction of the pins is determined by setting bits in Register 2 according to the following table:

Bits	*Aux_Fnc*	*TV_Fnc*
xxxx**00**xx	**output**	**output**
xxxx01xx	output	input
xxxx10xx	input	output
xxxx11xx	Passthru I/O	Passthru O/I

For the case where Register 2 is set to xxxx11xx, the input signal on the *Aux_Fnc* pin is passed directly through to the

TV_Fnc pin as an output, or vice versa. This mode is useful when the rest of the system powers down and all signals from the auxiliary port are passed directly through to the TV port, or vice versa.

When a function pin is set as an input, the voltage on that pin is applied to an internal comparator. The comparator senses the voltage on the input pin and sets the two (2) LSBs in the read register according to the following table:

| Input voltage	Bits	Function
< 2.0 V	xxxxxx00	Normal TV
4.5 to 7.0V	xxxxxx01	16:9 aspect
>9.5 V	xxxxxx10	Peritelevision

When a function pin is set as an output, the output level for the pin is determined by the state of the two LSBs in Register 2, according to the following table:

Bits	Output voltage	Function
xxxxxx**00**	**~0 V**	**Normal TV**
xxxxxx01	~6 V	16:9 aspect
xxxxxx10	~ 11 V	Peritelevision
xxxxxx11	~ 11 V	Peritelevision

Note that both the *Aux_Fnc* pin and the *TV_Fnc* pin can be set as outputs simultaneously, however they will have the same output voltage.

The function output circuit includes short circuit protection. When a function pin is in the 6V or 11V output mode, if the SCART connection is shorted to ground, then the output is disabled. Likewise, when a function pin is in the 0V output mode, if the SCART connection is connected to a voltage source, then the output is disabled. The load for the function outputs is designed to be 10kΩ or higher.

Figure 2: 5002R Audio Switching Block Diagram
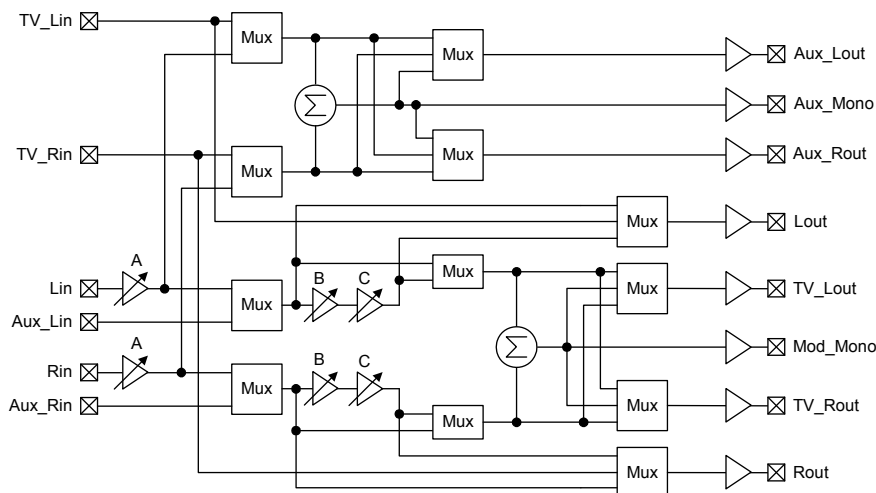
A: DAC Input Gain (0, 6, 9, or 11.5dB)
B: Volume Control Gain (0 or 6dB)
C: Volume Control Attenuation (0 to –63 dB in –1dB steps)

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SCART Audio Switching

The audio inputs are considered to be associated with the respective video inputs. As a result, the video selection determines which audio signals will be switched to a given SCART output. Refer to the serial port register table for more information. Also see the audio switching block diagram shown in Figure 2.

The 5002R provides inputs for the auxiliary audio source (*Aux_Lin*/*Aux_Rin*), a stereo DAC associated with the video encoder inputs (*Lin*/*Rin*), and inputs from the TV SCART (*TV_Lin/TV_Rin*).

TV Audio Operation

The audio source for the TV port is selected in concert with the video source using the three (3) LSBs of Register 1. The selected audio signals are input to internal multiplexers that allow the user to select between mono and stereo output options. Bits 4 and 5 of Register 3 control the stereo/mono selection according to the following table:

Bit 1	Bit 0	*TV left source*	*TV right source*
0	**0**	**left input**	**right input**
0	1	left + right	left + right
1	0	left input	left input
1	1	right input	right input

At power-up, these bits default to 00 putting the device in the stereo mode.

Volume Control: The left and right TV audio channels can be selected to pass through volume control circuits. Each volume control circuit is formed by a serially connected amplifier and attenuator pair. The amplifier is programmed by register 4, bit 2("0" for 0 dB and "1" for 6 dB gains). The attenuator is programmed by the lower 6 bits of register 0("xx000000" for 0 dB and "xx111111" for –63 dB attenuation, in –1 dB steps).

DAC Input Gain (*Lin/Rin*): To support audio DACs that have a limited output range, the 5002R provides programmable gain amplifiers on the *Lin* and *Rin* inputs. The gain is set by Bits 2 and 3 of Register 3, according to the following table:

Bit 3	Bit 2	Gain
0	**0**	**Gain = 0 dB**
0	1	Gain = 6 dB
1	0	Gain = 9 dB
1	1	Gain = 11.5 dB

TV SCART Audio Outputs: The first pair of signals is labeled *TV_Lout* and *TV_Rout* on the block diagram. *TV_Lout* and *TV_Rout* are typically used to drive the TV SCART audio pins. These outputs also have an internal multiplexer that allows the user to select TV audio either before or after the internal volume control function. When Bit 0 in Register 4 is set low (0), the volume control is used. When this bit is set high (1), the volume control is bypassed. The power-up default state is volume control active.

TV Audio Line Outputs: The second pair of signals is labeled *Lout* and *Rout* on the block diagram. *Lout* and *Rout* are standard line outputs. The *Lout*/*Rout* outputs have an internal multiplexer that allows the user to select TV audio either before or after the internal volume control function. When Bit 1 in Register 4 is set low (0), the volume control is used. When this bit is set high (1), the volume control is bypassed. The power-up default state is volume control active. In addition, the audio inputs from the TV SCART connector (*TV_Lin/TV_Rin*) can be switched to the line outputs. This is controlled by bit-3 of Register 4. Setting this bit low (0) is the normal operation where the line outputs follow the TV SCART outputs. Setting this bit high (1) will switch the line outputs to the audio source on the *TV_Lin/TV_Rin* inputs.

RF Mono Output: The *TV_Lout* and *TV_Rout* signals are also summed internally to generate a mono audio signal for an external RF modulator. This output is labeled *Mod_Mono*. The internal summing circuit is after the volume control mux so the audio control on this output will be the same as that selected for the *TV_Lout* and *TV_Rout* outputs.

TV Audio Mute: A mute function is provided for all *TV* audio outputs. The mute function is controlled by setting Bit 6 in Register 0. When this bit is set to a high state (1), all *TV* audio outputs are muted. This will be the default condition at power-up. When the bit is set to a low state (0), the audio path will be in normal operating mode. This bit can be set independent of the volume control such that the outputs can be muted before any change in volume, or any switching of audio sources.

Auxiliary Audio Operation

The auxiliary port includes stereo audio outputs for a SCART connector (*Aux_Lout*, *Aux_Rout*) and a mono audio output (*Aux_Mono*). These outputs can choose between the *Lin*/*Rin* input pins or the *TV_Lin/TV_Rin* input pins. The audio inputs are switched in concert with the associated video inputs according to Bits 3-5 in Register 1.

Internal multiplexers allow the *Aux_Lout* and *Aux_Rout* outputs to be configured into either stereo or mono audio outputs. The two MSBs of Register 3 control the stereo/mono selection according to the following table:

Bit 1	Bit 0	*Aux_Lout source*	*Aux_Rout source*
0	**0**	**Lin**	**Rin**
0	1	Lin+Rin	Lin+Rin
1	0	Lin	Lin
1	1	Rin	Rin

At power-up, these bits default to 00 putting the device in the stereo mode.

The *Aux_Mono* output is generated through an internal summing node that combines the signals of the *Aux_Lout* and *Aux_Rout* outputs. All three auxiliary audio outputs can be muted by setting the MSB in Register 0. This bit is set high (1) at power-up causing the outputs to be muted. Setting this bit low (0) enables all auxiliary audio outputs.

Digital Outputs

The 5002R provides two programmable digital outputs, *DO_0* and *DO_1 (not available on the 48 QFN option)*. These pins are general purpose outputs programmed by setting Bit 0 and 1 in Register 3. Setting the register bits to 0 puts these outputs in the logic low state. Setting the register bits to 1 puts the outputs in the logic high state. Internal pull-up resistors (approximately 17kΩ) are included on these pins.

Serial Port Definition

Internal functions of the device are monitored and controlled by a standard inter-IC (I^2C)bus with data being transferred MSB first on the rising edge of the clock. The serial port operates in a slave mode only and can be written to or read from. The device uses 7-bit addressing, and does not support 10-bit addressing mode. The write register data is sent sequentially, such that if register 4 is to be programmed, then registers 0, 1, 2, 3 and 4 need to be sent. If only register 2 needs to be programmed, then only registers 0, 1 and 2 data need to be sent. It will support standard and fast bus speed. The default address of the device is 1001000x (1001000 for Write and 10010001 for Read).

The 5002R includes a read register in which the upper four bits identify the specific chip within the AVPro® family. This allows a single application platform and software to work with a wide variety of AVPro® chips. The ID code for the 5002R is 0001.

Data Transfers

A data transfer starts when the *SDATA* pin is driven from HIGH to LOW by the bus master while the *SCLK* pin is HIGH. On the following eight clock cycles, the device receives the data on the *SDATA* pin and decodes that data to determine if a valid address has been received. The first seven bits of information are the address with the eighth bit indicating whether the cycle is a read (bit is HIGH) or a write (bit is LOW). If the address is valid for this device, on the falling *SCLK* edge of the eighth bit of data, the device will drive the *SDATA* pin low and hold it LOW until the next rising edge of the *SCLK* pin to acknowledge the address transfer. The device will continue to transmit or receive data until the bus master has issued a stop by driving the *SDATA* pin from LOW to HIGH while the *SCLK* pin is held HIGH

Write Operation: When the read/write bit (LSB) is LOW and a valid address is decoded, the device will receive data from the *SDATA* pin. The device will continue to latch data into the registers until a stop condition is detected. The device generates an acknowledge after each byte of data written.

Read Operation: When the read/write bit (LSB) is HIGH and a valid address is decoded, the device will transmit the data from the internal register on the following eight *SCLK* cycles. Following the transfer of the register data and the acknowledge from the master, the device will release the data bus.

Reset: At power-up the serial port defaults to the states indicated in boldface type. The device also responds to the system level reset that is transmitted through the serial port. When the master sends the address 00000000 followed by the data 00000110, the device resets to the default condition.

SERIAL PORT REGISTER TABLES

Read register Device Address = 10010001

FUNCTION	BITS	DESCRIPTION
Function Control Input	xxxxxx00 xxxxxx01 xxxxxx10	*TV_Fnc* or *Aux_Fnc* pin level =Level 0 < 2V *TV_Fnc* or *Aux_Fnc* pin level =Level 1A ~6.0V *TV_Fnc* or *Aux_Fnc* pin level = Level 1B >9.5V
Not Used	xxxx00xx xxxx11xx	**Ignore these bits**
Device ID code	0001xxxx	This code identifies the device type as the 5002R

Write Registers: Device Address = 10010000 (**Bold** indicates default setting)

Register 0: Audio Control Register A

FUNCTION	BITS	DESCRIPTION
Volume Control Attenuation for TV, Line or Mod_Mono audio	xx**000000** xx011111 xx100000 xx111111	**Audio volume = maximum (0 dB)** Audio volume = minimum (-31 dB attenuation) Extended TV audio volume control range. Range is approximately -32 dB to -63 dB.
TV audio mute	x0xxxxxx x**1**xxxxxx	TV audio (*TV_Lout/TV_Rout, Lout/Rout, Mod_Mono*) output = normal audio output **TV audio (*TV_Lout/TV_Rout, Lout/Rout, Mod_Mono*) output = Muted**
AUX audio mute	0xxxxxxx **1**xxxxxxx	AUX audio (*Aux_Lout/Aux_Rout*) output = normal audio output **AUX audio (*Aux_Lout/Aux_Rout*) output = Muted**

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Register 1: Audio/Video Control Register; audio/video source select bits

TV A/V source	Bits	*TV_R*	*TV_G*	*TV_B*	*TV_YCout*	*Mod_YC*	*TV_Lout, TV_Rout*
RGB/YC, Encoder	xxxxx000	Enc_R	Enc_G	Enc_B	Enc_YC	Enc_YC	Lin, Rin
RGB/YC, Auxiliary	xxxxx001	Aux_R	Aux_G	Aux_B	Aux_YC	Aux_YC	Aux_Lin, Aux_Rin
SVHS, Enc 1	xxxxx010	Enc_C	0V	0V	Enc_Y	Enc_YC	Lin, Rin
SVHS, Enc 2	xxxxx011	Enc_B	0V	0V	Enc_G	Enc_YC	Lin, Rin
SVHS, Enc 3	xxxxx100	Enc_R	0V	0V	Enc_G	Enc_B	Lin, Rin
SVHS, Aux 1**	xxxxx101	Aux_R	0V	0V	Aux_YC	AuxYC+AuxCin	Aux_Lin, Aux_Rin
TV mute	xxxxx110	Enc_R	Enc_G	Enc_B	0V	0V	Lin, Rin
TV mute	xxxxx**111**	**Aux_R**	**Aux_G**	**Aux_B**	**0V**	**0V**	**Aux_Lin,Aux_Rin**

Aux A/V source	Bits	*Aux_Cout*		*Aux_YCout*		*Aux_Lout, Aux_Rout*
Composite, Enc 1	xx000xxx	0V		Enc_B		Lin, Rin
Composite, Enc 2	xx001xxx	0V		Enc_YC		Lin, Rin
Composite, TV	xx010xxx	0V		TV_YCin		TV_Lin, TV_Rin
SVHS, Enc 1	xx011xxx	Enc_C		Enc_Y		Lin, Rin
SVHS, Enc 2	xx100xxx	Enc_B		Enc_G		Lin, Rin
SVHS, Enc 3	xx101xxx	Enc_R		Enc_G		Lin, Rin
SVHS, Enc 4***	xx110xxx	Enc2_C		Enc2_Y		TV_Lin, TV_Rin
Aux mute	xx**111**xxx	**0V**		**0V**		**Lin, Rin**

Function	Bits	Description
TV RGB Mute	x**0**xxxxxx	**TV RGB OUTPUTS ARE ACTIVE**
	x1xxxxxx	TV RGB outputs are mute (Blank level)
RGB Sync Source	**0**xxxxxxx	**RGB sync /DC restore source = RGB**
	1xxxxxxx	RGB sync /DC restore source = Aux_YC or Enc_YC depending on source selection

Register 2: Video Control Register; video function bits

Function	Bits	Description
Function Control Output Voltage	xxxxxx**00**	**Level 0; normal TV output (Function Voltage ~ 0V)**
	xxxxxx01	Level 1A; 16:9 aspect ratio (Function Voltage ~ 6V)
	xxxxxx10	Level 1B; Peritelevision output mode (Function Voltage ~ 12V)
	xxxxxx11	Level 1B; Peritelevision output mode (Function Voltage ~ 12V)
Function Pin Control*	**xxxx00xx**	**Aux_Fnc pin = output, TV_Fnc pin = output**
	xxxx01xx	Aux_Fnc pin = output, TV_Fnc pin = input
	xxxx10xx	Aux_Fnc pin = input, TV_Fnc pin = output
	xxxx11xx	Signals will pass through from Aux_Fnc to TV_Fnc or vice versa. The voltage applied to this pin (when set as an input) sets the state of the two LSBs of the read register. See the note*
RGB Gain Control	xx**00**xxxx	**RGB output amplifier gain = normal**
	xx01xxxx	RGB output amplifiers attenuated by 10%
	xx10xxxx	RGB output amplifiers attenuated by 20%
	xx11xxxx	RGB output amplifiers attenuated by 30%
BLANK output selection	**00**xxxxxx	**BLANK = ABLANK**
	01xxxxxx	BLANK = EBLANK
	10xxxxxx	BLANK = 0V
	11xxxxxx	BLANK = 4V @ IC output pin

* Function pin voltages: (I) in output mode, are defined by the two LSBs of register 2, (II) in input mode, set the state of the two LSBs of the read register.
 Digital read is not meaningful in the pass-through mode(xxxx11xx).
** Aux_Cin is not available on the 48 QFN package option.
*** Not available in the 48 QFN package option.

Register 3: Audio and general purpose control register B

Function	Bits	Description
DO_0 output control*	xxxxxxx**0**	**DO_0 output = 0 (low)**
	xxxxxxx1	DO_0 output = 1 (high)
DO_1 output control*	xxxxxx**0**x	**DO_1 output = 0 (low)**
	xxxxxx1x	DO_1 output = 1 (high)
Lin/Rin Gain control	xxxx**00**xx	Input amplifier gain set at 0 dB
	xxxx01xx	Input amplifier gain set at 6 dB
	xxxx10xx	Input amplifier gain set at 9 dB
	xxxx11xx	Input amplifier gain set at 11.5 dB
TV Stereo/mono control	xx**00**xxxx	**TV audio mode: stereo**
	xx01xxxx	TV audio mode: mono (sum L+R) on both TV_Lout and TV_Rout
	xx10xxxx	TV audio mode: L channel on both TV_Lout and TV_Rout
	xx11xxxx	TV audio mode: R channel on both TV_Lout and TV_Rout
Aux Stereo/mono control	**00**xxxxxx	**Aux audio mode: stereo**
	01xxxxxx	Aux audio mode: mono (sum L+R) on both Aux_Lout and Aux_Rout
	10xxxxxx	Aux audio mode: L channel on both Aux_Lout and Aux_Rout
	11xxxxxx	Aux audio mode: R channel on both Aux_Lout and Aux_Rout

* Not available in the 48 QFN package option.

Register 4: Audio control register C

Function	Bits	Description
TV volume control select 1	xxxxxxx**0**	**Volume control active on TV_Lout, TV_Rout; Mod_Mono**
	xxxxxxx1	TV_Lout, TV_Rout; Mod_Mono bypass the volume control
TV volume control select 2	xxxxxx**0**x	**Volume control active on Lout, Rout**
	xxxxxx1x	Lout, Rout bypass the volume control
Enable 6dB gain	xxxxx**0**xx	0 dB of additional gain added to volume control
	xxxxx1xx	6 dB additional gain added to volume control
Line Out Source	xxxx0xxx	Audio on *Lout/Rout* will be the same as the *TV_Lout/TV_Rout*
	xxxx1xxx	**Audio on *Lout/Rout* will be from the *TV_Lin/TV_Rin* inputs**
Not used	**0000**xxxx	Reserved, set to 0 for normal operation

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SCART Switching Table

INPUT PINS	OUTPUT PIN
Aux_R: Red input from Aux port Enc_R: Red input from Enc port Enc_B: Optional chroma input from Enc port Enc_C: Chroma input from Enc port	TV_R: Red video output to TV port or SVHS chroma output to TV port
Aux_G: Green input from Aux port Enc_G: Green input from Enc port	TV_G: Green video output to TV port
Aux_B: Blue input from AUX SCART Enc_B: Blue input from Enc port	TV_B: Blue video output to TV port
ABLANK: Blanking input from Aux port EBLANK: Blanking input from Enc port	BLANK: TV blanking output for RGB (also can have internal 0V or 4V produced at this pin)
Aux_YC: Composite input from Aux port Enc_YC: Composite input from Enc port Enc_Y: Luminance input from Enc port Enc_G: Optional luminance input from Enc port	TV_YCout: Composite video or SVHS Luminance output to TV port
Aux_YC: Composite input from Aux port Enc_YC: Composite input from Enc port Enc_B: Optional chroma input from Enc port Aux_Cin/Aux_YC: sum of chroma and luma	Mod_YC: Follows TV_YCout output. Composite (or luma sum with chroma) output to RF modulator
Enc_C: Chroma input from Enc port Enc_R: Optional chroma input from Enc port Enc_B: Optional chroma input from Enc port Enc2_C: Encoder 2 chroma input	Aux_Cout: Chroma output to auxiliary port
Enc_YC: Composite input from Enc port Enc_B: Optional chroma input from Enc port Enc_G: Optional luminance input from Enc port Enc_Y: Luminance input from Enc port TV_YCin: Composite input from TV SCART Enc2_Y: Encoder 2 luminance input	Aux_YCout: Composite video output to auxiliary port
Aux_Lin: Left audio input from Aux port Lin: Left audio input from audio DAC TV_Lin: Left audio input from TV SCART	Lout: Left audio output to RCA jack
Aux_Lin: Left audio input from Aux port Lin: Left audio input from audio DAC	TV_Lout: Left audio output to TV port
Lin: Left audio input from audio DAC TV_Lin: Left input from TV SCART	Aux_Lout: Left audio output to auxiliary port
Aux_Rin: Right audio input from Aux port Rin: Right audio input from audio DAC TV_Rin: Right audio input from TV SCART	Rout: Right audio output to RCA jack
Aux_Rin: Right audio input from Aux port Rin: Right audio input from audio DAC	TV_Rout: Right audio output to TV port
Rin: Right audio input from audio DAC TV_Rin: Right input from TV SCART	Aux_Rout: Right audio output to auxiliary port

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PIN DESCRIPTIONS (Pins marked N/C should be left unconnected during normal use)

Name	Pin QFN	Pin LQFP	Type	Description
Analog Pins				
ABLANK	2	4	I	Auxiliary Blanking Input: In a typical system, this pin is connected to the RGB status pin (pin 16) from the auxiliary SCART connector.
Aux_R	4	6	I	Auxiliary Red Input: In a typical system, this pin is connected to the RED input pin (pin 15) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_R* output pin.
Aux_G	5	7	I	Auxiliary Green Input: In a typical system, this pin is connected to the GREEN input pin (pin 11) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_G* output pin.
Aux_B	6	8	I	Auxiliary Blue Input: In a typical system, this pin is connected to the BLUE input pin (pin 7) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_B* output pin.
Aux_Fnc	28	37	I/O	Auxiliary Function Pin: This is a bi-directional pin. As an input, it digitizes the analog voltage on the auxiliary SCART function pin (8). As an output, it puts out one of three voltage levels to the auxiliary SCART function pin.
Aux_Cin	----	3	I	Auxiliary Chroma Input: In a typical application, this pin is AC coupled to the Red input line from the Auxiliary SCART connector. When the SVHS mode is selected from the Auxiliary SCART video source, this pin is internally summed to the *Aux_YC* input to generate a composite video signal for the *Mod_YC* output.
Aux_YC	1	2	I	Auxiliary Video Input: In a typical system, this pin is connected to the composite video input pin (pin 20) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_YCout.*
Aux_Lin	11	13	I	Auxiliary Left Audio Input: In a typical system, this pin is connected to the L Audio input pin (pin 6) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_Lout.*
Aux_Rin	12	15	I	Auxiliary Right Audio Input: In a typical system, this pin is connected to the R Audio input pin (pin 2) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_Rout.*
EBLANK	3	5	I	Encoder Blanking Input: In a typical system, this pin is connected to the blanking signal from the external video encoder device.
Enc_R	33	45	I	Encoder Red Input: In a typical system, this pin is connected to the RED output pin from the external video encoder device. This input can be selected as the signal source for the *TV_R* output pin.
Enc_G	32	44	I	Encoder Green Input: In a typical system, this pin is connected to the GREEN output pin from the external video encoder device. This input can be selected as the signal source for the *TV_G* output pin.
Enc_B	31	43	I	Encoder Blue Input: In a typical system, this pin is connected to the BLUE output pin from the external video encoder device. This input can be selected as the signal source for the *TV_B* output pin.

PIN DESCRIPTIONS (Continued)

Name	Pin QFN	Pin LQFP	Type	Description
Enc_YC	34	46	I	Encoder Video Input: In a typical system, this pin is connected to the composite video output pin from the external video encoder device. This input can be selected as the signal source for the *AUX_YCout* and/or *TV_YCout* pins.
Enc_Y	36	48	I	Encoder Luminance Input: In a typical system, this pin is connected to the composite video output pin from the external video encoder device. In SVHS mode, this input can be selected as the signal source for the *TV_YCout* pin and/or the *Aux_YCout* pin.
Enc2_Y	-----	61	I	Encoder 2 Luminance Input: In a typical system, this pin is used as an alternate source for S-video luminance information to a VCR when OSD information is not desired. This input can be selected as the signal source for the *Aux_YCout* pin.
Enc_C	35	47	I	Encoder Chroma Input: In a typical system, this pin is connected to the *TV_R* output pin from the external video encoder device. In the SVHS mode, this input can be selected as the signal source for the *TV_R* pin and/or the *Aux_Cout* output pin.
Enc2_C	-----	63	I	Encoder 2 Chroma Input: In a typical system, this pin is used as an alternate source for S-video chroma information to a VCR when OSD information is not desired. This input can be selected as the signal source for the *Aux_Cout* output pin.
Lin	25	34	I	Left Audio Input: In a typical system, this pin is connected to the left audio output pin of the external audio DAC. This input can be selected as the signal source for the *TV_Lout* and/or *Aux_Lout* pins.
Rin	24	33	I	Right Audio Input: In a typical system, this pin is connected to the right audio output pin of the external audio DAC. This input can be selected as the signal source for the *TV_Rout* and/or *Aux_Rout* pins.
TV_YCin	48	1	I	TV Composite Video input: This pin accepts composite video from the TV SCART. This pin can be selected as the source for the *Aux_YCout* pin.
TV_Lin	9	11	I	TV Left Audio input: This pin accepts audio from the TV SCART. This pin can be selected as the source for the Aux_Lout audio output and the Lout audio output.
TV_Rin	10	12	I	TV Right Audio input: This pin accepts audio from the TV SCART. This pin can be selected as the source for the Aux_Rout audio output and the Rout audio output.
Aux_YCout	46	60	O	Auxiliary Video Output: This pin is the composite video output to the auxiliary SCART connector (pin 19). In the SVHS mode, this pin is the luma output.
Aux_Lout	15	22	O	Auxiliary Left Audio Output: This pin is the output to the left channel audio (pin 3) of the auxiliary SCART connector.
Aux_Rout	22	29	O	Auxiliary Right Audio Output: This pin is the output to the right channel audio (pin1) of the auxiliary SCART connector.
Aux_Mono	18	25	O	Auxiliary Mono Output: This pin is equivalent to the sum of the output signals on *Aux_Lout* and *Aux_Rout*.
BLANK	41	55	O	Blanking output: This output provides the blanking signal to the TV SCART connector (pin 16). This signal is either the blanking signal from the auxiliary SCART connector (*ABLANK*) or the external video encoder (*EBLANK*).
Lout	17	24	O	Left Audio Output: This pin is the output to the left channel audio RCA jack.
Rout	20	27	O	Right Audio Output: This pin is the output to the right channel audio RCA jack.
Mod_Mono	19	26	O	Mono Audio Output: This pin is sum of Lout & Rout to the RF modulator input.

PIN DESCRIPTIONS (continued)

Name	Pin QFN	Pin LQFP	Type	Description
Aux_Cout	47	62	O	Aux Chroma Output: This output provides a chroma signal to the auxiliary SCART connector to support SVHS operation. This pin is typically AC coupled to pin 15 of the auxiliary SCART connector. When the S-video mode is selected, a chroma signal from the video encoder is output to this pin.
Mod_YC	39	53	O	TV Modulator Video Output: This pin provides composite video for an external RF modulator. The signal on this pin follows the composite video output to the *TV_YCout* pin.
TV_YCout	40	54	O	TV Video Output: This pin is the composite video output to the TV SCART connector (pin 19). In the SVHS mode, this pin provides luminance information.
TV_R	42	56	O	TV Red Output: This pin provides Red video to the TV SCART connector (pin 15). In SVHS mode, this pin provides the chroma information.
TV_G	44	58	O	TV Green Output: This pin provides Green video to the TV SCART connector (pin 11).
TV_B	45	59	O	TV Blue Output: This pin provides Blue video to the TV SCART connector (pin 7).
TV_Lout	16	23	O	TV Left Audio Output: This pin is the output to the left channel audio (pin 3) of the TV SCART connector.
TV_Rout	21	28	O	TV Right Audio Output: This pin is the output to the right channel audio (pin1) of the TV SCART connector.
TV_Fnc	27	36	I/O	TV Function Pin: This is a bi-directional pin. As an input, it digitizes the analog voltage on the TV SCART function pin (8). As an output, it puts out one of three voltage levels to the TV SCART function pin.
Digital Pins				
DO_0	----	40	O	Digital Output 0: This pin is a general purpose output that is controlled by serial port register.
DO_1	----	41	O	Digital Output 1: This pin is a general purpose output that is controlled by serial port register.
SCLK	30	39	I	Serial Clock Input: This pin accepts a serial port clock input signal.
SDATA	29	38	I/O	Serial Data Input/Output that can receive or transmit serial data.
POWER/GROUND PINS				
VCC	14,37,43	21, 50, 57	-	+5 VDC power supply pins.
VDD	13,26	20,35	-	+12 VDC power supply pin for function switching circuits.
Vref	7	9	-	Internal voltage reference, bypass pin. Add capacitor 0.1µF(1.0µF for better PSRR) to ground.
GND	23	17, 32, 49, 64	-	Ground for all blocks.
Rbias	8	10	-	Bias point of internal current generator. Add resistor 10.0kΩ(± 1%) to ground.
Tgen	38	51	-	Reference point for internal timing circuit. Add capacitor 470pF to ground.

Note: The exposed pad on the bottom of the 48 QFN package must be grounded.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS
Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage temperature	-55 to 150 °C
Junction operating temperature	+125 °C
5V supply voltage pins	-0.3 V < VCC < 6 V
12V supply pin	-0.3 V < VDD < 13 V
Voltage applied to Digital and Video Inputs	-0.3 V to VCC+0.3 V
Voltage applied to video pins	-0.3 V to VCC+0.3 V
Voltage applied to audio pins	-0.3 V < VDD < 13 V
Voltage applied to FNC pin (input)	-0.3 V < VDD < 13 V
ESD tolerance – SCART pins*	±5 kV
ESD tolerance – other pins	±2.5 kV

* Note: To pass the SCART 15 kV ESD requirement, external protection for the IC is required.

SPECIFICATIONS: Unless otherwise specified: $0° < T_a < 70 °C$; power supplies VCC = +5.0 V ±5%, VDD = 12.0 V ±5%.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Operating Characteristics					
Power Supply Currents (Default register setting)	No signal, video outputs not loaded VCC (+5 VDC) VDD (+12 VDC)		18 17		mA mA
Power Supply Currents (Composite Auxiliary outputs on)	No signal, video outputs not loaded VCC (+5 VDC) VDD (+12 VDC)		28 20		mA mA
PSRR	f_{in} = 100 Hz, 0.3 Vpp on VCC/ VDD	40			dB
Switch time	From rising edge of 8th clock		0.8		μs
Serial Port Timing(Set by I^{2}C controller)					
SCLK Input Frequency				400	kHz
SCLK LOW time (t_{CL})		1.3			μs
SCLK HIGH time (t_{CH})		0.6			μs
Rise time (t_{RT})	*SCLK* and *SDATA*			300	ns
Fall time (t_{FT})	*SCLK* and *SDATA*			300	ns
Data set-up time* (t_{DSU})	*SDATA* change to *SCLK* HIGH	100			ns
Data hold time* (t_{DH})	*SCLK* LOW to *SDATA* change	30			ns
Start set-up time (t_{SSU})		0.6			μs
Start hold time (t_{SH})		0.6			μs
Stop set-up time (t_{PSU})		0.6			μs
Glitch rejection	maximum pulse on *SCLK* and/or *SDATA*			50	ns
* These specifications also apply to an acknowledge generated by the device.					

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SPECIFICATIONS (continued)

Digital I/O Characteristics (SCLK, SDATA)					
Parameter	**CONDITION**	MIN	NOM	MAX	UNIT
High level input voltage		0.7* VCC		VCC+0.3	V
Low level input voltage		GND-0.3		0.3* VCC	V
High level input current (SCLK)	Vin = Vcc - 1.0V	-10		10	µA
High level input current (SDATA)	Vin = Vcc - 1.0V	-50		50	µA
Low level input current (SCLK)	Vin = 1.0V	-10		10	µA
Low level input current (SDATA)	Vin = 1.0V	-50		50	µA
Low level output voltage (SDATA)	I_{OL} = 3 mA			0.4	V
Fall time (t_{FT}) V_{Ihmin} to V_{ILmax} (SDATA)	Acknowledge or read with C_L = 400pF			250	ns
Digital I/O Characteristics (DO_0, DO_1, TV_Fnc, Aux_Fnc)					
Digital output sink current	DO_0, DO_1, Register bits read 0		3.0		mA
Digital output fall time	R_{pullup} = 10 kΩ, C_L = 15 pF		100		ns
Digital output voltage high	R_{pullup} = 10 kΩ, C_L = 15 pF	4.0		VCC	V
Digital output voltage low	R_{pullup} = 10 kΩ, C_L = 15 pF	0		1	V
TV_Fnc or Aux_Fnc output level 10kΩ or higher load to ground	Register 2 = xxxxxx00	0.0	.002	1.2	V
	Register 2 = xxxxxx01	4.9	5.6	6.5	V
	Register 2 = xxxxxx10 or xxxxxx11	10.0	11.7	VDD	V
	Passthrough Mode Register 2 = xxxx11xx				
	0.0 V ≤ Vin ≤ 2.0 V	0.0		2.0	V
	5.1 V ≤ Vin ≤ 7.0 V	4.5		7.0	V
	11.0 V ≤ Vin ≤ VDD V	9.5		VDD	V
TV_Fnc or Aux_Fnc input levels	Read Register = xxxxxx00	0.0		2.0	V
	Read Register = xxxxxx01	4.5		7.0	V
	Read Register = xxxxxx10	9.5		VDD	V
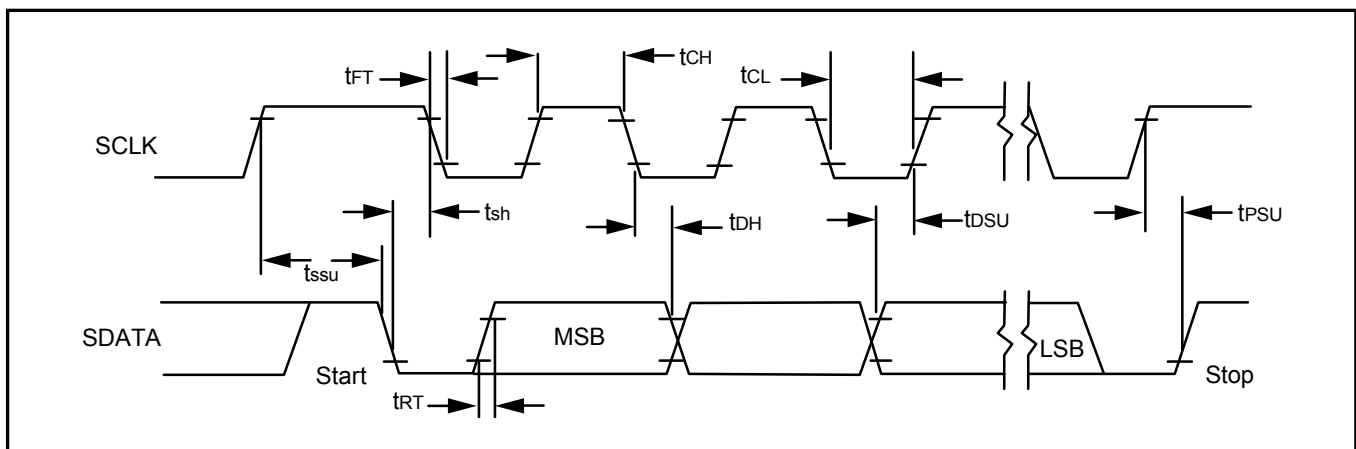
Serial Port Timing (Typical)

Video Characteristics - Unless otherwise noted, typical output loading on all video outputs is 150Ω. All video outputs are capable of withstanding a sustained 75Ω load to ground without damage.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input impedance	All video inputs	100			kΩ
Input dynamic range	f_{in} = 100 kHz, THD < 0.15%		1.5		Vpp
Gain at all video outputs, Except Mod_YC	1.0 Vpp input, f_{in} = 100 kHz	1.9	2.0	2.1	V/V
Gain at Mod_YC	1.0 Vpp input, f_{in} = 100 kHz	0.95	1.0	1.05	V/V
RGB Gain control A_0 = reading xx00xxxx gain	1.0 Vpp input, f_{in} = 100 kHz; Register 2 = xx00xxxx Register 2 = xx01xxxx Register 2 = xx10xxxx Register 2 = xx11xxxx	1.9 A_0 −12% A_0 −22% A_0 −33%	2.0 A_0 −10% A_0 −20% A_0 −30%	2.1 A_0 −8% A_0 −18% A_0 −27%	V/V V/V V/V V/V
Output gain inequality	RGB or SVHS output channel to channel	-2.5		2.5	%
Output DC level Blank level clamp voltage Average level	RGB outputs CVBS or Luma output		1.2		V
	chroma output		1.7		V
Signal to noise ratio	1 Vpp, 100kHz input	58	63		dB
Cross talk	f_{in} = 4.43 MHz, 1 Vpp		-55		dB
Output to output differential delay	RGB signals, f_{in} = 100 kHz	-20		20	ns
Blanking level	Input or output, logical "0"	0.0		0.4	V
	Input or output, logical "1"	1.0		3.0	V
Blanking delay	BLANK to RGB signals	-50		50	ns
Differential phase	TV_YCout, Aux_YCout and Mod_YC	-2.5		2.5	Deg.
Differential gain	TV_YCout, Aux_YCout and Mod_YC	-2.5		2.5	%

Audio Characteristics - Unless otherwise noted, all audio outputs shall drive a load of 10.3 kΩ. All audio outputs will withstand a sustained 300Ω to ground without damage.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input impedance			100		kΩ
Output impedance			10		Ω
Gain	f_{in} = 1.0 kHz, 0 dB settings	0.95	1.0	1.05	V/V
Frequency response	0.5 Vrms input, Flat within ± 0.3 dB	20			kHz
	Measured -3 dB point	100			kHz
Dynamic Range A Weighting filter	f_{in} = 1.0 kHz, 2.0 Vrms; Register 4 = xxxxxx11	90			dB

Audio Characteristics – Cont. (THD* spec. at 1 kHz frequency and 0 dB DAC Input gain and Volume Control settings)

PARAMETER	CONDITION		MIN	NOM	MAX	UNIT
Signal to Noise ratio A Weighting filter	f_{in} = 1.0 kHz, 2.0 Vrms; Register 4 = xxxxxx11		90			dB
Distortion (THD)* Aux_Lin/Aux_Rin to all outputs	Bypass Volume Control	0.5 Vrms output			0.1	%
		2.0 Vrms output			0.1	%
	Pass through Volume Control	0.5 Vrms output			0.1	%
		2.0 Vrms output			0.1	%
Distortion (THD)* Lin/Rin to Lout/Rout, TV_Lout/TV_Rout and Mod_Mono	Bypass Volume Control	0.5 Vrms output			0.1	%
		2.0 Vrms output			0.1	%
	Pass through Volume Control	0.5 Vrms output			0.1	%
		2.0 Vrms output			0.1	%
Distortion (THD)* Lin/Rin to Aux_Lout, Aux_Mono and Aux_Rout	Independent of Volume Control	0.5 Vrms output			0.1	%
		2.0 Vrms output			0.1	%
Distortion (THD)* TV_Lin/TV_Rin to all outputs	Independent of Volume Control	0.5 Vrms output			0.1	%
		2.0 Vrms output			0.1	%
DC Offset at Aux Outputs Aux_Lout, _Rout and _Mono			-55		45	mV

DC Offset at TV & Line Outputs
   TV_Rout, TV_Lout, Rout,
   Lout and Mod_Mono
	Bypass Volume Control		-55		45	mV

	Volume Control Active, 0 dB gain		-100		60	mV
	Volume Control Active, 6 dB gain		-140		120	mV
Output phase matching	f_{in} = 1.0 kHz, 0.5 Vrms; any stereo pair			0.5		Deg.
Stereo separation any stereo pair	f_{in} = 1.0 kHz, 2.0 Vrms		85			dB
Crosstalk (Any combination)	f_{in} = 1.0 kHz, 2.0 Vrms		75			dB
DAC Input Gain	Register 3 xxxx00xx			0		dB
	xxxx01xx			6		dB
	xxxx10xx			9		dB
	xxxx11xx			11.5		dB

Output attenuation (volume control)
 	
At TV_Lout/TV_Rout, Lout/Rout
And Mod_Mono
	Reg. 0=x0000000 (0 dB attenuation)
	   Register 4 = 00000000
	   Register 4 = 00000100
				0
				6
						dB
						dB

	Reg. 0=x0011111 (31 dB attenuation)
	   Register 4 = 00000000
	   Register 4 = 00000100
				-31
				-25
						dB
						dB

	Reg. 0=x0111111 (63 dB attenuation)
	   Register 4 = 00000000
	   Register 4 = 00000100
				-63
				-57
						dB
						dB

	Register 0 = x1xxxxxx (MUTE) Register 4 = 00000000			-75		dB
Attenuation accuracy	Register 0 = 00000100 to 00011111		-5		5	%
Attenuation accuracy	Register 0 = 00000001 to 00000011		-10		10	%
Audio to video path skew	Video input = 1.0 Vpp @ 100kHz Audio input = 0.5 Vrms @ 1.0kHz			1.5		µs

Applications Diagram:
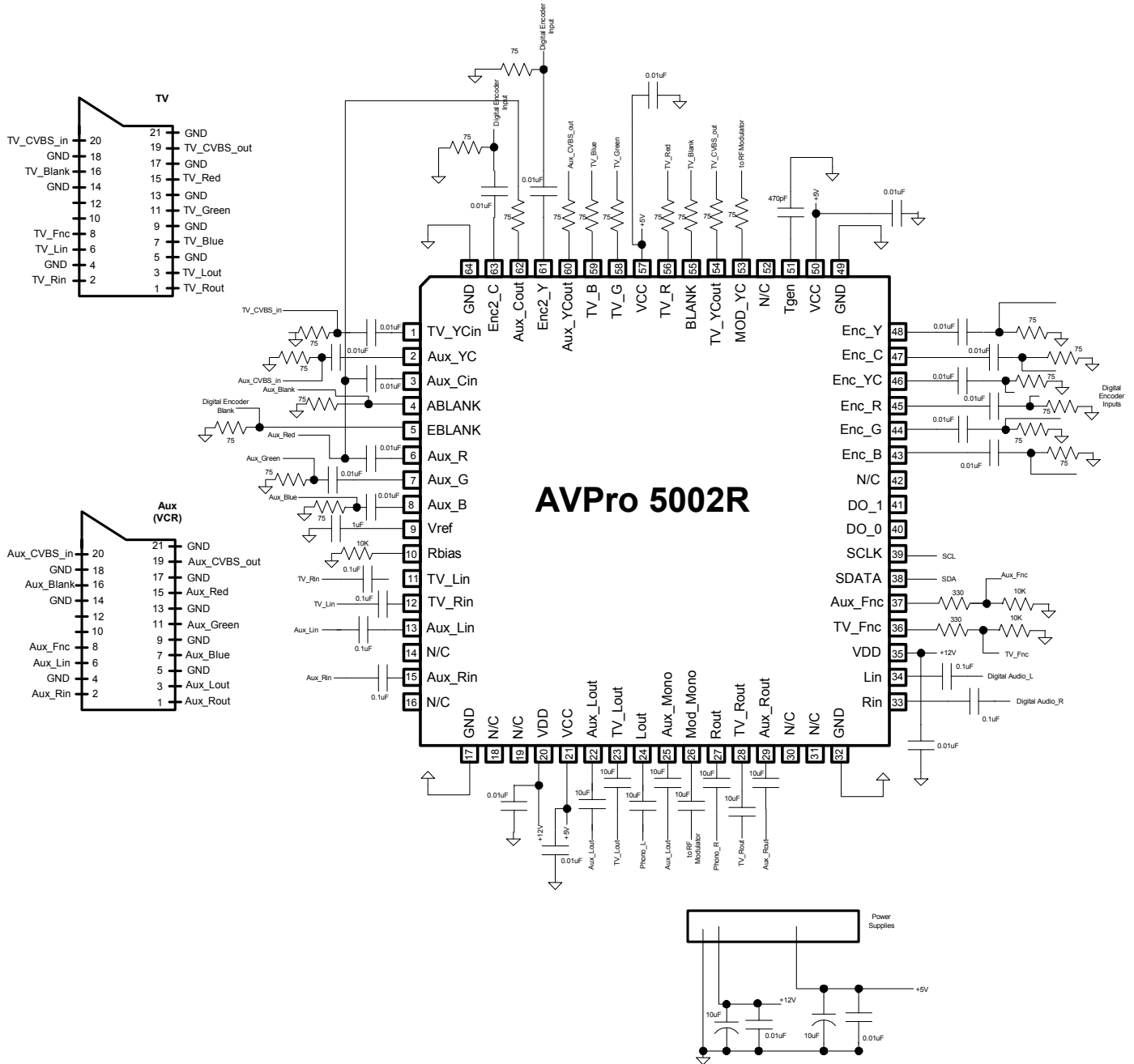
Applications Information

Function Pin Control

The AVPro® 5002R controls the output voltage of the Aux_FNC and TV_Fnc pins with the same register bits. In some applications (such as BskyB), independent control of these output voltages is required. An external circuit pictured below that will allow independent control. The internal register bits should be used to control the Aux_Fnc pin as this pin is typically bi-directional. The control for the TV_Fnc pin is then controlled by the external circuit. The DO_0 and DO_1 pins are used to switch two external transistors to create the three different voltage levels. The 150Ω resistor is used to limit the current through Q2. With a SCART load of 10kΩ, the voltage at the TV_Fnc pin is as follows:

DO_0 = 0, DO_1 = 0; TV_Fnc = 10.9V

DO_0 = 1, DO_1 = 0; TV_Fnc = 5.7V

DO_0 = 0, DO_1 = 1; TV_Fnc = 0.0V
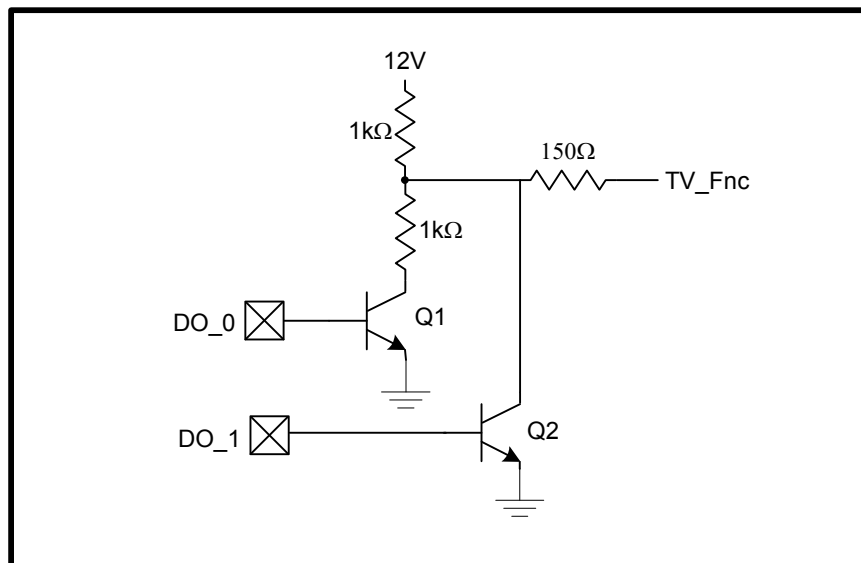
Note: DO_0 and DO_1 are not available on the 48 QFN package.

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AUXILIARY Red / Chroma Bi-directional Operation:

For the TV source selection of Auxiliary RGB (Register 1 xxxxx001) and S- video (Register 1 xxxxx101), the output driver on the *Aux_Cout* pin acts as part of the load for the RED/Chroma signal input on pin 15 of the SCART connector. In order to get the correct 75Ω load impedance, the *Aux_Cout* amplifier needs either a DC bias, an extra resistance to ground, or a FET pulldown.

1). To select an internal DC bias for the *Aux_Cout* amplifier, the Aux A/V source should be set for S-video mode (SVHS Enc 1, Enc 2, Enc 3 or Enc 4) per the following table. This puts 0.9 VDC bias at the input, or about 1.8V at the *Aux_Cout* pin, and 0.9V at the auxiliary SCART connector when terminated (driven) in a 75Ω system. Therefore, the outputs of the external video encoder must be disabled in this mode in order to prevent corruption of the incoming RED/Chroma video signal.

2). As an alternative, to select a 0V DC bias for the *Aux_Cout* amplifier, the Aux A/V source should select one of the Composite modes (Enc1, ENC2 or TV) or Aux mute in the following table. In this mode, the internal amplifier bias set to 0V, but amplifier is a weak pulldown. The amplifier is biased between ground and +5V, as such, the output impedance of the *Aux_Cout* is around 100Ω including the 75Ω series resistor. A shunt resistor of 330 to 470 Ω will compensate, but will slightly lower the Aux_Cout chroma signal.

3). Another option is to add a FET with ~20Ω series resistor from the *Aux_Cout* to ground. Select 0VDC bias for the *Aux_Cout* amplifier, and bias the FET in the "ON" or conducting state. The Aux A/V source should select one of the Composite modes (Enc1, ENC2 or TV) or Aux mute. See the Register 1: Audio/Video Control bit table for settings. This method will compensate for the *Aux_Cout* pin pulldown, and not significantly reduce the Aux_Cout chroma signal.
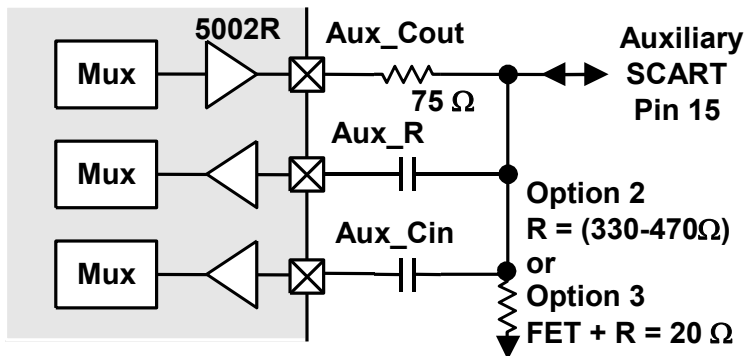
Note: Aux_Cin is not available on the 48QFN package

HOT-PLUG OF SCART CONNECTORS

Semiconductor ICs can be sensitive to discharges caused by floating chassis grounds between audio/video equipment. This is observed when the SCART cables are repeatedly connected and disconnected while the ICs are powered on inside the IRD. When the SCART cable is unplugged, an AC potential can exist between equipment. When the SCART cable is plugged back into the IRD, the AC potential discharges through the SCART connector. If the discharge occurs through the shield of the SCART connector or the ground pins, there is no problem. If the discharge occurs through the signal pins, semiconductor devices can experience potential issues. These issues will occur if the pulse created by the discharge has a fast rising edge, typically a few hundred pico-seconds. This is an order of magnitude faster than a standard ESD pulse so the internal ESD diodes of ICs will not respond fast enough to protect the device. This issue can be resolved by placing a small shunt capacitor on each SCART I/O pin. The capacitor slows the rising edge of the discharge pulse and allows the internal ESD diodes to react to the discharge. An exact value should be calculated for each signal line depending upon the signal type so as to avoid roll-off of the intended signal. (see Equivalent Circuit section)
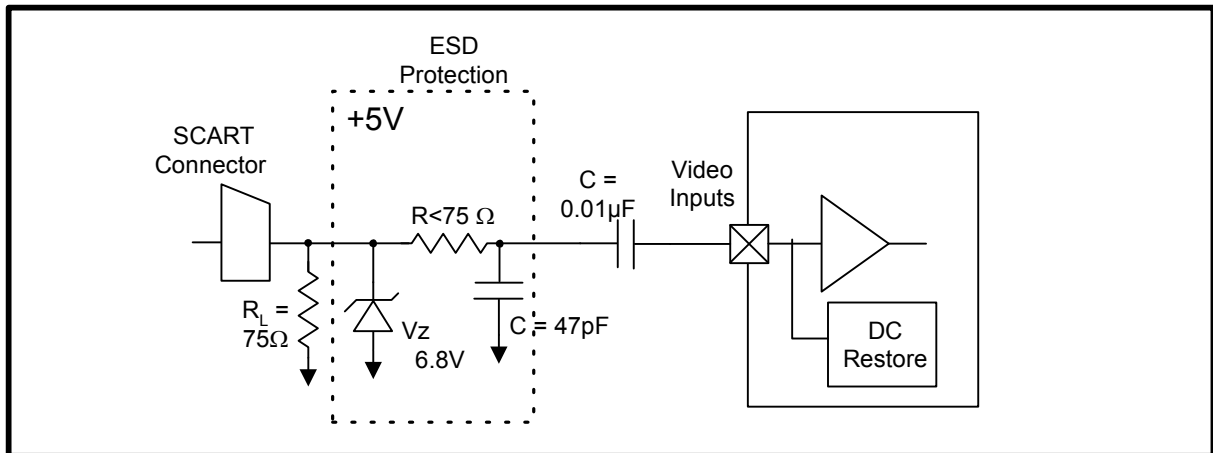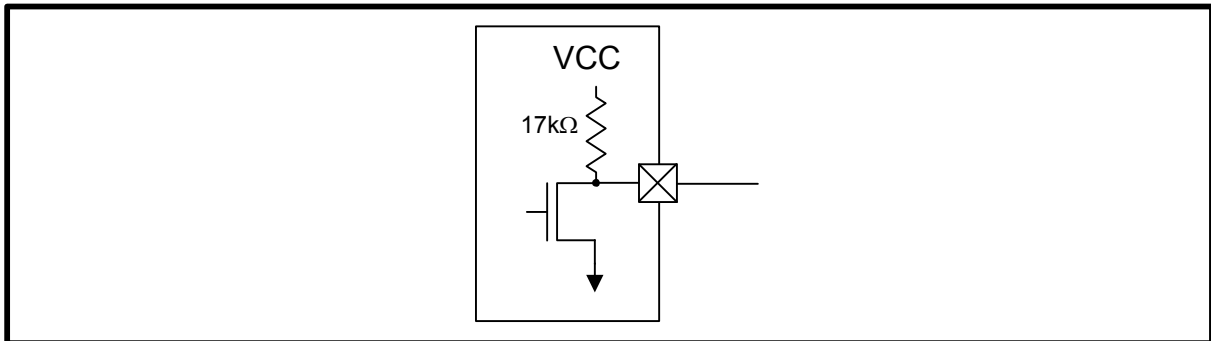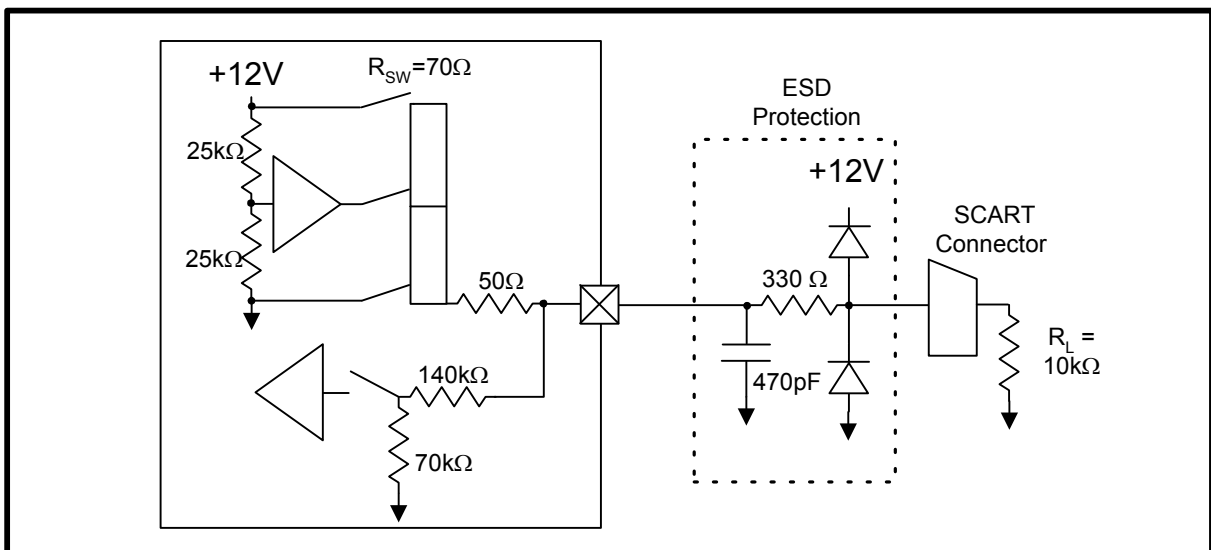
Equivalent Circuits:
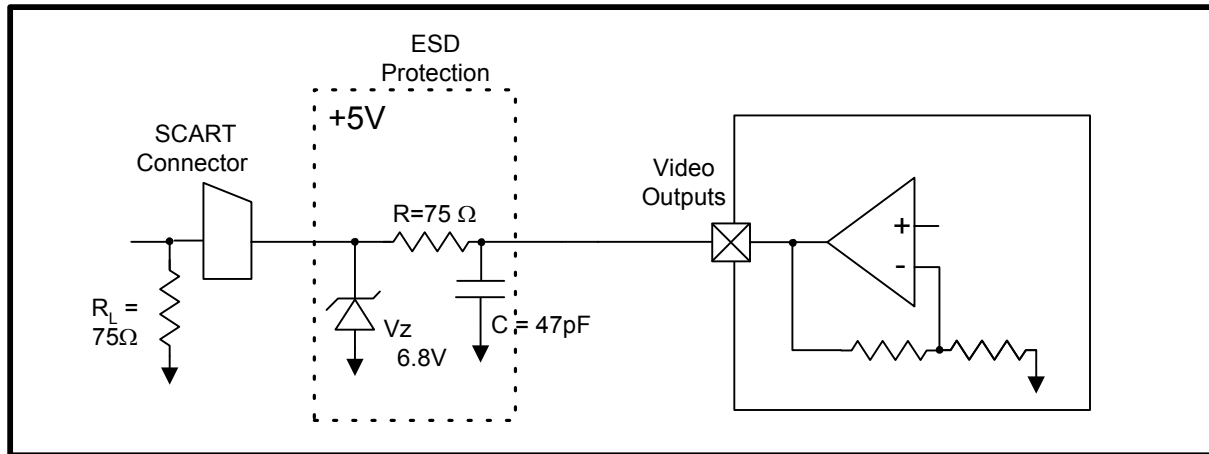
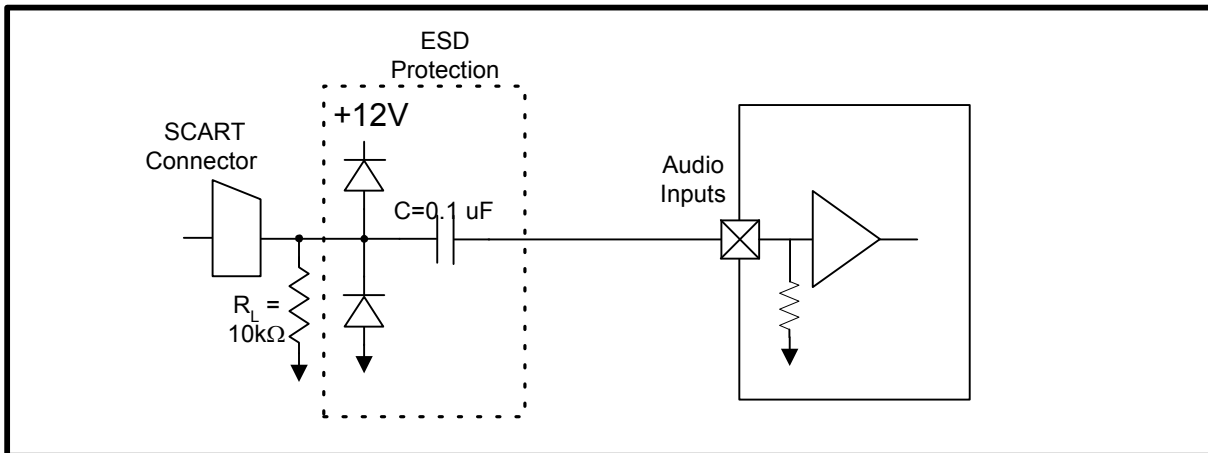**Video Output Circuit**
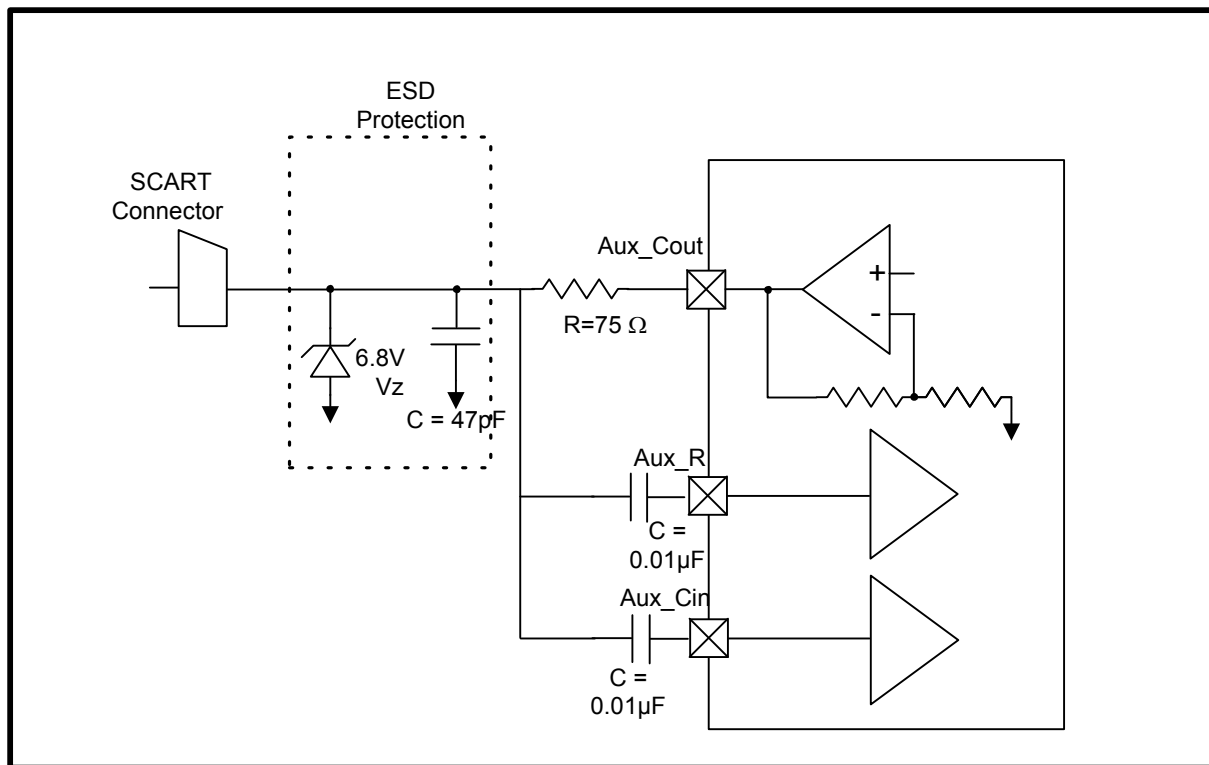
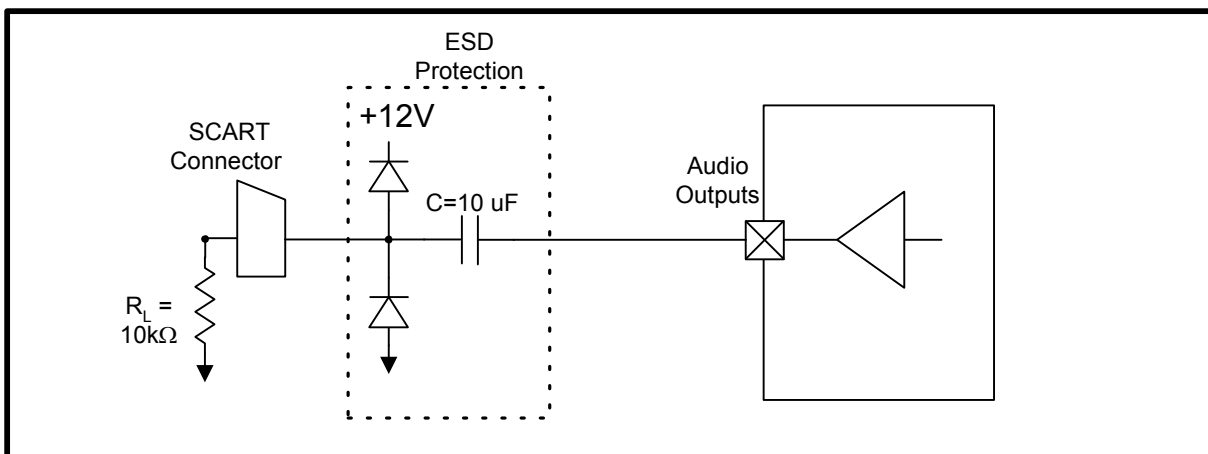**Auxiliary SCART pin 15 Circuit**

Video Input Circuit

Digital Output Circuit

AUX and TV Function Switching Circuit

Audio Input Circuit

Audio Output Circuit

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PACKAGE PIN DESIGNATION

(Top View)
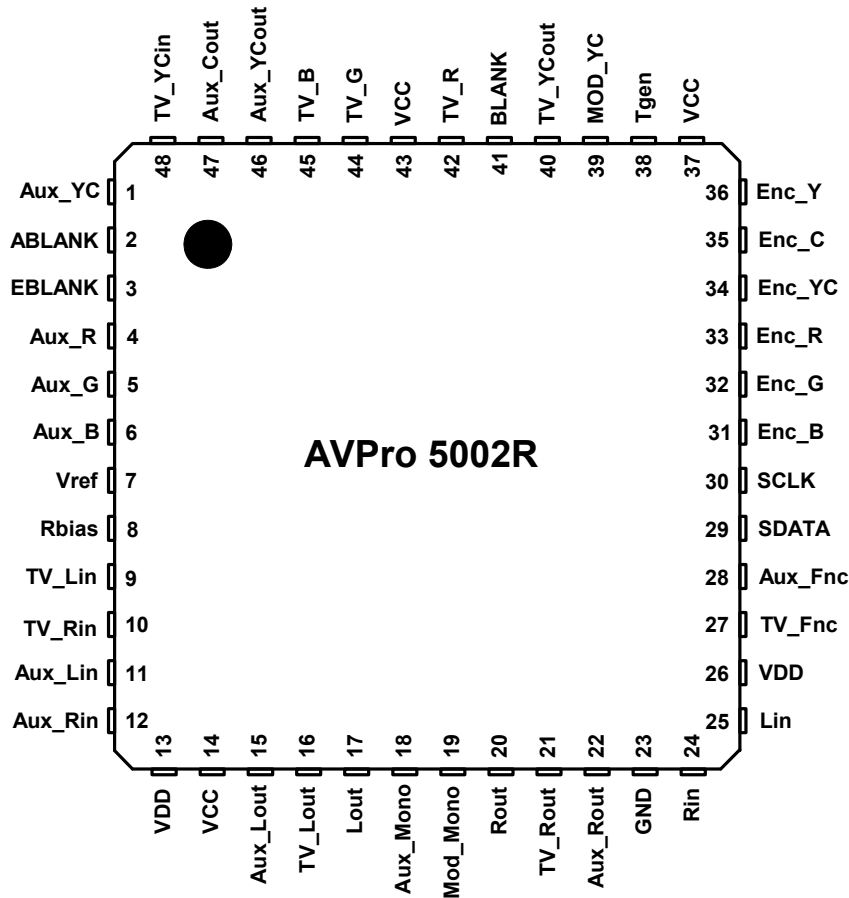
AVPRO® 5002R-CM (JEDEC 48 QFN)

MECHANICAL DRAWING (48 QFN)

TOP VIEW

SIDE VIEW

BOTTOM VIEW

© 2008 TERIDIAN Semiconductor Corporation
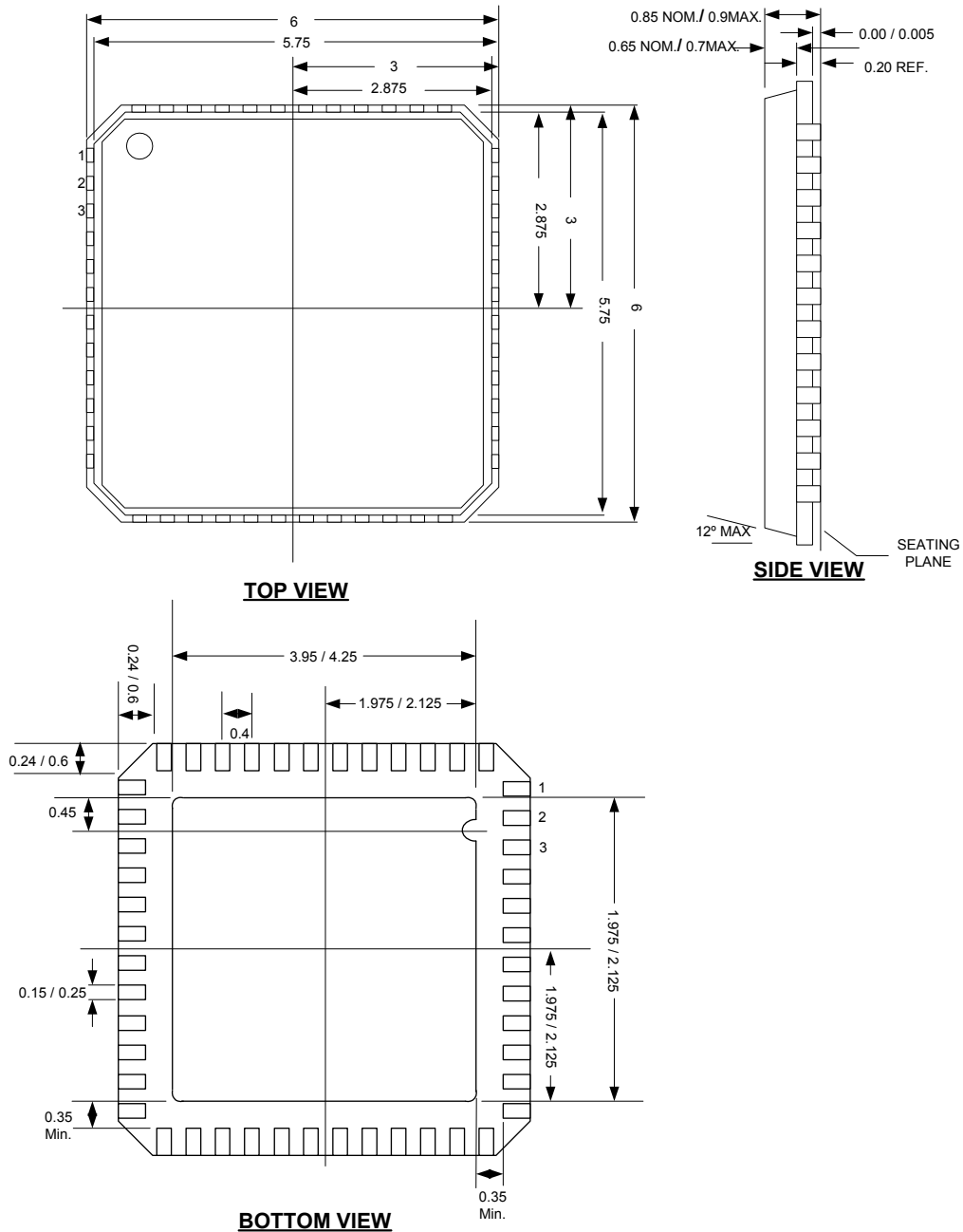
RECOMMENDED PCB LAND PATTERN DIMENSIONS
48 Pin - QFN
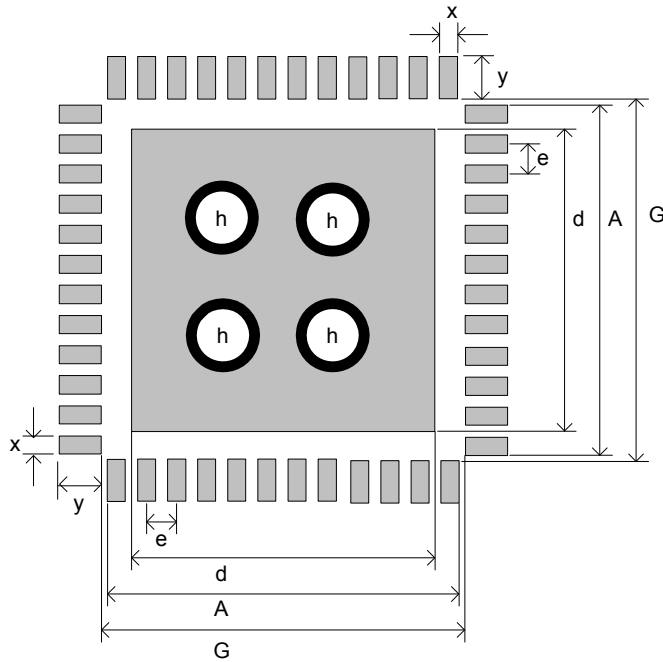
Recommended PCB Land Pattern Dimensions

SYMBOL	DESCRIPTION	MIN	TYP	MAX
e	Lead pitch		0.4 mm	
x			0.25 mm	0.28 mm
y			0.6 mm	
d			4.1 mm	
A			4.65 mm	
G			5.1 mm	
h	Via diameter, see Note 1		0.3 mm	

Note 1: Provide thermal pad with solid via connection to the ground plane. Vias should be incorporated with a 1.2mm pitch.

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PACKAGE PIN DESIGNATION

(Top View)
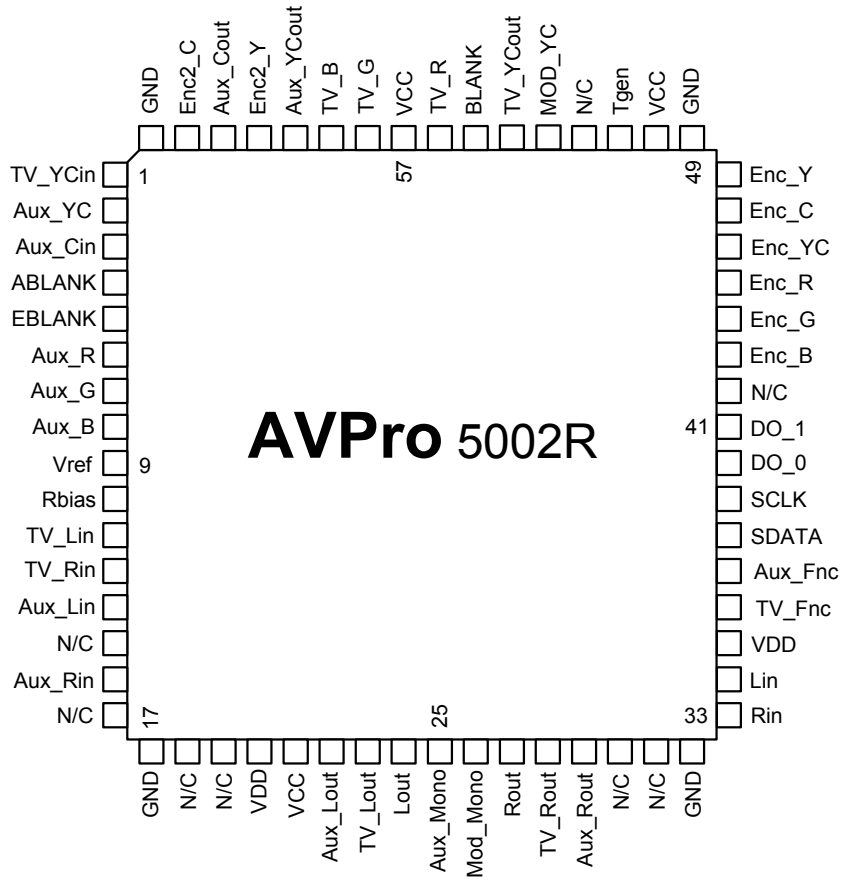
AVPro® 5002R-CGT (JEDEC 64 PIN LQFP)

MECHANICAL DRAWING
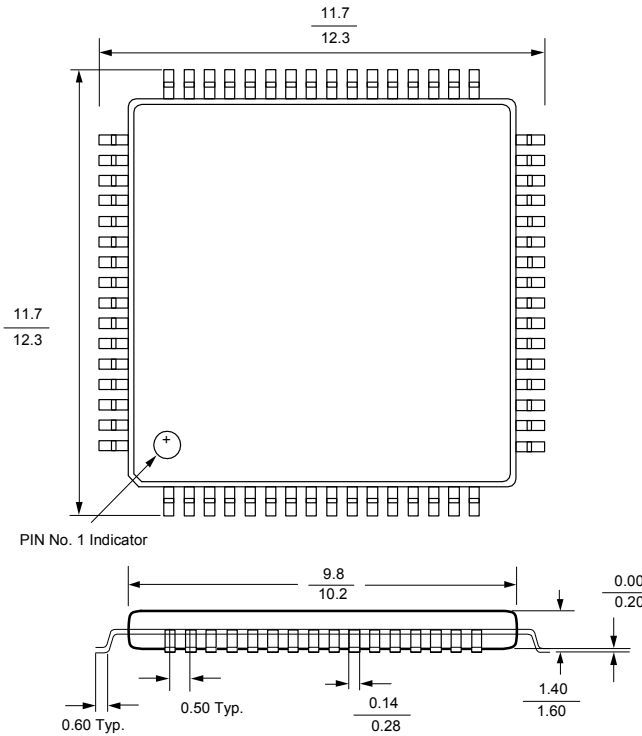
64-Lead Low Profile Plastic Quad Flatpack Package (JEDEC LQFP)

Note: Controlling dimensions are in mm.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
AVPro® 5002R Dual SCART A/V Switch (64 LQFP)	AVPro 5002R-CGT	AVPro 5002R 5002R-CGT
AVPro® 5002R Dual SCART A/V Switch (64 LQFP) Tape / Reel	AVPro 5002R-CGTR	AVPro 5002R 5002R-CGT
AVPro® 5002R Dual SCART A/V Switch (64 LQFP) Lead Free	AVPro 5002R-CGT/F	AVPro 5002R 5002R-CGT
AVPro® 5002R Dual SCART A/V Switch (64 LQFP) Lead Free, Tape / Reel	AVPro 5002R-CGTR/F	AVPro 5002R 5002R-CGT
AVPro® 5002R Dual SCART A/V Switch (48 QFN)	AVPro 5002R-CM	AVPro5002R
AVPro® 5002R Dual SCART A/V Switch (48 QFN) Tape / Reel	AVPro 5002R-CMR	AVPro5002R
AVPro® 5002R Dual SCART A/V Switch (48 QFN) Lead Free	AVPro 5002R-CM/F	AVPro5002R
AVPro® 5002R Dual SCART A/V Switch (48 QFN) Lead Free, Tape / Reel	AVPro 5002R-CMR/F	AVPro5002R

 Rev 2.1

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