Military 10H610

Dual 3-Input 3-Output "OR" Gate

ELECTRICALLY TESTED PER:
5962-8754101

The 10H610 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the 10H610 particularly useful in clock distribution applications where minimum clock skew is desired.

- Propagation Delay, 1.0 ns Typical
- 230 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	GND
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	GND
B_{OUT}	12	16	15	51 Ω to V_{TT}
B_{OUT}	13	1	17	51 Ω to V_{TT}
B_{OUT}	14	2	18	51 Ω to V_{TT}
V_{CC1}	15	3	19	GND
V_{CC2}	16	4	20	GND

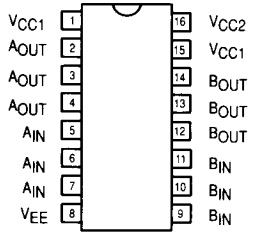
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

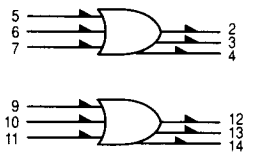
1) JAN: N/A
2) SMD: 5962-8754101
3) 883: 10H610/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

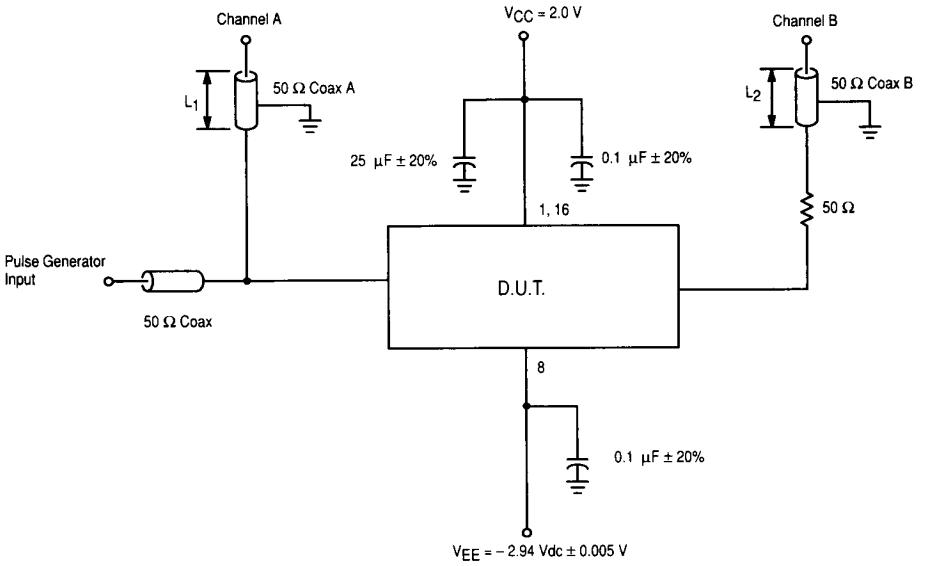
The letter "M" appears before the slash on LCC.

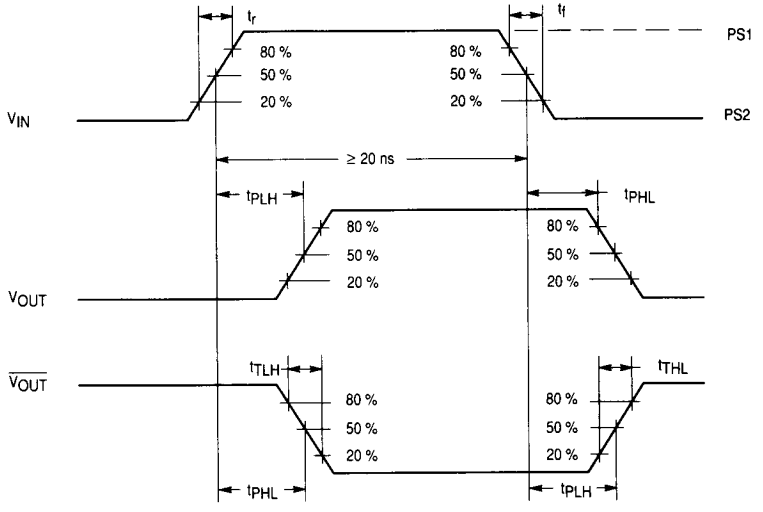


LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8





NOTES

1. All other outputs are loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. L_1: L_2: Matched for equal time delay.
4. V_{IN} = has the following characteristics:
   a. pulse width = ≥ 20 ns.
   b. frequency = 1.0 MHz.
   c. $t_r = t_f$ = 1.0 ns (20% – 80%) + 0.1 ns.

Figure 1. Test Circuit

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+0.28	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 1.01	− 0.78	− 0.86	− 0.65	− 1.06	− 0.84	V	5 - 7 9 - 11				8		1, 16, 5	2 - 4, 12 - 14
V_{OL}	Low Output Voltage	− 1.95	− 1.58	− 1.95	− 1.565	− 1.95	− 1.61	V		5 - 7 9 - 11			8		1, 16, 5	2 - 4, 12 - 14
V_{OL1}	Low Output Voltage	− 1.95	− 1.58	− 1.95	− 1.565	− 1.95	− 1.61	V				5 - 7 9 - 11	8	8	1, 16, 5	2 - 4, 12 - 14
V_{OH1}	High Output Voltage	− 1.01	− 0.78	− 0.86	− 0.65	− 1.06	− 0.84	V			5 - 7 9 - 11		8	8	1, 16, 5	2 - 4, 12 - 14
I_{IH1}	Input Current High		450		720		720	µA	5 - 7 9 - 11				8		1, 16, 5	5 - 7, 9 - 11
I_{IL1}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 11			8		1, 16, 5	5 - 7, 9 - 11
I_{EE}	Power Supply Drain Current	− 38		− 42		− 42		mA					8		1, 16, 5	8

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T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.75	1.8	0.7	1.9	0.65	1.75	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14
t_{THL}	Fall Time	0.75	1.8	0.7	1.9	0.65	1.75	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14
t_{PLH}	Propagation Delay	0.8	1.65	0.9	1.9	0.75	1.85	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14
t_{PHL}	Propagation Delay	0.55	1.7	0.6	1.95	0.5	1.6	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14