VECTRON INTERNATIONAL
A DOVER COMPANY

Helping Customers Innovate, Improve & Grow

VM-702

Description

Vectron's VM-702 Crystal Oscillator is a silicon based MEMS stabilized, differential output oscillator, operating off a 2.5 or 3.3 volt supply in a hermetically sealed 5x7 plastic package.
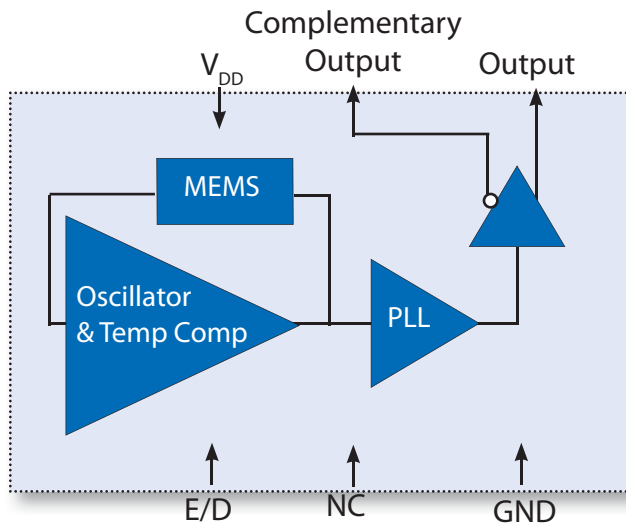
Features

• High Shock MEMS based Oscillator
• 10.00-460.0000MHz Output Frequencies
• Low Power
• Differential Output
• Enable/Disable
• 2.25V to 3.6V Operation
• -20/70°C or -40/85°C Operation

• Product is compliant to RoHS directive Pb
  and fully compatible with lead free assembly

Applications

• PCI Express
• Ethernet, GbE, Synchronous Ethernet
• Fiber Channel
• Enterprise Servers
• Telecom
• Clock source for A/D's, D/A's
• Driving FPGA's
• Test and Measurement
• PON
• Medical
• COTS

Block Diagram

Performance Specifications

Table 1. Electrical Performance, HCSL Output

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.25		3.60	V
Current (No Load)	I_{DD}			42	mA
Frequency					
Nominal Frequency	f_N	10		460	MHz
Stability[2] (Ordering Options)			±10, ±25, ±50		ppm
Outputs					

Output Logic Levels
  Output Logic High
  Output Logic Low
	V_{OH}
	V_{OL}
		0.725		0.1	V
					V

Output Rise and Fall Time[3]
  Rise Time
  Fall Time
	t_R
	t_F
				400
				400
					ps
					ps

Load		50 ohms to ground			
Duty Cycle[4]		48		52	%
Jitter (200 kHz - 20 MHz) 156.250MHz[5] 12kHz-20MHz	ϕJ		280 1.7		fs ps

Period Jitter[6]
  RMS
  P/P
	ϕJ		3.9
			28
					ps
					ps

Enable/Disable					
Output Enabled[7] Output Disabled	V_{IH} V_{IL}	$0.75*V_{DD}$		$0.25*V_{DD}$	V V
Disable Time	t_D			5	ns
Enable/Disable Leakage Current	$I_{E/D}$			±200	uA
Start-Up Time	t_{SU}			5	ms
Operating Temp. (Ordering Option)	T_{OP}		-10/70 or -40/85		°C
Package Size			5.0 x 7.0 x 0.9		mm

1. The VM-702 power supply pin should be filtered, e.g., a 0.1 and 0.01uf capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 1 defines the test circuit and Figure 2 defines these parameters.
4. Duty Cycle is defined as the On Time/Period.
5. Measured using an Agilent E5052.
6. Measured using a Wavecrest SIA3300C, 90K samples.
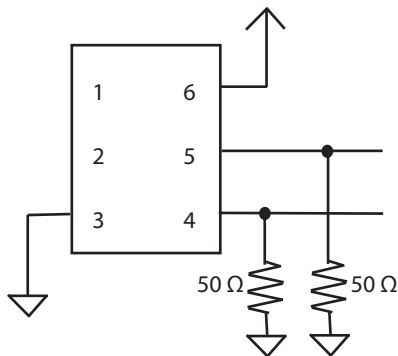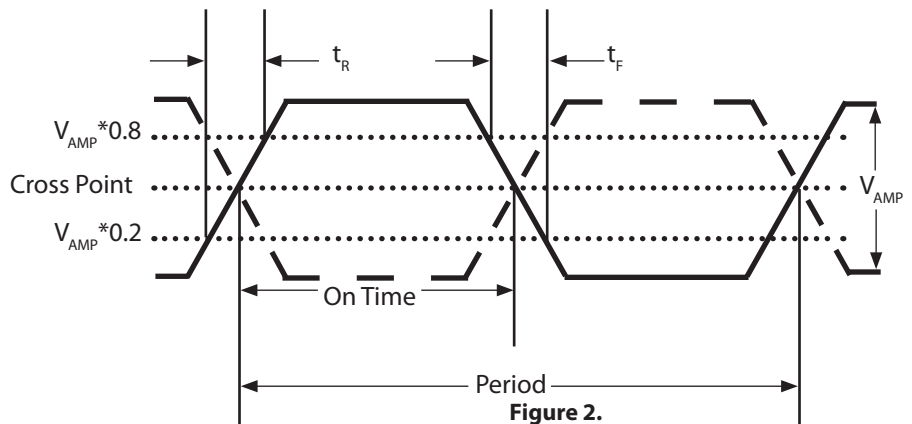7. Outputs will be Enabled if the Enable/Disable pad is left open.

Figure 1.

Figure 2.

Performance Specifications

Table 2. Electrical Performance, LVPECL Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.25		3.60	V
Current (No Load)	I_{DD}			32	mA
Frequency					
Nominal Frequency	f_N	10		460	MHz
Stability[3] (Ordering Option)			±10, ±25, ±50		ppm
Outputs					

Output Logic Levels[4]
  Output Logic High
  Output Logic Low
	V_{OH}
	V_{OL}
		V_{DD}-1.08		V_{DD}-1.555	V
					V

Output Rise and Fall Time[3]	t_R/t_F				ps
Load		50 ohms into V_{DD}-1.3V			
Duty Cycle[4]		48		52	%

Jitter, 156.250MHz[5]
  200kHz-20MHz
  12kHz -20MHz
	ϕJ		280
			1.7
					fs
					ps

Period Jitter[6]
  RMS
  P/P
	ϕJ		3.9
			28
					ps
					ps

Enable/Disable					
Output Enabled[7] Output Disabled	V_{IH} V_{IL}	$0.75*V_{DD}$		$0.25*V_{DD}$	V V
Disable Time	t_D			5	ns
Enable/Disable Leakage Current				±200	uA
Start-Up Time	t_{SU}			5	ms
Operating Temp. (Ordering Option)	T_{OP}		-10/70 or -40/85		°C
Package Size			5.0 x 7.0 x 0.9		mm

1. The VM-702 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 3 defines the test circuit and Figure 4 defines these parameters.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a Wavecrest SIA3300C, 90K samples.
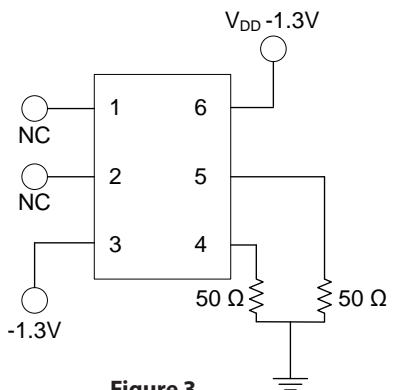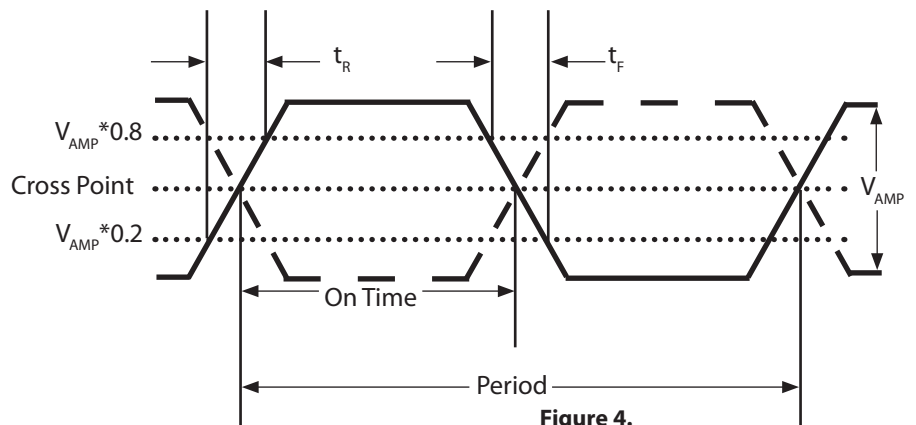7. Outputs will be Enabled if Enable/Disable is left open.

Figure 3.

Figure 4.

Table 3. Electrical Performance, LVDS Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.25		3.60	V V
Current (No Load)	I_{DD}			60	mA
Frequency					
Nominal Frequency	f_N	10		460	MHz
Stability[2] (Ordering Option)			±10, ±25, ±50		ppm
Outputs					
Output Logic Levels[3] Output Logic High Output Logic Low	V_{OH} V_{OL}	 0.9	 1.43 1.10	 1.6	 V V
Differential Output Amplitude		250	350	450	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.4	V
Offset Voltage Error				50	mV
Output Leakage Current				10	uA
Output Rise and Fall Time[3]	t_R/t_F			400	ps
Load			100 ohms differential		
Duty Cycle[4]		48	50	52	%
Jitter, 156.250MHz[5] 200kHz -2 0MHz 12kHz - 20MHz	ϕJ		 280 1.7		 fs ps
Period Jitter[6] RMS P/P	ϕJ		 3.9 28		 ps ps
Enable/Disable					
Output Enabled[7] Output Disabled	V_{IH} V_{IL}	$0.75 \times V_{DD}$		 $0.25 \times V_{DD}$	V V
Disable Time	t_D			5	ns
Enable/Disable Leakage Current	$I_{E/D}$			±200	uA
Start-Up Time	t_{SU}			5	ms
Operating Temp. (Ordering Option)	T_{OP}		-10/70 or -40/85		°C
Package Size			5.0 x 7.0 x 0.9		mm

1. The VM-702 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 5 defines these parameters and Figure 4 defines the test circuit.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a Wavecrest SIA3300C, 90K samples.
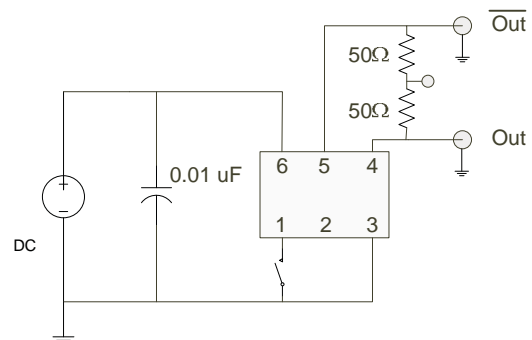7. Outputs will be Enabled if Enable/Disable is left open.

Figure 5.

Package and Pinout

Table 4. Pinout

Pin #	Symbol	Function
1	E/D or NC	Enable/Disable
2	NC	No Connection
3	GND	Electrical and Lid Ground
4	f_O	Output Frequency
5	Cf_O	Complementary Output Frequency
6	V_{DD}	Supply Voltage

Contact Pads are
Gold flash (0.003 um min) over
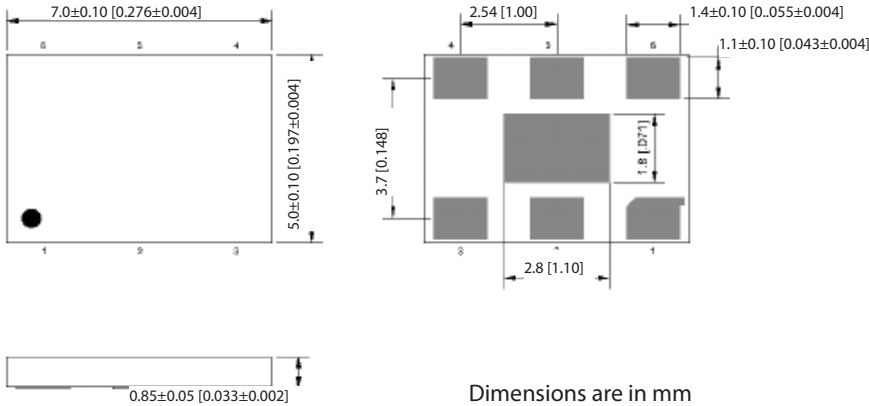Palladium (0.01-0.15um) over
Nickel (0.508-2.032um)

Power Supply cap
is required

Figure 6. Package Outline Drawing

Dimensions are in mm

Figure 7. Pad Layout
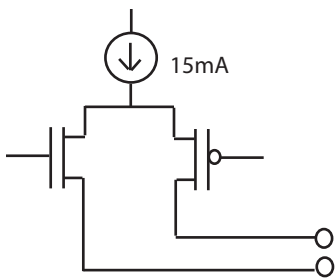
HCSL Application Diagrams

Figure 8.
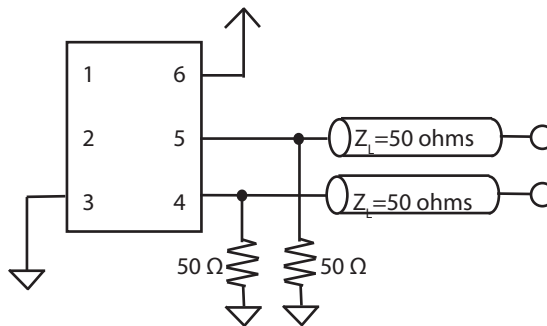**Standard HCSL Output Configuration**
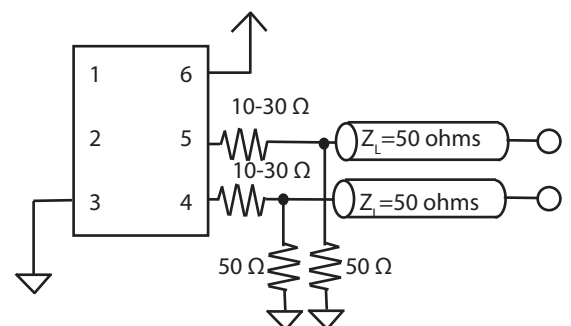
Figure 9.
Single Resistor Termination Scheme

Figure 10.
In some cases a 10-30 ohm series resistor is used to help reduce overshoot.

The VM-702 incorporates a standard High Speed Current Logic, HCSL ,output scheme which is a 15mA current source switched between Out and Complementary Out. Being un-terminated drains, as shown in Figure 8, they require external 50 ohm resistors to ground as shown in Figure 9. HCSL is a high impedance output with quick switching times, in can be advantageous to use a 10 to 30 ohm series resistor as shown in Figure 10, to help reduce overshoot/ringing.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.
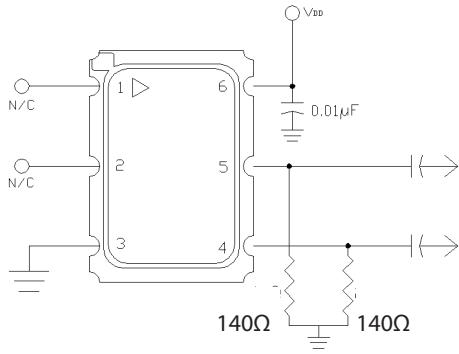
LVPECL Application Diagrams

Figure 11. Single Resistor Termination Scheme
Resistor values are typically 140 ohms for 3.3V operation
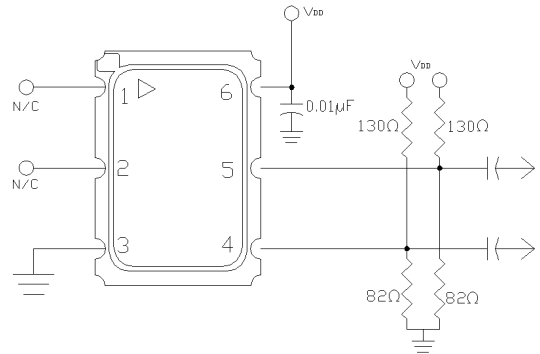and 82.5ohms for 2.5V operation.

Figure 12. Pull-Up Pull Down Termination
Resistor values are typically for 3.3V operation
For 2.5V operation, the resistor to ground is 62
ohms and the resistor to supply is 250 ohms

The VM-702 incorporates a standard LVPECL output scheme, which are un-terminated emitters as shown in Figure 8. There are numerous application notes on terminating and interfacing LVPECL logic and the two most common methods are a single resistor to ground, Figure 9, and a pull-up/pull-down scheme as shown in Figure 10. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.
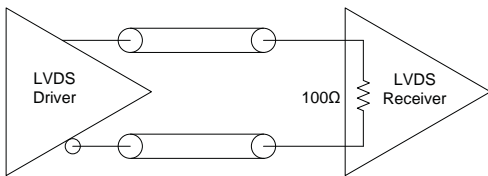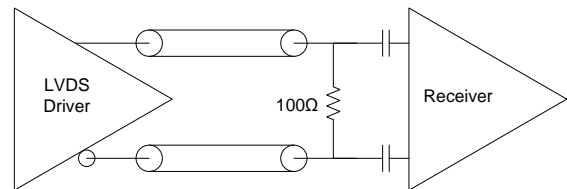
LVDS Application Diagrams

Figure 13. LVDS to LVDS Connection, Internal 100ohm

Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.

**Figure 14. LVDS to LVDS Connection
External 100ohm and AC blocking caps**

Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

Environmental and IR Compliance

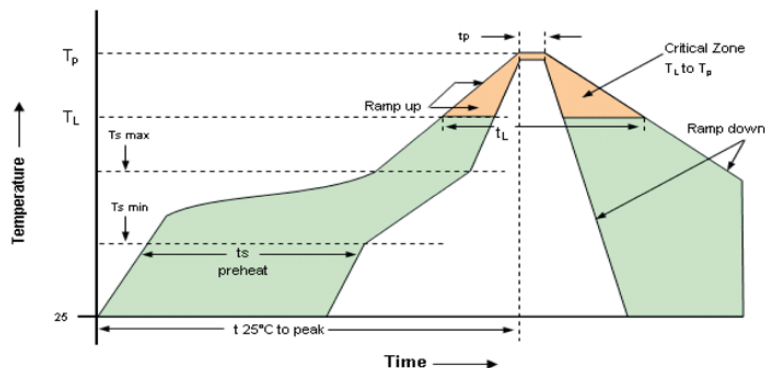| Table 5. Environmental Compliance			
Parameter	Condition		
Mechanical Shock	MIL-STD-883 Method 2002		
Mechanical Vibration	MIL-STD-883 Method 2007		
Temperature Cycle	MIL-STD-883 Method 1010		
Solderability	MIL-STD-883 Method 2003		
Fine and Gross Leak	MIL-STD-883 Method 1014		
Resistance to Solvents	MIL-STD-202 Method 215		
Moisture Sensitivity Level	MSL1		

IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 6. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 6. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	ts	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	tL	150 sec Max
Time to Peak Temperature	tAMB-P	480 sec Max
Time at 260°C	tP	30 sec Max
Time at 240°C	tP2	60 sec Max
Ramp down	R_{DN}	6°C/sec Max

Solderprofile:

Maximum Ratings, Tape & Reel

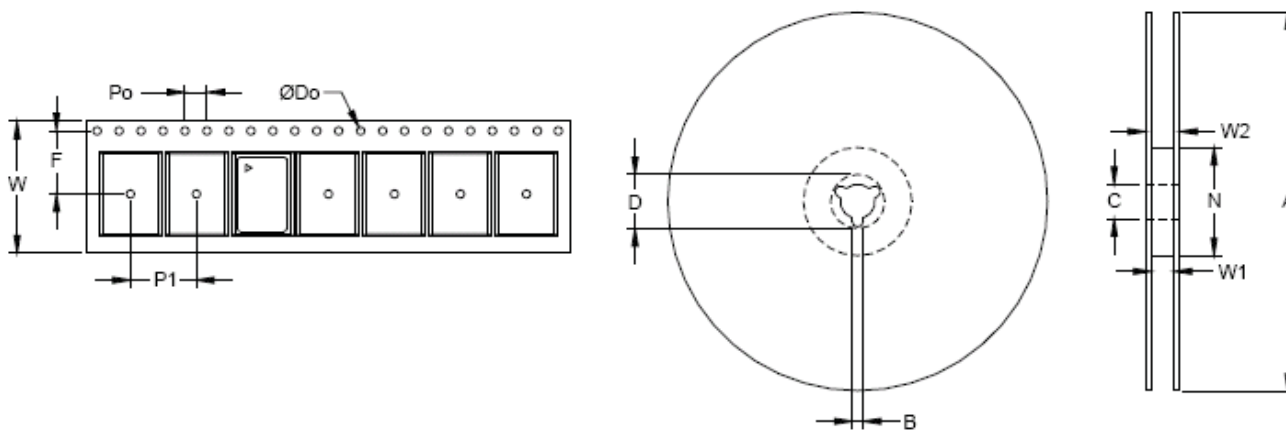**Absolute Maximum Ratings and Handling Precautions**

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Although ESD protection circuitry has been designed into the VM-702, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Table 7. Maximum Ratings		Unit
Parameter		
Storage Temperature	-55 to 125	°C
Junction Temperature	150	C
Supply Voltage	-0.5 to 5.0	V
Enable Disable Voltage	-0.5 to V_{DD}+0.5	V
ESD, Human Body Model	1500	V
ESD, Charged Device Model	1500	V

Table 8. Tape and Reel Information												
Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	60	16	22.4	1000

VM-702- F C E - K A A N - xxxMxxxxxx

Frequency in MHz

Product
XO

Package
5x7

Voltage Options
F: +2.25 t0 3.63 Vdc

Output
H: HCSL
C: LVPECL
D: LVDS

Temp Range
J: -20/70°C
E: -40/85°C

Other (Future Use)
N: Standard

Enable/Disable Pin
A: Pin 1

Enable/Disable Logic
A: Enable High

Stability
B: ±10ppm (excludes aging)
F: ±25ppm
K: ±50ppm

Note: not all combination of options are available.
Other specifications may be available upon request.

Example: VM-702-ECE-KAAN-156M250

For Additional Information, Please Contact

USA:
Vectron International
267 Lowell Road
Hudson, NH 03051
Tel: 1.888.328.7661
Fax: 1.888.329.8328

Europe:
Vectron International
Landstrasse, D-74924
Neckarbischofsheim, Germany
Tel: +49 (0) 3328.4784.17
Fax: +49 (0) 3328.4784.30

Asia:
VI Shanghai
1589 Century Avenue, the 19th Floor
Chamtime International Financial Center
Shanghai, China
Tel: 86.21.6081.2888
Fax: 86.21.6163.3598

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