

**CLOCK GENERATOR AND DRIVER FOR
8080A PROCESSORS**

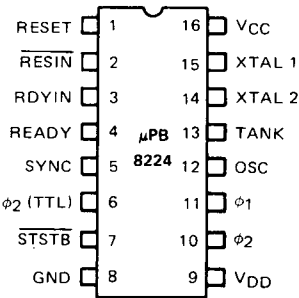
DESCRIPTION The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

- FEATURES**
- Crystal Controlled Clocks
 - Oscillator Output for External Timing
 - MOS Level Clocks for 8080A Processor
 - TTL Level Clock for DMA Activities
 - Power-up Reset for 8080A Processor
 - Ready Synchronization
 - Advanced Status Strobe
 - Reduces System Package Count
 - Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

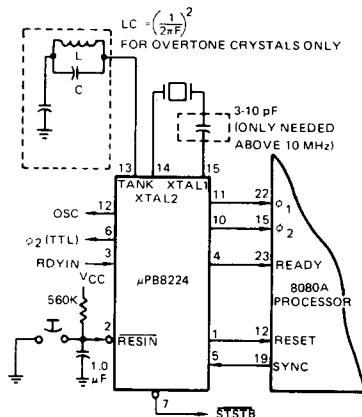
RESIN	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
STSTB	Status STB Output
φ1	} Processor Clocks
φ2	
XTAL 1	} Crystal Connections
XTAL 2	
TANK	Used With Overtone Crystal
OSC	Oscillator Output
φ2 (TTL)	φ2 CLK (TTL Level)
VCC	+5V
VDD	+12V
GND	0V

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2 , which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

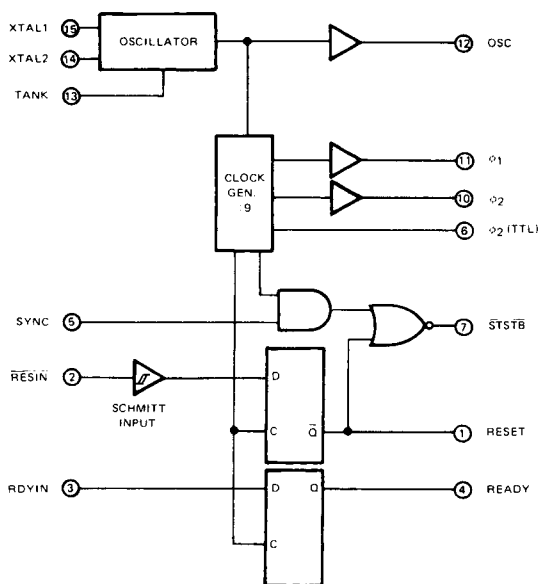
In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

The $\overline{STSTB}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{STSTB}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{RESIN}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages (TTL)	-0.5 to +7 Volts
All Output Voltages (MOS)	-0.5 to +13.5 Volts
All Input Voltages	-1.0 to +7 Volts
Supply Voltage V _{CC}	-0.5 to +7 Volts
Supply Voltage V _{DD}	-0.5 to +13.5 Volts
Output Currents	100 mA

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Current Loading	I _F			-0.25	mA	V _F = 0.45V
Input Leakage Current	I _R			10	μA	V _R = 5.25V
Input Forward Clamp Voltage	V _{CC}			-1.0	V	I _C = -5 mA
Input "Low" Voltage	V _{IL}			0.8	V	V _{CC} = 5.0V
Input "High" Voltage	V _{IH}	2.6			V	Reset Input
		2.0			V	All Other Inputs
RESIN Input Hysteresis	V _{IH} - V _{IL}	0.25			V	V _{CC} = 5.0V
Output "Low" Voltage	V _{OL}			0.45	V	φ ₁ , φ ₂ , Ready, Reset, STSTB
				0.45	V	I _{OL} = 2.5 mA
					V	All Other Inputs
					V	I _{OL} = 15 mA
Output "High" Voltage	V _{OH}	9.4			V	I _{OH} = -100 μA
φ ₁ , φ ₂		3.6			V	I _{OH} = -100 μA
READY, RESET		2.4			V	I _{OH} = -1 mA
All Other Outputs					V	I _{OH} = -1 mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I _{SC} ①	-10		-60	mA	V _O = 0V V _{CC} = 5.0V
Power Supply Current	I _{CC}			115	mA	
Power Supply Current	I _{DD}			12	mA	

Note: ① Caution, φ₁ and φ₂ output drivers do not have short circuit protection

T_a = 25°C; f = 1 MHz; V_{CC} = 5V; V_{DD} = 12V; V_{BIAS} = 2.5V

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C _{IN}			8	pF	

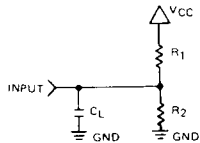
Note: ① This parameter is not 100% tested.

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

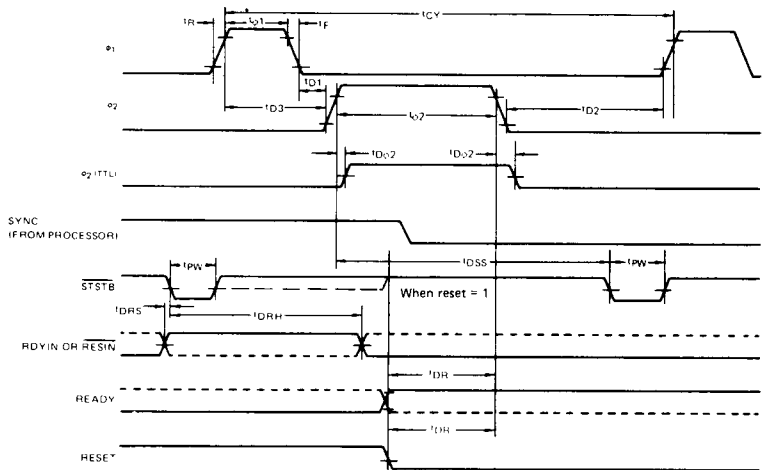
AC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS ①			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
φ ₁ Pulse Width	t _{φ1}	$\frac{2t_{CY}}{9}$ -20 ns			ns	C _L = 20 pF to 50 pF
φ ₂ Pulse Width	t _{φ2}	$\frac{5t_{CY}}{9}$ -35 ns				
φ ₁ to φ ₂ Delay	t _{D1}	0				
φ ₂ to φ ₁ Delay	t _{D2}	$\frac{2t_{CY}}{9}$ -14 ns				
φ ₁ to φ ₂ Delay	t _{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20 ns		
φ ₁ and φ ₂ Rise Time	t _R			20		
φ ₁ and φ ₂ Fall Time	t _F			20		
φ ₂ to φ ₂ (TTL) Delay	t _{Dφ2}	-5		+15	ns	φ ₂ TTL, C _L = 30 pF R ₁ = 300Ω R ₂ = 600Ω
φ ₂ to STSTB Delay	t _{DSS}	$\frac{6t_{CY}}{9}$ -30 ns		$\frac{6t_{CY}}{9}$	ns	STSTB, C _L = 15 pF R ₁ = 2K R ₂ = 4K
STSTB Pulse Width	t _{PW}	$\frac{t_{CY}}{9}$ -15 ns			ns	
RDYIN Setup Time to STSTB	t _{DRS}	50 ns - $\frac{4t_{CY}}{9}$				
RDYIN Hold Time After STSB	t _{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to φ ₂ Delay	t _{DR}	$\frac{4t_{CY}}{9}$ -25 ns			ns	Ready and Reset C _L = 10 pF R ₁ = 2K R ₂ = 4K
Crystal Frequency	f _{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f _{MAX}			27	MHz	

Note: (1) t_{CY} represents the processor clock period



TEST CIRCUIT



TIMING WAVEFORMS

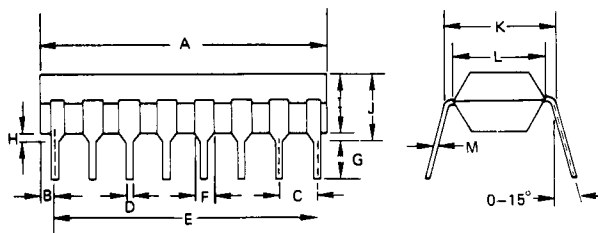
Voltage Measurement Points: φ₁, φ₂ Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

Note: ① With tank circuit use 3rd overtone mode.

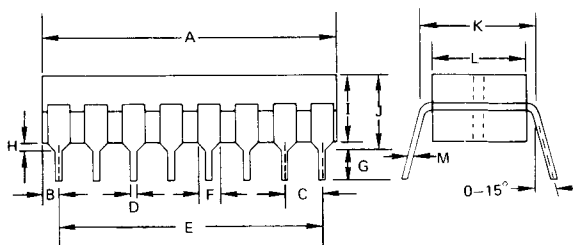
PACKAGE OUTLINE μPB8224C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	0.25 $\begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$	0.01

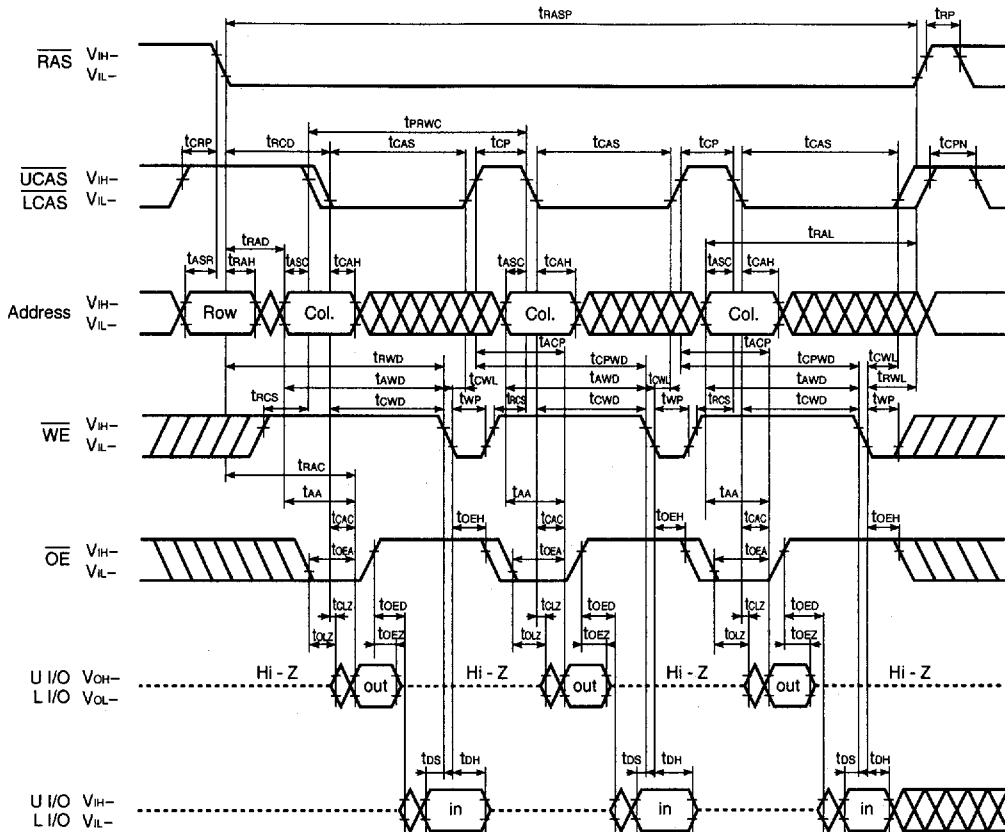
μPB8224D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.8	0.27
M	0.25 $\begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$	0.0098 $\begin{smallmatrix} +0.0039 \\ -0.0019 \end{smallmatrix}$

Fast Page Mode Read Modify Write Cycle

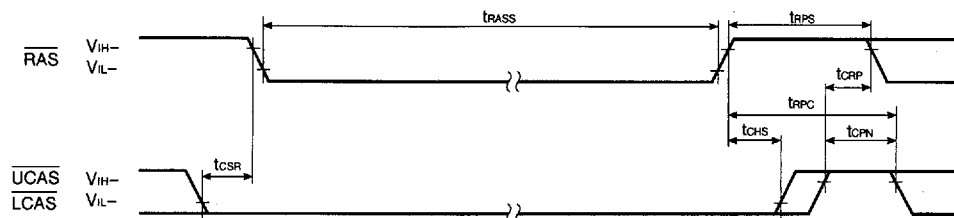


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

[illegible]

- 6427525 0091572 02T

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S18160: 1,024 times within a 16 ms interval

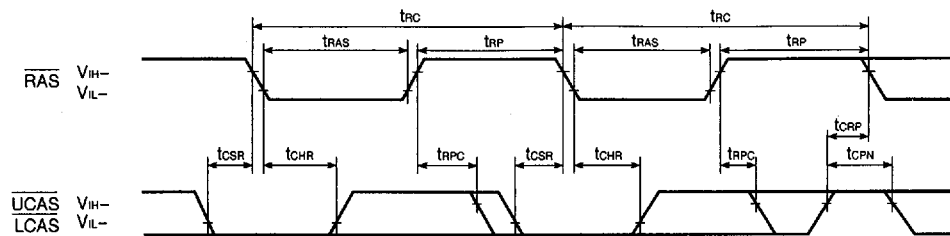
(3) If $t_{RASS} (MIN.)$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied. And refresh cycles as follows should be met.

μ PD42S18160: 1,024 times within a 128 ms interval

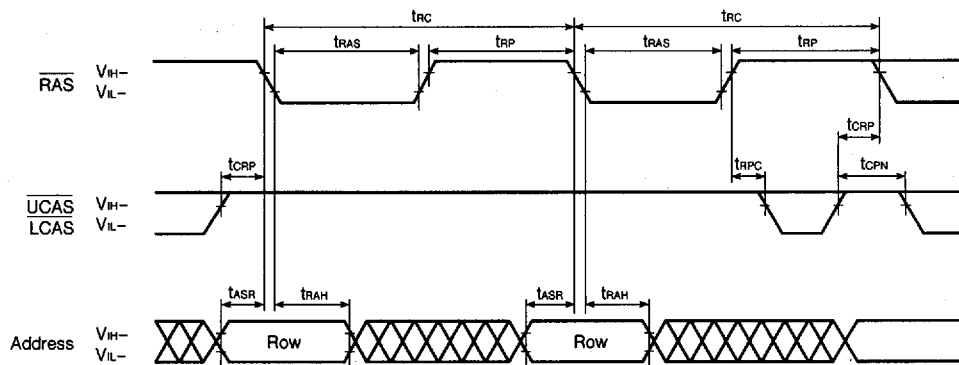
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle



Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)

