

IP4770/71/72CZ16

VGA/video interface with integrated buffers, ESD protection and integrated termination resistors

Rev. 01 — 25 October 2006

Product data sheet

1. General description

The IP4770CZ16, IP4771CZ16, IP4772CZ16 is connected between the VGA/DVI interface and the video graphics controller and includes level shifting for the DDC signals, buffering for the SYNC lines as well as high-level ESD protection diodes for the RGB signal lines.

The level shifting functions are required when the DDC controller operates at a lower supply voltage than the monitor. To use this level shifting function the gates of the two N-channel MOSFETs have to be connected to the supply rail of the DDC transceivers.

Buffering for the SYNC signals is provided by two non-inverting buffers, which accept TTL input levels and convert these to CMOS compliant output levels between pins $V_{CC(SYNC)}$ and GND.

The IP4770CZ16 and IP4771CZ16 contain the formerly external termination resistors, which are typically required for the HSYNC and VSYNC lines of the video interface:

- IP4770CZ16: $R_{sync} = 55 \Omega$
- IP4771CZ16: $R_{sync} = 65 \Omega$
- IP4772CZ16: $R_{sync} = 10 \Omega$ to allow termination of the SYNC lines

All RGB I/Os are protected by a special diode configuration offering a low line capacitance of 4 pF (maximum) only to provide protection to downstream components for ESD voltages as high as ± 8 kV contact discharge according to IEC 61000-4-2, level 4 standard.

2. Features

- Integrated high-level ESD protection, buffering, SYNC signal impedance matching and level shifting
- Terminal connections with integrated rail-to-rail clamping diodes with downstream ESD protection of ± 8 kV according to IEC 61000-4-2, level 4 standard
- Backflow protection on DDC lines
- Drivers for HSYNC and VSYNC lines
- Bidirectional level shifting N-channel FETs available for DDC clock and DDC data channels
- Integrated impedance matching resistors on SYNC lines
- Line capacitance < 4 pF per channel
- Lead-free package and RoHS compliant

3. Applications

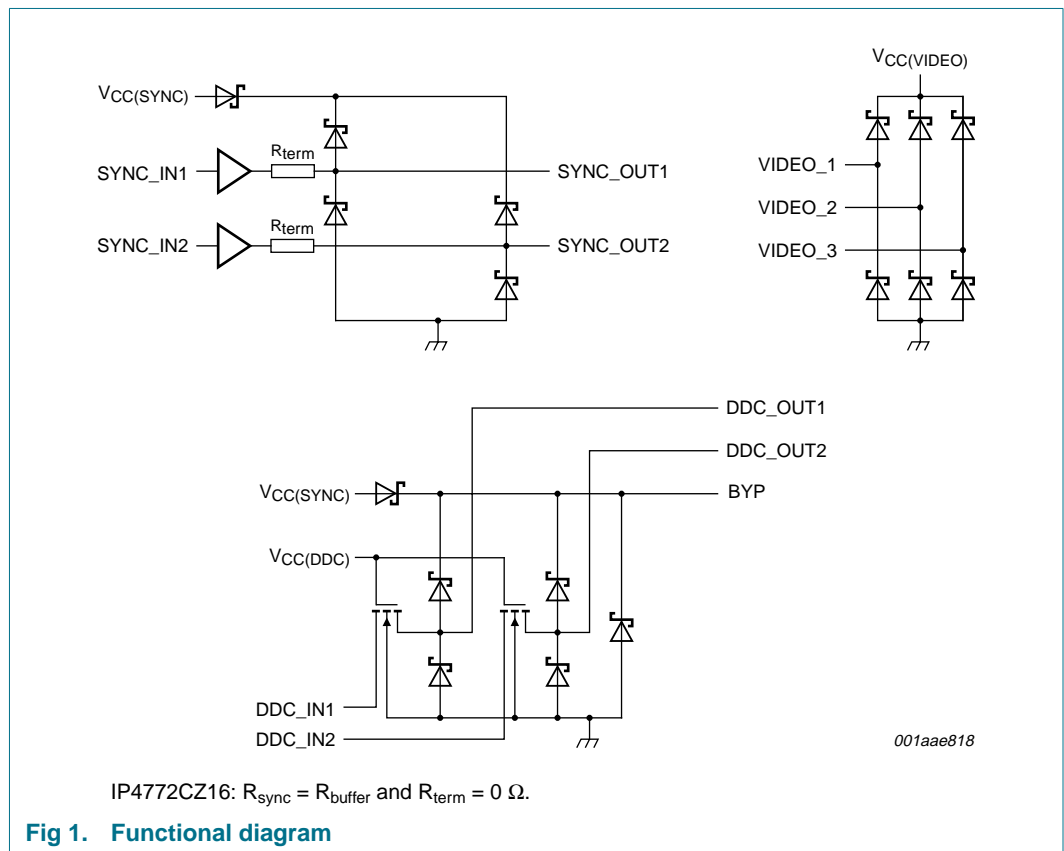
- To terminate and to buffer channels, to reduce EMI/RFI and to provide downstream ESD protection for:
 - ◆ VGA interfaces including DDC channels
 - ◆ Desktop and notebooks PCs
 - ◆ Graphics cards
 - ◆ Set top boxes

4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
IP4770CZ16	SSOP16	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
IP4771CZ16			
IP4772CZ16			

5. Functional diagram



6. Pinning information

6.1 Pinning

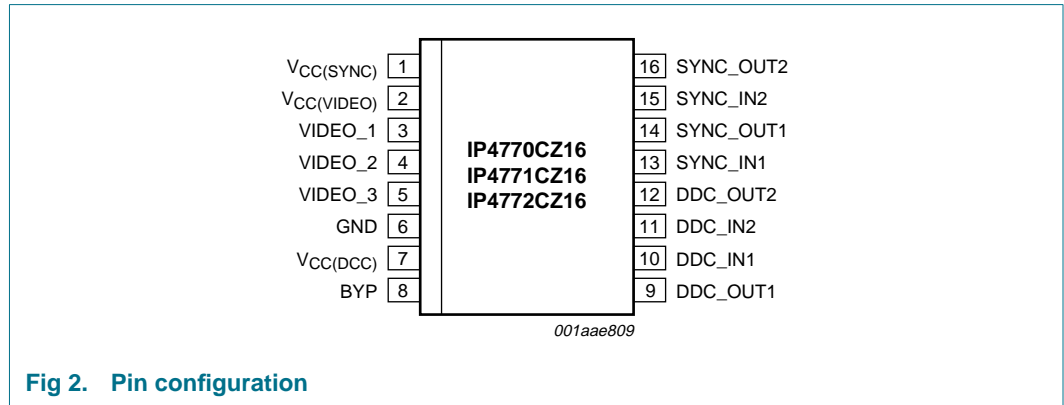


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{CC(SYNC)}	1	supply voltage for SYNC_1 and SYNC_2 level shifter and their connected ESD protections
V _{CC(VIDEO)}	2	supply voltage for VIDEO_1, VIDEO_2 and VIDEO_3 protection circuits
VIDEO_1	3	video signal ESD protection channel 1
VIDEO_2	4	video signal ESD protection channel 2
VIDEO_3	5	video signal ESD protection channel 3
GND	6	ground
V _{CC(DCC)}	7	supply voltage for DDC_1 and DDC_2 level shifter N-FET gates
BYP	8	this input is used to connect an external 0.2 μF bypass capacitor to increase ESD withstand voltage rating for the DDC outputs (±8 kV with capacitor or ±4 kV without capacitor)
DDC_OUT1	9	DDC signal output 1; connected to the video connector side of one of the SYNC lines
DDC_IN1	10	DDC signal input 1; connected to the VGA controller side of one of the SYNC lines
DDC_IN2	11	DDC signal input 2; connected to the VGA controller side of one of the SYNC lines
DDC_OUT2	12	DDC signal output 2; connected to the video connector side of one of the SYNC lines
SYNC_IN1	13	SYNC signal input 1; connected to the VGA controller side of one of the SYNC lines
SYNC_OUT1	14	SYNC signal output 1; connected to the video connector side of one of the SYNC lines
SYNC_IN2	15	SYNC signal input 2; connected to the VGA controller side of one of the SYNC lines
SYNC_OUT2	16	SYNC signal output 2; connected to the video connector side of one of the SYNC lines

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground (GND).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2; pins VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2, DDC_OUT1, DDC_OUT2	[1]		
		level 4; contact	-8	+8	kV
		level 4; air discharge	-15	+15	kV
		IEC 61000-4-2; all other pins			
		level 1; contact	-2	+2	kV
		level 1; air discharge	-2	+2	kV
V _{CC(VIDEO)}	video supply voltage		-0.5	5.5	V
V _{CC(DDC)}	data display channel supply voltage		-0.5	5.5	V
V _{CC(SYNC)}	synchronization supply voltage		-0.5	5.5	V
V _{I(VIDEO_1)}	input voltage on pin VIDEO_1		-0.5	V _{CC(VIDEO)}	V
V _{I(VIDEO_2)}	input voltage on pin VIDEO_2		-0.5	V _{CC(VIDEO)}	V
V _{I(VIDEO_3)}	input voltage on pin VIDEO_3		-0.5	V _{CC(VIDEO)}	V
V _{I(DDC_IN1)}	input voltage on pin DDC_IN1		-0.5	V _{CC(DDC)}	V
V _{I(DDC_IN2)}	input voltage on pin DDC_IN2		-0.5	V _{CC(DDC)}	V
V _{I(SYNC_IN1)}	input voltage on pin SYNC_IN1		-0.5	V _{CC(SYNC)}	V
V _{I(SYNC_IN2)}	input voltage on pin SYNC_IN2		-0.5	V _{CC(SYNC)}	V
V _{O(DDC_OUT1)}	output voltage on pin DDC_OUT1		-0.5	V _{CC(DDC)}	V
V _{O(DDC_OUT2)}	output voltage on pin DDC_OUT2		-0.5	V _{CC(DDC)}	V
P _{tot}	total power dissipation	T _{amb} = 25 °C	-	500	mW
T _{stg}	storage temperature		-55	+125	°C

[1] Pins BYP, V_{CC(VIDEO)} and V_{CC(SYNC)} must be bypassed to ground (pin GND) via a low-impedance ground plane with 0.22 µF, low inductance, chip ceramic capacitor at each supply pin.

ESD pulse is applied between the pins VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2, DDC_OUT1, DDC_OUT2 and GND.

The bypass capacitor at pin BYP can be omitted. In this case the maximum ESD level for DDC_OUT1 and DDC_OUT2 pins is reduced to ±4 kV.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{oper}	operating temperature		-40	-	+85	°C

9. Characteristics

Table 5. Sync circuit characteristics

$V_{CC(SYNC)} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply: pin $V_{CC(SYNC)}$						
$I_{CC(SYNC)}$	supply current on pin $V_{CC(SYNC)}$		[1]	-	50	μA
		SYNC input at 3 V	[1]	-	2	mA
Input: pins SYNC_IN1 and SYNC_IN2						
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.6	V
Output: pins SYNC_OUT1 and SYNC_OUT2						
V_{OH}	HIGH-level output voltage	$I_{OH} = 1\text{ mA}$	4.85	-	-	V
		IP4772CZ16; $I_{OH} = 24\text{ mA}$	2.0	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 1\text{ mA}$	-	-	0.15	V
		IP4772CZ16; $I_{OL} = 24\text{ mA}$	-	-	0.8	V
R_{sync}	synchronization resistance	IP4770CZ16	[2]	-	55	Ω
		IP4771CZ16	[2]	-	65	Ω
		IP4772CZ16	[3]	-	10	Ω
Sync channel						
t_{PLH}	LOW-to-HIGH propagation delay	$C_L = 50\text{ pF}$; t_r and $t_f \leq 5\text{ ns}$	[4]	-	12	ns
t_{PHL}	HIGH-to-LOW propagation delay	$C_L = 50\text{ pF}$; t_r and $t_f \leq 5\text{ ns}$	[4]	-	12	ns
$t_{r(o)}$	output rise time	$C_L = 50\text{ pF}$; t_r and $t_f \leq 5\text{ ns}$	-	4	-	ns
		$C_L = 7\text{ pF}$; t_r and $t_f \leq 5\text{ ns}$	-	1.5	-	ns
$t_{f(o)}$	output fall time	$C_L = 50\text{ pF}$; t_r and $t_f \leq 5\text{ ns}$	-	4	-	ns
		$C_L = 7\text{ pF}$; t_r and $t_f \leq 5\text{ ns}$	-	1.5	-	ns
Protection diode						
$I_{L(r)}$	reverse leakage current	per channel; $V = 3.0\text{ V}$	-	-	1	μA
V_{BRzd}	Zener diode breakdown voltage	$I = 1\text{ mA}$	6	-	9	V
V_{Fd}	diode forward voltage	$I_F = 1\text{ mA}$	-	0.7	-	V

[1] SYNC outputs unloaded.

[2] $R_{sync} = R_{term} + R_{buffer}$.

[3] $R_{sync} = R_{buffer}$ because $R_{term} = 0\text{ Ω}$.

[4] This parameter is guaranteed by design and characterization.

Table 6. Video circuit characteristics $V_{CC(VIDEO)} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply: pin $V_{CC(VIDEO)}$						
$I_{CC(VIDEO)}$	supply current on pin $V_{CC(VIDEO)}$	static input signals	-	-	10	μA
Video channel: pins VIDEO_1, VIDEO_2 and VIDEO_3						
$C_{ch(video)}$	video channel capacitance	$f_i = 1\text{ MHz}$; $V_I = 2.5\text{ V}$	[1]	-	4	pF
$I_{i(video)}$	video input current	$V_I = V_{CC(VIDEO)}$ or GND	-1	-	+1	μA
Protection diode						
V_{Fd}	diode forward voltage	$I_F = 1\text{ mA}$	-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

Table 7. Level circuit characteristics $V_{CC(DDC)} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply: pin $V_{CC(DDC)}$						
$I_{CC(DDC)}$	supply current on pin $V_{CC(DDC)}$		-	-	10	μA
N-MOSFET						
$I_{L(off)}$	off-state leakage current		[1]	-	10	μA
ΔV_{on}	on-state voltage drop	$V_{CC(DDC)} = 2.5\text{ V}$; $V_S = \text{GND}$; $I_{DS} = 3\text{ mA}$	-	-	0.18	V
Protection diode						
$I_{L(r)}$	reverse leakage current	per channel; $V = 3.0\text{ V}$	-	-	1	μA
V_{BRzd}	Zener diode breakdown voltage	$I = 1\text{ mA}$	6	-	9	V
V_{Fd}	diode forward voltage	$I_F = 1\text{ mA}$	-	0.7	-	V

[1] Input $V_{I(DDC_INx)} \leq V_{CC(DDC)} - 0.4\text{ V}$ and output $V_{O(DDC_OUTx)} = V_{CC(DDC)}$ or
input $V_{I(DDC_INx)} = V_{CC(DDC)}$ and output $V_{O(DDC_OUTx)} \leq V_{CC(DDC)} - 0.4\text{ V}$.

10. Application information

The IP4770CZ16, IP4771CZ16, IP4772CZ16 should be placed as close as possible to the VGA/DVI interface connector.

The ESD protection channels VIDEO_1, VIDEO_2 and VIDEO_3 can be connected in any order with RGB signals.

The 100 kΩ resistors between the DDC_OUTx channels and VCC_5V are optional. They may be used, if required, to pull-up the DDC_OUTx lines to VCC_5V when no monitor is connected to the VGA connector. Backflow current can flow between pins DDC_OUTx and VCC_5V via these resistors when VCC_5V is powered down.

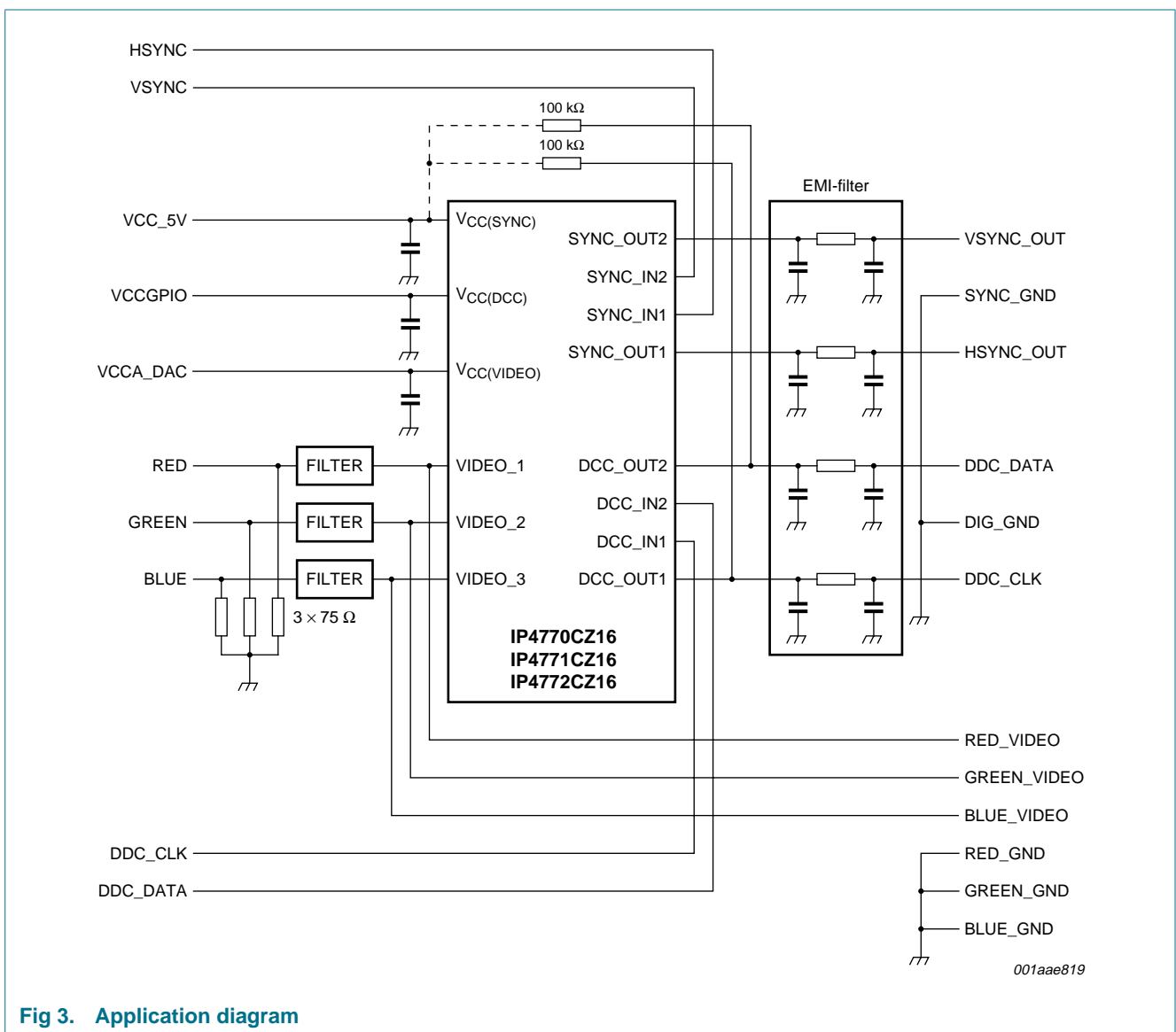


Fig 3. Application diagram

11. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

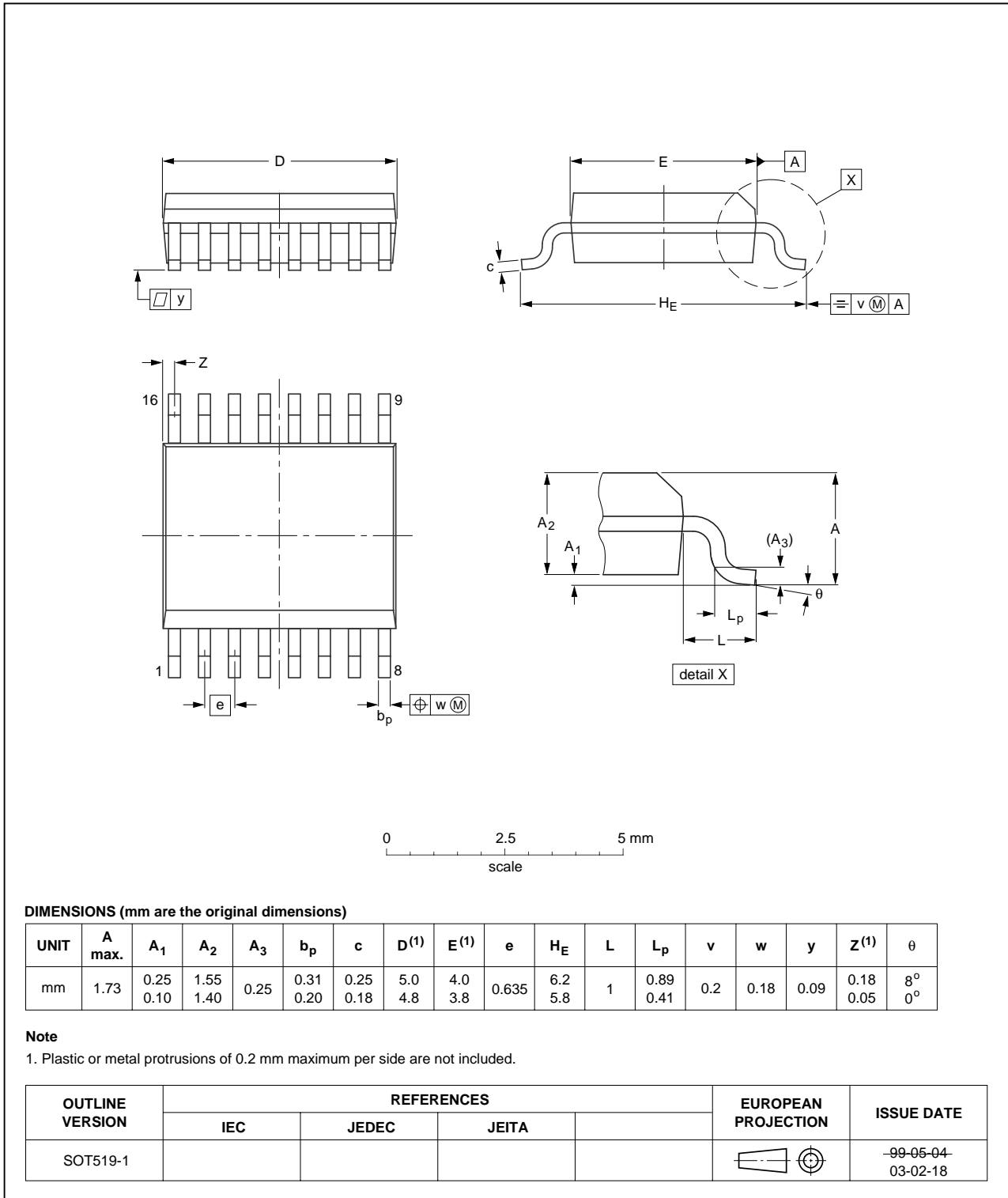


Fig 4. Package outline SOT519-1 (SSOP16)

12. Abbreviations

Table 8. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DDC	Data Display Channel
DVI	Digital Video Interface
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HSYNC	Horizontal SYNChronization
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PC	Personal Computer
RFI	Radio Frequency Interference
RGB	Red Green Blue
SYNC	SYNChronization
TTL	Transistor-Transistor Logic
VGA	Video Graphics Adapter
VSYNC	Vertical SYNChronization

13. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4770CZ16_4771_4772_1	20061025	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

14.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

16. Contents

1 **General description** 1

2 **Features** 1

3 **Applications** 2

4 **Ordering information** 2

5 **Functional diagram** 2

6 **Pinning information** 3

6.1 Pinning 3

6.2 Pin description 3

7 **Limiting values** 4

8 **Recommended operating conditions** 5

9 **Characteristics** 5

10 **Application information** 7

11 **Package outline** 8

12 **Abbreviations** 9

13 **Revision history** 9

14 **Legal information** 10

14.1 Data sheet status 10

14.2 Definitions 10

14.3 Disclaimers 10

14.4 Trademarks 10

15 **Contact information** 10

16 **Contents** 11

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

