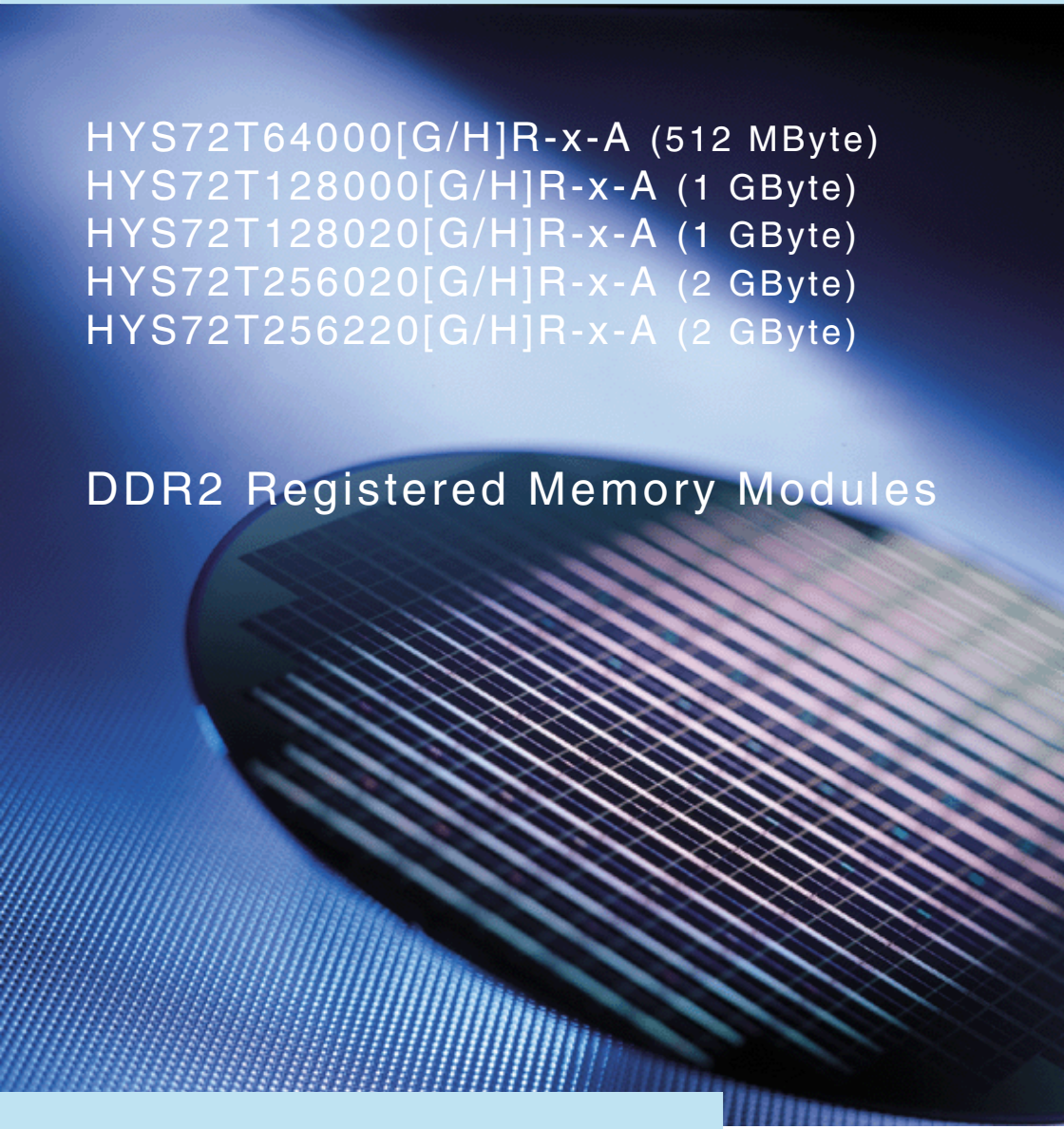
Data Sheet, Rev. 0.85, Apr. 2004

HYS72T64000[G/H]R-x-A (512 MByte)
HYS72T128000[G/H]R-x-A (1 GByte)
HYS72T128020[G/H]R-x-A (1 GByte)
HYS72T256020[G/H]R-x-A (2 GByte)
HYS72T256220[G/H]R-x-A (2 GByte)

DDR2 Registered Memory Modules



Memory Products

Never stop thinking.

Low Profile 240-pin Registered DDR2 SDRAM Modules Datasheet

512 MByte, 1 GByte & 2 GByte Modules
PC2-3200R, PC2-4300R

- 240-pin Registered 8-Byte ECC Dual-In-Line DDR2 SDRAM Module for PC, Workstation and Server main memory applications
- One rank 64Mb x 72, 128Mb x 72 and two ranks 128Mb × 72 and 256Mb x 72 organizations
- JEDEC standard Double Data Rate 2 Synchronous DRAMs (DDR2 SDRAMs) with + 1.8 V (± 0.1 V) power supply
- 512MB and 1 GB modulesModules built with 512Mb DDR2 SDRAMs in 60-ball FBGA chipsize packages
- Two versions of 2 GB modules
  built with 63-ball FBGA dual die chipsize packages (2 x 512Mb components) or 60-ball FBGA packages
- Programmable $\overline{\text{CAS}}$ Latencies (3, 4 & 5), Burst Length (4 & 8) and Burst Type.
- Auto Refresh and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- Re-drive for all input signals using register and PLL devices.
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 133.35 mm x 30,00 mm (MO-237)
- Based on JEDEC standard reference card designs

Performance:

Speed Grade Indicator	–5	–3.7	Unit
Component Speed Grade on Module	DDR2–400	DDR2–533	
Module Speed Grade	PC2–3200R	PC2–4300R	
Max. Clock Frequency @ CL = 3	200	200	MHz
Max. Clock Frequency@ CL = 4 & 5	200	266	MHz

1.0 Description

The INFINEON HYS72Taaabcd[G/H]R module family are low profile Registered DIMM modules with 30,00 mm height based on DDR2 technology. DIMMs are available in 64M x 72 (512MByte), 128M x 72 (1GByte) and 256M x 72 (2GByte) organisation and density, intended for mounting into 240 pin connector sockets.

The memory array is designed with 512Mb Double Data Rate (DDR2) Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board, which provide a proper voltage supply impedance over the whole frequency range of operations as number and values are accordant to the JEDEC specification. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

1.1 Ordering Information

Product Type	Compliance Code	Description	SDRAM Technology
PC2-3200 (DDR2-400)			
HYS72T64000GR-5-A	PC2-3200R-333-11-A	one rank 512 MB Reg. DIMM	512 Mbit (x8)
HYS72T128020GR-5-A	PC2-3200R-333-11-B	two ranks 1024 MB Reg.DIMM	512 Mbit (x8)
HYS72T128000GR-5-A	PC2-3200R-333-11-C	one rank 1024 MB Reg. DIMM	512 Mbit (x4)
HYS72T256220GR-5-A	PC2-3200R-333-11	two ranks 2048 MB Reg. DIMM	512 Mbit (x4)
HYS72T256020GR-5-A	PC2-3200R-333-11	two ranks 2048 MB Reg. DIMM	512 Mbit (x4)
PC2-4300 (DDR2-533)			
HYS72T64000GR-3.7-A	PC2-4300R-444-11-A	one rank 512 MB Reg. DIMM	512 Mbit (x8)
HYS72T128020GR-3.7-A	PC2-4300R-444-11-B	two ranks 1024 MB Reg.DIMM	512 Mbit (x8)
HYS72T128000GR-3.7-A	PC2-4300R-444-11-C	one rank 1024 MB Reg. DIMM	512 Mbit (x4)
HYS72T256020GR-3.7-A	PC2-4300R-444-11	two ranks 2048 MB Reg. DIMM	512 Mbit (x4)
PC2-3200 (DDR2-400)			
HYS72T64000HR-5-A	PC2-3200R-333-11-A	one rank 512 MB Reg. DIMM	512 Mbit (x8)
HYS72T128020HR-5-A	PC2-3200R-333-11-B	two ranks 1024 MB Reg.DIMM	512 Mbit (x8)
HYS72T128000HR-5-A	PC2-3200R-333-11-C	one rank 1024 MB Reg. DIMM	512 Mbit (x4)
HYS72T256220HR-5-A	PC2-3200R-333-11	two ranks 2048 MB Reg. DIMM	512 Mbit (x4)
HYS72T256020HR-5-A	PC2-3200R-333-11	two ranks 2048 MB Reg. DIMM	512 Mbit (x4)
PC2-4300 (DDR2-533)			
HYS72T64000HR-3.7-A	PC2-4300R-444-11-A	one rank 512 MB Reg. DIMM	512 Mbit (x8)
HYS72T128020HR-3.7-A	PC2-4300R-444-11-B	two ranks 1024 MB Reg.DIMM	512 Mbit (x8)
HYS72T128000HR-3.7-A	PC2-4300R-444-11-C	one rank 1024 MB Reg. DIMM	512 Mbit (x4)
HYS72T256020HR-3.7-A	PC2-4300R-444-11	two ranks 2048 MB Reg. DIMM	512 Mbit (x4)

Notes:

1. For all INFINEON DDR2 module and component nomenclature see section 8 of this data sheet.
2. The Compliance Code is printed on the module label and describes the speed grade, e. g. “PC2-4300R-444-11-C”, where 4300R means Registered modules with 4.26 GB/sec Module Bandwidth and “444-11” means $\overline{\text{CAS}}$ latency = 4, trcd latency = 4 and trp latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card “C”.

1.2 Address Format

Product Type	DIMM Density	Organization	DIMM Ranks	SDRAMs	# of SDRAMs	# of row/bank/ column bits
HYS72T64000GR HYS72T64000HR	512 MB	64Mb × 72	1	(512Mb) 64Mb × 8	9	14/2/10
HYS72T128020GR HYS72T128020HR	1024 MB	2 x 64Mb × 72	2	(512Mb) 64Mb × 8	18	14/2/10
HYS72T128000GR HYS72T128000HR	1024 MB	128Mb x 72	1	(512Mb) 128Mb × 4	18	14/2/11
HYS72T256220GR HYS72T256220HR	2048 MB	2 x 128Mb × 72	2	(512Mb) 128Mb × 4	36	14/2/11
HYS72T256020GR HYS72T256020HR	2048 MB	2 x 128Mb × 72	2	(512Mb) 128Mb × 4	36	14/2/11

1.3 Components on Modules and RawCard

DIMM Density	DRAM components reference datasheet	PLL	Register	Raw Card
512 MB	HYB18T512800AC HYB18T512800AF	1:10, 1.8V, CU877	1:1 25-bit 1.8V SSTU32864	A
1024 MB	HYB18T512800AC HYB18T512800AF	1:10, 1.8V, CU877	1:2 14-bit 1.8V SSTU32864	B
1024 MB	HYB18T512400AC HYB18T512400AF	1:10, 1.8V, CU877	1:2 14-bit 1.8V SSTU32864	C
2048 MB	HYB18T512400AC HYB18T512400AF	tbd.	tbd.	tbd.
2048 MB	HYB18T512400AC HYB18T512400AF	tbd.	tbd.	tbd.

For a detailed description of all functionalities of the DRAM components on these modules see the referenced component data sheet

1.4 Pin Definition and Function

Pin Name	Description	Pin Name	Description
A[13:0]	Row Address Inputs	CB[7:0]	DIMM ECC Check Bits
A11, A[9:0]	Column Address Inputs [4]	DQS[8:0]	SDRAM low data strobes
A10/AP	Column Address Input for Auto-Precharge	DM[8:0] / DQS[17:9]	SDRAM low data mask/ high data strobes
BA[1:0]	SDRAM Bank Selects	$\overline{\text{DQS}}$[17:0]	SDRAM differential data strobes
CK0	Clock input (positive line of differential pair)	SCL	Serial bus clock
$\overline{\text{CK0}}$	Clock input (negative line of differential pair)	SDA	Serial bus data line
$\overline{\text{RAS}}$	Row Address Strobe	SA[2:0]	slave address select
$\overline{\text{CAS}}$	Column Address Strobe	V_{DD}	Power (+ 1.8 V)
$\overline{\text{WE}}$	Read/Write Input	V_{REF}	I/O reference supply
$\overline{\text{CS}}$[1:0]	Chip Selects [3]	V_{SS}	Ground
CKE[1:0]	Clock Enable [3]	V_{DDSPD}	EEPROM power supply
ODT[1:0]	Active termination control lines [1] [3]	$\overline{\text{RESET}}$	Register and PLL control pin [2]
DQ[63:0]	Data Input/Output	NC	No connection

1) Active termination only applies to DQ, DQS, $\overline{\text{DQS}}$ and DM signals
2) When low, all register outputs will be driven low and the PLL clocks to the DRAM and registers will be set to low levels (the PLL will remain synchronized with the input clock
3) $\overline{\text{CS1}}$, ODT1 and CKE1 are used on dual rank modules only
4) Column address A11 is used on modules based on x4 organised 512Mb DDR2 components only.

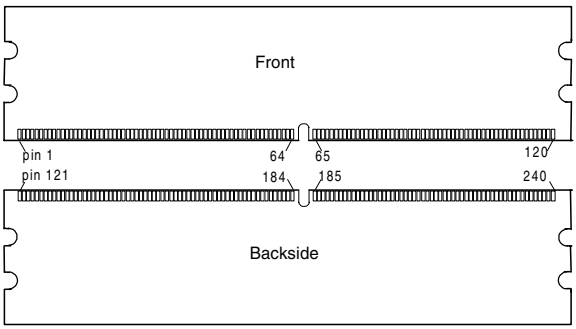
1.5 Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	VREF	121	VSS	61	A4	181	VDDQ
2	VSS	122	DQ4	62	VDDQ	182	A3
3	DQ0	123	DQ5	63	A2	183	A1
4	DQ1	124	VSS	64	VDD	184	VDD
5	VSS	125	DM0, DQS9	KEY		KEY	
6	$\overline{\text{DQS0}}$	126	$\overline{\text{DQS9}}$	65	VSS	185	$\overline{\text{CK0}}$
7	DQS0	127	VSS	66	VSS	186	CK0
8	VSS	128	DQ6	67	VDD	187	VDD
9	DQ2	129	DQ7	68	NC	188	A0
10	DQ3	130	VSS	69	VDD	189	VDD
11	VSS	131	DQ12	70	A10/AP	190	BA1
12	DQ8	132	DQ13	71	BA0	191	VDDQ
13	DQ9	133	VSS	72	VDDQ	192	$\overline{\text{RAS}}$
14	VSS	134	DM1, DQS10	73	$\overline{\text{WE}}$	193	$\overline{\text{CS0}}$
15	$\overline{\text{DQS1}}$	135	$\overline{\text{DQS10}}$	74	$\overline{\text{CAS}}$	194	VDDQ
16	DQS1	136	VSS	75	VDDQ	195	ODT0
17	VSS	137	NC	76	$\overline{\text{CS1}}$	196	A13
18	$\overline{\text{RESET}}$	138	NC	77	ODT1	197	VDD
19	NC	139	$\overline{\text{VSS}}$	78	VDDQ	198	VSS
20	VSS	140	DQ14	79	VSS	199	DQ36
21	DQ10	141	DQ15	80	DQ32	200	DQ37
22	DQ11	142	VSS	81	DQ33	201	VSS
23	VSS	143	DQ20	82	VSS	202	DM4, DQS13
24	DQ16	144	DQ21	83	$\overline{\text{DQS4}}$	203	$\overline{\text{DQS13}}$
25	DQ17	145	VSS	84	DQS4	204	VSS
26	VSS	146	DM2, DQS11	85	VSS	205	DQ38
27	$\overline{\text{DQS2}}$	147	$\overline{\text{DQS11}}$	86	DQ34	206	DQ39
28	DQS2	148	VSS	87	DQ35	207	VSS
29	VSS	149	DQ22	88	VSS	208	DQ44
30	DQ18	150	DQ23	89	DQ40	209	DQ45
31	DQ19	151	VSS	90	DQ41	210	VSS
32	VSS	152	DQ28	91	VSS	211	DM5, DQS14
33	DQ24	153	DQ29	92	$\overline{\text{DQS5}}$	212	$\overline{\text{DQS14}}$
34	DQ25	154	VSS	93	DQS5	213	VSS
35	VSS	155	DM3, DQS12	94	VSS	214	DQ46
36	$\overline{\text{DQS3}}$	156	$\overline{\text{DQS12}}$	95	DQ42	215	DQ47
37	DQS3	157	VSS	96	DQ43	216	VSS
38	VSS	158	DQ30	97	VSS	217	DQ52
39	DQ26	159	DQ31	98	DQ48	218	DQ53
40	DQ27	160	VSS	99	DQ49	219	VSS

Pin Configuration (cont'd)

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
41	VSS	161	CB4	100	VSS	220	NC
42	CB0	162	CB5	101	SA2	221	NC
43	CB1	163	VSS	102	NC	222	VSS
44	VSS	164	DM8, DQS17	103	VSS	223	DM6, DQS15
45	$\overline{\text{DQS8}}$	165	$\overline{\text{DQS17}}$	104	$\overline{\text{DQS6}}$	224	$\overline{\text{DQS15}}$
46	DQS8	166	VSS	105	DQS6	225	VSS
47	VSS	167	CB6	106	VSS	226	DQ54
48	CB2	168	CB7	107	DQ50	227	DQ55
49	CB3	169	VSS	108	DQ51	228	VSS
50	VSS	170	VDDQ	109	VSS	229	DQ60
51	VDDQ	171	NC, CKE1	110	DQ56	230	DQ61
52	CKE0	172	VDD	111	DQ57	231	VSS
53	VDD	173	NC	112	VSS	232	DM7, DQS16
54	NC	174	NC	113	$\overline{\text{DQS7}}$	233	$\overline{\text{DQS16}}$
55	NC	175	VDDQ	114	DQS7	234	VSS
56	VDDQ	176	A12	115	VSS	235	DQ62
57	A11	177	A9	116	DQ58	236	DQ63
58	A7	178	VDD	117	DQ59	237	VSS
59	VDD	179	A8	118	VSS	238	VDDSPD
60	A5	180	A6	119	SDA	239	SA0
				120	SCL	240	SA1

1.6 Pin Locations



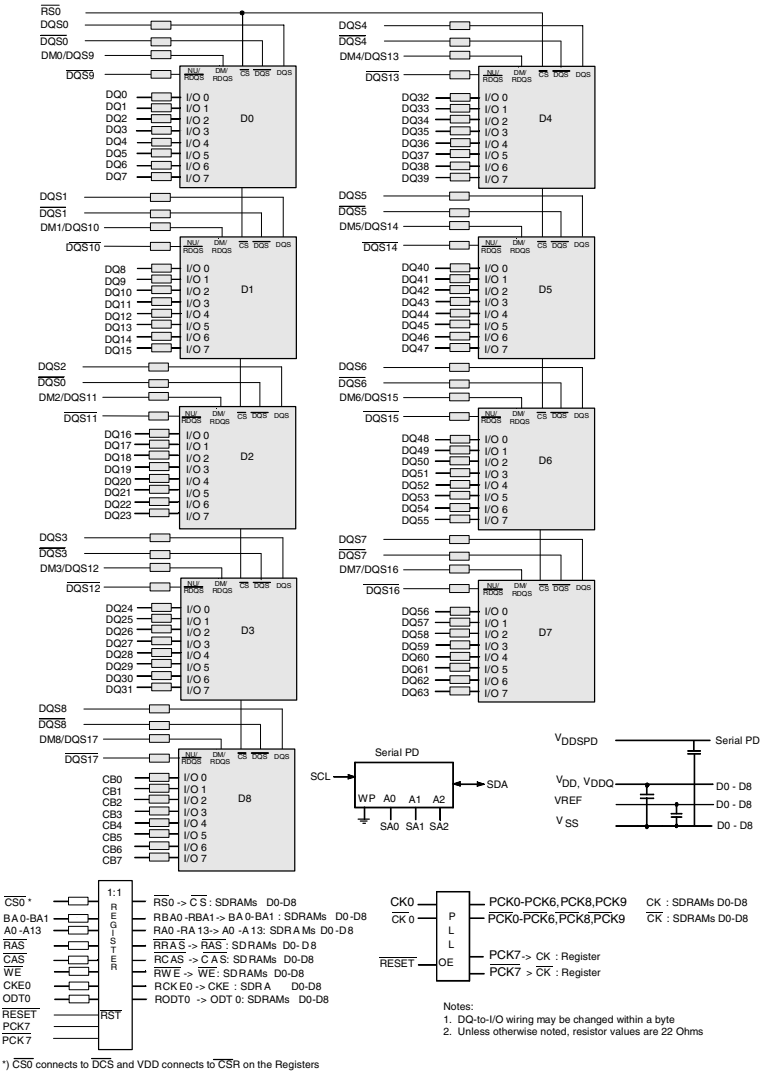
240 pin Modules (MO-237)

1.7 Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, $\overline{CK0}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. An on-board DLL circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers of the SDRAMs. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank).
$\overline{CS}$[1:0]	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both $\overline{CS}$[1:0] are high, all register outputs (except CK, ODT and Chip select) remain in the previous state.
ODT[1:0]	Input	Active High	On-Die Termination control signals
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive edge of the clock, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
DM[8:0]	Input	Active High	Masks write data when high, issued concurrently with input data.
BA[1:0]	Input	-	Selects which internal SDRAM memory bank is activated
A[13:0]	Input	-	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10(=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ[63:0], CB[7:0]	I/O	-	Data and Check Bit Input /Output pins.
DQS[17:0], $\overline{DQS}$[17:0]	I/O	Cross point	The data strobes, associated with one data byte, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sources by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA[2:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
$\overline{RESET}$	Input	-	The $\overline{RESET}$ pin is connected to the $\overline{RST}$ pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and the register(s) will be set to low level. The PLL will remain synchronized with the input clock.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V_{REF}	Supply	-	Reference voltage for the SSTL-18 inputs.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.
Note: $\overline{CS1}$, ODT1 and CKE1 are used on dual rank modules only.			

2.0 Block Diagrams

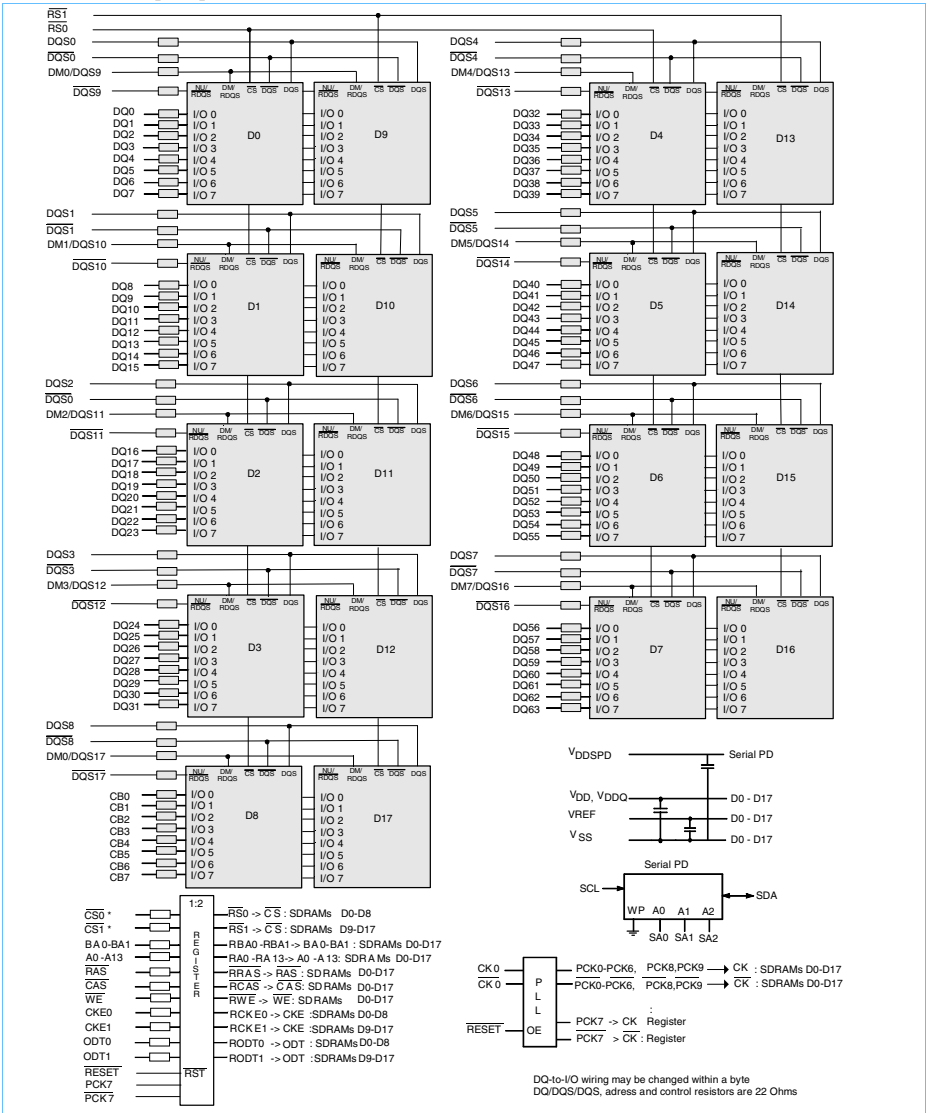
2.1 One Rank 64M x 72 (512 MByte) DDR2 SDRAM DIMM Module (x8 components) HYS72T64000[G/H] on Raw Card A



Block Diagrams (cont'd)

2.2 128M x 72 (1GByte) two rank DDR2 SDRAM DIMM Modules (x8 components)

HYS72T128020[G/H] on Raw Card B

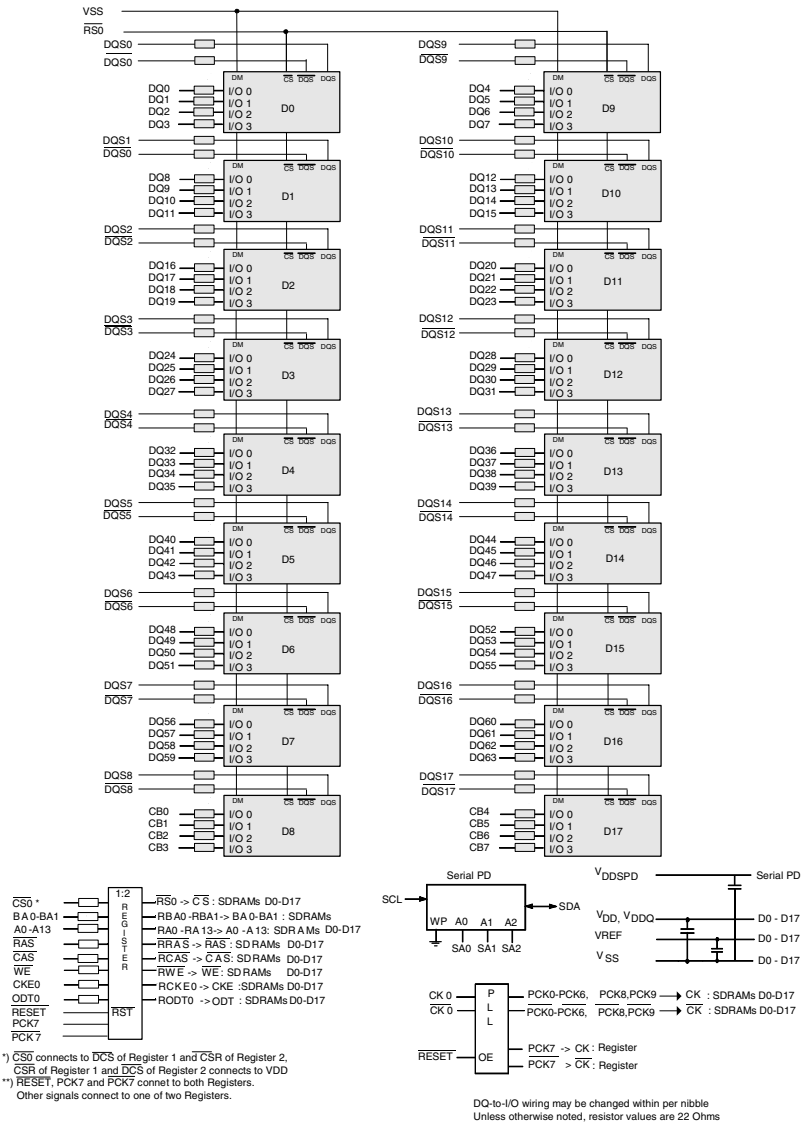


*) CS0 connects to CRS, CS1 connects to CSR on a Register. CS1 connects to DCS and CS0 connects to CSR on another Register.
RESET, PCK7 and PCK7 connect to bother Registers. Other signals connect to one of two Registers.

Block Diagrams (cont'd)

2.3 One Rank 128M x 72 (1 GByte) DDR2 SDRAM DIMM Modules (x4 components)

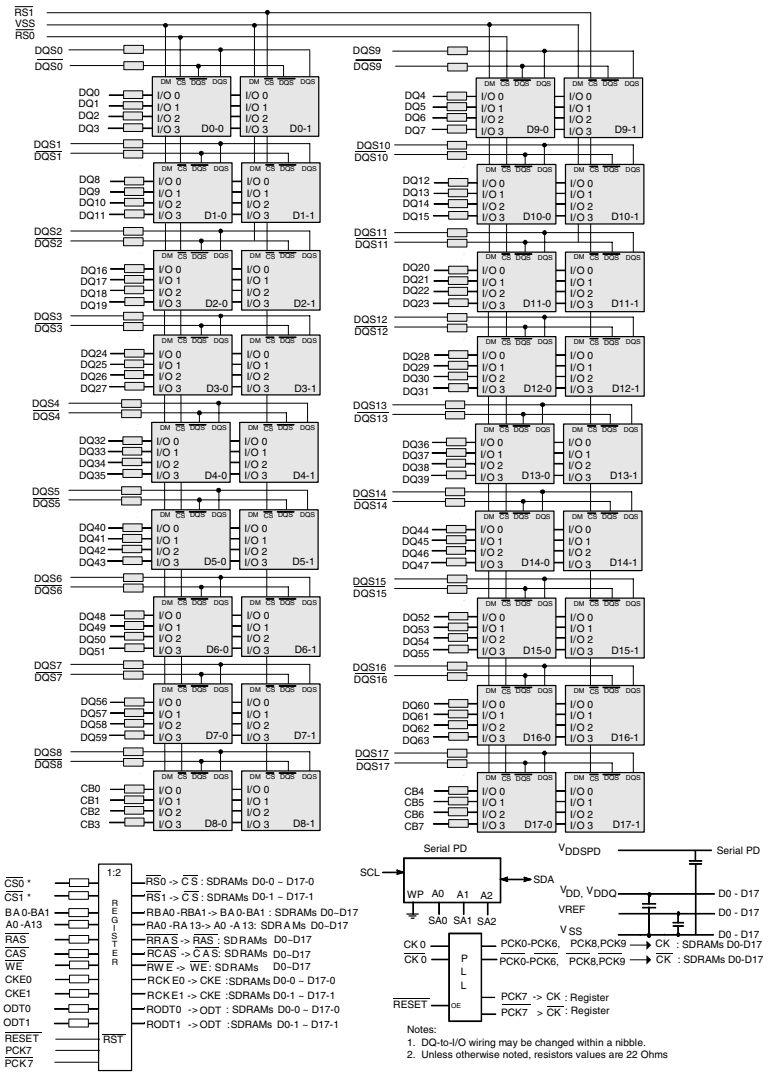
HYS72T128000[G/H] on Raw Card C



Block Diagrams (cont'd)

2.4 256M x 72 (2 GByte) two rank DDR2 SDRAM DIMM Modules (x4 components)

HYS72T256020[G/H] / HYS72T256220[G/H]



*) $\overline{CS0}$ connects to $\overline{CRS}$, $\overline{CS1}$ connects to $\overline{CSR}$ on a Register. $\overline{CS1}$ connects to $\overline{DCS}$ and $\overline{CS0}$ connects to $\overline{CSR}$ on another Register. RESET, PCK7 and $\overline{PCK7}$ connect to bother Registers. Other signals connect to one of two Registers.

3.0 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V
Voltage on $V_{DD\,Q}$ relative to V_{SS}	V_{DDQ}	– 0.5	2.3	
Storage temperature range	T_{STG}	-55	+100	°C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.1 Operating Temperature Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DIMM Module Operating Temperature Range (ambient)	TOPR	0	+55	°C	
DRAM Component Case Temperature Range	TCASE	0	+95	°C	1 - 4

1. DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85°C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREFI = 3.9 µs.
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.

3.2 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
EEPROM Supply Voltage	V_{DDSPD}	1.7	–	3.6	V	
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.125	–	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	–	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5	–	5	µA	3)

1 Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2 Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\,(DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
3 For any pin on the DIMM connector under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V.

4.0 I_{DD} Specifications and Conditions

4.1 512 MByte Registered Module HYS72T64000[G/H] (one rank, nine components x8)

512 MByte HYS72T64000[G/H]		PC2-3200R "-5"	PC2-4300R "-3.7"		
Symbol	Parameter / Condition	max.	max.	Unit	Note
I_{DD0}	Operating Current	745	918	mA	1
I_{DD1}	Operating Current	790	1008	mA	1
I_{DD2P}	Precharge PD Standby Current	286	369	mA	1
I_{DD2N}	Precharge Standby Current	538	639	mA	1
I_{DD2Q}	Precharge Quiet Standby Current	475	603	mA	1
$I_{DD3P(0)}$	Active PD Standby Current	367	477	mA	1
$I_{DD3P(1)}$	LP Active PD Standby Current	295	378	mA	1
I_{DD3N}	Active Standby Current	565	693	mA	1
I_{DD4R}	Operating Current Burst Read	880	1143	mA	1
I_{DD4W}	Operating Current Burst Write	925	1188	mA	1
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	1330	1503	mA	1
I_{DD5D}	Auto-Refresh Current (tREFI)	304	387	mA	1
I_{DD6}	Self-Refresh Current	36	36	mA	1
I_{DD7}	Operating Current	1420	1593	mA	1

Note: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled. Currents includes Registers and PLL.

4.2 1024 MByte Registered Module HYS72T128020[G/H] (two ranks, 18 components x8)

1024 MByte HYS72T128020[G/H]		PC2-3200R "-5"	PC2-4300R "-3.7"		
Symbol	Parameter / Condition	max.	max.	Unit	Note
I_{DD0}	Operating Current	899	1111	mA	1, 2
I_{DD1}	Operating Current	944	1201	mA	1, 2
I_{DD2P}	Precharge PD Standby Current	440	562	mA	1, 3
I_{DD2N}	Precharge Standby Current	944	1210	mA	1, 3
I_{DD2Q}	Precharge Quiet Standby Current	818	1030	mA	1, 3
$I_{DD3P(0)}$	Active PD Standby Current	602	778	mA	1, 3
$I_{DD3P(1)}$	LP Active PD Standby Current	458	580	mA	1, 3
I_{DD3N}	Active Standby Current	998	1210	mA	1, 3
I_{DD4R}	Operating Current Burst Read	1034	1336	mA	1, 2
I_{DD4W}	Operating Current Burst Write	1079	1381	mA	1, 2
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	1484	1696	mA	1, 2
I_{DD5D}	Auto-Refresh Current (tREFI)	476	598	mA	1, 3
I_{DD6}	Self-Refresh Current	72	72	mA	1, 3
I_{DD7}	Operating Current	1574	1786	mA	1, 2

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled. Currents includes Registers and PLL.
2) The other rank is in IDD2P Precharge Power-Down Standby Current mode
3) Both ranks are in the same IDD current mode

4.3 1024 Mbyte Registered Module HYS72T128000[G/H] (one rank, 18 components x4)

1024 MByte HYS72T128000[G/H]		PC2-3200R "-5"	PC2-4300R "-3.7"		
Symbol	Parameter / Condition	max.	max.	Unit	Note
I_{DD0}	Operating Current	1358	1660	mA	1
I_{DD1}	Operating Current	1448	1840	mA	1
I_{DD2P}	Precharge PD Standby Current	440	562	mA	1
I_{DD2N}	Precharge Standby Current	944	1210	mA	1
I_{DD2Q}	Precharge Quiet Standby Current	818	1030	mA	1
$I_{DD3P(0)}$	Active PD Standby Current	602	778	mA	1
$I_{DD3P(1)}$	LP Active PD Standby Current	458	580	mA	1
I_{DD3N}	Active Standby Current	998	1210	mA	1
I_{DD4R}	Operating Current Burst Read	1628	2110	mA	1
I_{DD4W}	Operating Current Burst Write	1718	2200	mA	1
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	2528	2830	mA	1
I_{DD5D}	Auto-Refresh Current (tREFI)	476	598	mA	1
I_{DD6}	Self-Refresh Current	72	72	mA	1
I_{DD7}	Operating Current	2708	3010	mA	1

Note: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled. Currents includes Registers and PLL.

4.4 2048 MByte Registered Module HYS72T256[0/2]20[G/H] (two ranks, 36 components x4)

2048 MByte HYS72T256020[G/H] 2048 MByte HYS72T256220[G/H]		PC2-3200R "-5"	PC2-4300R "-3.7"		
Symbol	Parameter / Condition	max.	max.	Unit	Note
I_{DD0}	Operating Current	1394	1696	mA	1, 2
I_{DD1}	Operating Current	1520	1912	mA	1, 2
I_{DD2P}	Precharge PD Standby Current	512	623	mA	1, 3
I_{DD2N}	Precharge Standby Current	1520	1930	mA	1, 3
I_{DD2Q}	Precharge Quiet Standby Current	1268	1570	mA	1, 3
$I_{DD3P(0)}$	Active PD Standby Current	836	1066	mA	1, 3
$I_{DD3P(1)}$	LP Active PD Standby Current	548	670	mA	1, 3
I_{DD3N}	Active Standby Current	1628	1930	mA	1, 3
I_{DD4R}	Operating Current Burst Read	1700	2182	mA	1, 2
I_{DD4W}	Operating Current Burst Write	1790	2272	mA	1, 2
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	2600	2902	mA	1, 2
I_{DD5D}	Auto-Refresh Current (tREFI)	584	706	mA	1, 3
I_{DD6}	Self-Refresh Current	144	144	mA	1, 3
I_{DD7}	Operating Current	2780	3082	mA	1, 2

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled. Currents includes Registers and PLL.
2) The other rank is in IDD2P Precharge Power-Down Standby Current mode
3) Both ranks are in the same IDD current mode

4.5 I_{DD} Measurement Conditions

(V_{DD} = 1.8V ± 0.1V; V_{DDQ} = 1.8V ± 0.1V)

Symbol	Parameter/Condition
I_{DD0}	**Operating Current - One bank Active - Precharge** $t_{CK} = t_{CKmin.}$; $t_{RC} = t_{RCmin.}$; tRAS = tRASmin., CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.
I_{DD1}	**Operating Current - One bank Active - Read - Precharge** IOUT = 0 mA, BL = 4, $t_{CK} = t_{CKmin.}$, tRC = tRCmin., tRAS = tRASmin.,tRCD = tRCDmin.,AL = 0, CL = CLmin.; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.
I_{DD2P}	**Precharge Power-Down Current:** All banks idle; CKE is LOW; $t_{CK} = t_{CKmin.}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.
I_{DD2N}	**Precharge Standby Current**: All banks idle; $\overline{CS}$ is HIGH, CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD2Q}	**Precharge Quiet Standby Current**: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.
$I_{DD3P(0)}$	**Active Power-Down Current**: All banks open; $t_{CK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to "0" (Fast Power-down Exit);
$I_{DD3P(1)}$	**Active Power-Down Current**: All banks open; $t_{CK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to "1" (Slow Power-down Exit);
I_{DD3N}	**Active Standby Current**: All banks open; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax}$; tRP = tRPmin.,CKE is HIGH; $\overline{CS}$ is high between valid commands. Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD4R}	**Operating Current - Burst Read:** All banks open; Continuous burst reads; BL = 4; $_{AL = 0}$, CL = CLmin.; $t_{CK} = t_{CKmin.}$; tRAS = tRASmax., tRP = tRPmin.; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0mA.
I_{DD4W}	**Operating Current - Burst Write:** All banks open; Continuous burst writes; BL = 4; $_{AL = 0}$, CL = CLmin.; $t_{CK} = t_{CKmin.}$; tRAS = tRASmax., tRP = tRPmin.; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;
I_{DD5B}	**Burst Auto-Refresh Current**: $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{RFCmin.}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD5D}	**Distributed Auto-Refresh Current**: $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET = Low. IDD6 current values are guaranteed up to TCASE of 85oC max.
I_{DD7}	**All Bank Interleave Read Current:** 1. All banks are being interleaved at minimum tRC without violating tRRD using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. Iout = 0mA. 2. Timing pattern: - ***DDR2 -400***: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D - ***DDR2 -533***: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D - ***DDR2 -667***: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D 3. Legend: A = Activate, RA = Read with Auto-Precharge, D=DESELECT

Notes:

1. IDD specifications are tested after the device is properly initialized and IDD parameter are specified with ODT disabled.
2. Definitions for IDD:
   LOW is defined as VIN <= VIL(ac)max; HIGH is defined as VIN >= VIH(ac)min.
   STABLE is defined as inputs are stable at a HIGH or LOW level.
   FLOATING is defined as inputs are VREF = VDDQ / 2.
   SWITCHING is defined as:
   inputs are changing between HIGH and LOW every other clock (once per two cycles) for address and control signals, and inputs changing between HIGH and LOW every other clock (once per cycle) for DQ signals not including mask or strobes.
3. IDD1, IDD4R, and IDD7 current measurements are defined with the outputs disabled (Iout = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
3. For two rank modules: For all active current measurements the other rank is in Precharge Power-Down Mode IDD2P
4. RESET signal is high for all currents, except for IDD6 "Self Refresh".
5. All current measurements includes Register and PLL current consumption.

4.5 I_{DD} Measurement Conditions (cont'd)

For testing the IDD parameters, the following timing parameters are used:

Parameter		Symbol	PC2-3200R "-5"	PC2-4300R "-3.7"	Unit
			3-3-3	4-4-4	
CAS Latency		CLmin	3	4	tCK
Clock Cycle Time		tCKmin	5	3.75	ns
Active to Read or Write delay		tRCDmin	15	15	ns
Active to Active / Auto-Refresh command period		tRCmin	60	60	ns
Active bank A to Active bank B command delay	x4 & x8	tRRDmin	7.5	7.5	ns
Active to Precharge Command		tRASmin	45	45	ns
Precharge Command Period		tRPmin	15	15	ns
Auto-Refresh to Active / Auto-Refresh command period		tRFCmin	105	105	ns
Average periodic Refresh interval		tREFI	7.8	7.8	µs

4.6 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a "week" or "strong" termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving "0" or "1", as long a ODT is enabled during a given period of time.

ODT current per terminated pin:

		EMRS(1) State	min.	typ.	max.	Unit
Enabled ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING	IODTO	A6 = 0, A2 = 1	5	6	7.5	mA/DQ
		A6 = 1, A2 = 0	2.5	3	3.75	mA/DQ
Active ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	IODTT	A6 = 0, A2 = 1	10	12	15	mA/DQ
		A6 = 1, A2 = 0	5	6	7.5	mA/DQ
note: For power consumption calculations the ODT duty cycle has to be taken into account						

5.0 Electrical Characteristics & AC Timings

5.1 AC Timing Parameter by Speed Grade (Component level data, for reference only)

Symbol	Parameter		-5 DDR2-400		-3.7 DDR2-533		Unit
			Min	Max	Min	Max	
t_{AC}	DQ output access time from CK / $\overline{CK}$		– 600	+ 600	-500	+500	ps
t_{DQSCK}	DQS output access time from CK / $\overline{CK}$		– 500	+ 500	–450	+450	ps
t_{CH}	CK, $\overline{CK}$ high-level width		0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	CK, $\overline{CK}$ low-level width		0.45	0.55	0.45	0.55	t_{CK}
t_{HP}	Clock Half Period		min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		
t_{CK}	Clock cycle time	CL = 3	5000	8000	5000	8000	ps
		CL = 4 & 5	5000	8000	3750	8000	ps
t_{IS}	Address and control input setup time		600	-	600	-	ps
t_{IH}	Address and control input hold time		600	-	600	-	ps
t_{DS}	DQ and DM input setup time		400	-	350	-	ps
t_{DH}	DQ and DM input hold time		400	-	350	-	ps
t_{IPW}	Control and Addr. input pulse width (each input)		0.6	-	0.6	-	t_{CK}
t_{DIPW}	DQ and DM input pulse width (each input)		0.35	-	0.35	-	t_{CK}
t_{HZ}	Data-out high-impedance time from CK / $\overline{CK}$		-	tACmax	-	tACmax	ps
$t_{LZ(DQ)}$	DQ low-impedance from CK / $\overline{CK}$		2*tACmin	tACmax	2*tACmin	tACmax	ps
$t_{LZ(DQS)}$	DQS low-impedance from CK / $\overline{CK}$		tACmin	tACmax	tACmin	tACmax	ps
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)		-	350	-	300	ps
t_{QHS}	Data hold skew factor		-	450	-	400	ps
t_{QH}	Data Output hold time from DQS		$t_{HP-tQHS}$	-	$t_{HP-tQHS}$	-	
t_{DQSS}	Write command to 1st DQS latching transition		WL -0.25	WL +0.25	WL -0.25	WL +0.25	t_{CK}
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35	-	0.35	-	t_{CK}
t_{DSS}	DQS falling edge to CLK setup time (write cycle)		0.2	-	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CLK (write cycle)		0.2	-	0.2	-	t_{CK}
t_{MRD}	Mode register set command cycle time		2	-	2	-	t_{CK}
t_{WPRE}	Write preamble		0.25	-	0.25	-	t_{CK}
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	t_{CK}
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	t_{CK}
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	t_{CK}
t_{RAS}	Active to Precharge command		45	70000	45	70000	ns
t_{RC}	Active to Active/Auto-refresh command period		60	-	60	-	ns
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		105	-	105	-	ns

Symbol	Parameter		-5 DDR2-400		-3.7 DDR2-533		Unit
			Min	Max	Min	Max	
t_{RCD}	Active to Read or Write delay (with and without Auto-Pre-charge) delay		15	-	15	-	ns
t_{RP}	Precharge command period		15	-	15	-	ns
t_{RRD}	Active bank A to Active bank B command	x4 & x8 (1k page size)	7.5	-	7.5	-	ns
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B Command Period		2	-	2	-	t_{CK}
t_{WR}	Write recovery time		15	-	15	-	ns
t_{DAL}	Auto precharge write recovery + precharge time		WR+tRP	-	WR+tRP	-	t_{CK}
t_{WTR}	Internal write to read command delay		10	-	7.5	-	ns
t_{RTP}	Internal read to precharge command delay		7.5	-	7.5	-	ns
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)		2	-	2	-	t_{CK}
t_{XARDS}	Exit active power-down mode to read command (slew exit, lower power)		6 - AL	-	6 - AL	-	t_{CK}
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)		2	-	2	-	t_{CK}
t_{XSRD}	Exit Self-Refresh to read command		200	-	200	-	t_{CK}
t_{XSNR}	Exit Self-Refresh to non-read command		tRFC + 10	-	tRFC + 10	-	ns
t_{CKE}	CKE minimum high and low pulse width		3	-	3	-	t_{CK}
t_{OIT}	OCD drive mode output delay		0	12	0	12	ns
t_{DELAY}	Minimum time clocks remain ON after CKE asynchro-nously drops low		tIS+tCK +tIH	-	tIS+tCK +tIH	-	ns
t_{REFI}	Average Periodic Refresh Interval	0°C - 85°C	-	7.8	-	7.8	µs
		85°C - 95°C	-	3.9	-	3.9	

1. For details and notes see the relevant INFINEON component datasheet
2. Timing definition and values for tis, tih, tds and tdh may change due to actual JEDEC work. This may also effect the SPD code for these parameters.

5.2 ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

Symbol	Parameter / Condition		min.	max.	Units
t_{AOND}	ODT turn-on delay		2	2	t_{CK}
t_{AON}	ODT turn-on	DDR2-400/533	tAC(min)	tAC(max) + 1 ns	ns
		DDR2-667	tAC(min)	tAC(max) + 0.7 ns	
t_{AONPD}	ODT turn-on (Power-Down Modes)		tAC(min) + 2 ns	2 t_{CK} + tAC(max) + 1 ns	ns
t_{AOFD}	ODT turn-off delay		2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off		tAC(min)	tAC(max) + 0.6 ns	ns
t_{AOFPD}	ODT turn-off delay (Power-Down Modes)		tAC(min) + 2 ns	2.5 t_{CK} + tAC(max) + 1 ns	ns
t_{ANPD}	ODT to Power Down Mode Entry Latency		3	-	t_{CK}
t_{AXPD}	ODT Power Down Exit Latency		8	-	t_{CK}

6.0 Serial Presence Detect Codes for Registered Modules

6.1 SPD Codes for PC2–4300R (–3.7)

Product Type		HYS72T256020GR–3.7–A HYS72T256020HR–3.7–A	HYS72T128000GR–3.7–A HYS72T128000HR–3.7–A	HYS72T128020GR–3.7–A HYS72T128020HR–3.7–A	HYS72T64000GR–3.7–A HYS72T64000HR–3.7–A
Organization		**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**
		2 Ranks (×4)	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–4300R–444**			
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E
4	Number of Column Addresses	0B	0B	0A	0A
5	DIMM Rank and Stacking Information	61	60	61	60
6	Data Width	48	48	48	48
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D	3D	3D
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	02	02	02	02
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	04	04	08	08
14	Error Checking SDRAM Width	04	04	08	08
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	Not used	00	00	00	00
20	DIMM Type Information	01	01	01	01
21	DIMM Attributes	07	05	05	04
22	Component Attributes	01	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50	50
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60	60	60
27	$t_{RP.min}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.min}$ [ns]	1E	1E	1E	1E

Product Type		HYS72T256020GR–3.7–A HYS72T256020HR–3.7–A	HYS72T128000GR–3.7–A HYS72T128000HR–3.7–A	HYS72T128020GR–3.7–A HYS72T128020HR–3.7–A	HYS72T64000GR–3.7–A HYS72T64000HR–3.7–A
Organization		**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**
		2 Ranks (×4)	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–4300R–444**			
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
29	$t_{RCD.min}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	01	01	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	25	25	25
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	37	37	37
34	$t_{DS.min}$ [ns]	10	10	10	10
35	$t_{DH.min}$ [ns]	22	22	22	22
36	$t_{WR.min}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.min}$ [ns]	1E	1E	1E	1E
38	$t_{RTP.min}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80	80
44	$t_{DQSQ.max}$ [ns]	1E	1E	1E	1E
45	$t_{QHS.max}$ [ns]	28	28	28	28
46	PLL Relock Time	0F	0F	0F	0F
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51	51	51
48	Psi(T-A) DRAM	78	78	78	78
49	ΔT_0	3E	3E	3E	3E
50	ΔT_{2N} (UDIMM) or ΔT_{2Q} (RDIMM)	22	22	22	22
51	ΔT_{2P}	1E	1E	1E	1E
52	ΔT_{3N}	1E	1E	1E	1E
53	$\Delta T_{3P.fast}$	24	24	24	24
54	$\Delta T_{3P.slow}$	17	17	17	17
55	ΔT_{4R} / ΔT_{4R4W} Sign	34	34	34	34
56	ΔT_{5B}	1E	1E	1E	1E
57	ΔT_7	20	20	20	20
58	Psi(ca) PLL	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C
60	ΔT_{PLL}	61	61	61	61

Product Type		HYS72T256020GR–3.7–A HYS72T256020HR–3.7–A	HYS72T128000GR–3.7–A HYS72T128000HR–3.7–A	HYS72T128020GR–3.7–A HYS72T128020HR–3.7–A	HYS72T64000GR–3.7–A HYS72T64000HR–3.7–A
Organization		**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**
		2 Ranks (×4)	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–4300R–444**			
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
61	ΔT_{REG} / Toggle Rate	78	78	78	78
62	SPD Revision	11	11	11	11
63	Checksum of Bytes 0-62	8E	8B	12	10
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37
74	Product Type, Char 2	32	32	32	32
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	32	31	31	36
77	Product Type, Char 5	35	32	32	34
78	Product Type, Char 6	36	38	38	30
79	Product Type, Char 7	30	30	30	30
80	Product Type, Char 8	32	30	32	30
81	Product Type, Char 9	30	30	30	47 / 48
82	Product Type, Char 10	47 / 48	47 / 48	47 / 48	52
83	Product Type, Char 11	52	52	52	33
84	Product Type, Char 12	33	33	33	2E
85	Product Type, Char 13	2E	2E	2E	37
86	Product Type, Char 14	37	37	37	41
87	Product Type, Char 15	41	41	41	20
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	0x	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx	xx

Product Type		HYS72T256020GR–3.7–A HYS72T256020HR–3.7–A	HYS72T128000GR–3.7–A HYS72T128000HR–3.7–A	HYS72T128020GR–3.7–A HYS72T128020HR–3.7–A	HYS72T64000GR–3.7–A HYS72T64000HR–3.7–A
Organization		**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**
		2 Ranks (×4)	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–4300R–444**			
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

6.2 SPD Codes for PC2–3200R (–5)

Product Type		HYS72T256020GR–5–A HYS72T256020HR–5–A	HYS72T256220GR–5–A HYS72T256220HR–5–A	HYS72T128000GR–5–A HYS72T128000HR–5–A	HYS72T128020GR–5–A HYS72T128020HR–5–A	HYS72T64000GR–5–A HYS72T64000HR–5–A
Organization		**2 GByte**	**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200R–333**				
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E	0E
4	Number of Column Addresses	0B	0B	0B	0A	0A
5	DIMM Rank and Stacking Information	61	61	60	61	60
6	Data Width	48	48	48	48	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	60	60	60	60	60
11	Error Correction Support (non-ECC, ECC)	02	02	02	02	02
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	04	04	04	08	08
14	Error Checking SDRAM Width	04	04	04	08	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	Not used	00	00	00	00	00
20	DIMM Type Information	01	01	01	01	01
21	DIMM Attributes	07	07	05	05	04
22	Component Attributes	01	01	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	50	50	50	50	50
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	60	60	60	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60	60	60	60

Product Type		HYS72T256020GR–5–A HYS72T256020HR–5–A	HYS72T256220GR–5–A HYS72T256220HR–5–A	HYS72T128000GR–5–A HYS72T128000HR–5–A	HYS72T128020GR–5–A HYS72T128020HR–5–A	HYS72T64000GR–5–A HYS72T64000HR–5–A
Organization		**2 GByte**	**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200R–333**				
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
27	$t_{RP.min}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.min}$ [ns]	1E	1E	1E	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	01	01	01	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	35	35	35	35	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	47	47	47	47	47
34	$t_{DS.min}$ [ns]	15	15	15	15	15
35	$t_{DH.min}$ [ns]	27	27	27	27	27
36	$t_{WR.min}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.min}$ [ns]	28	28	28	28	28
38	$t_{RTP.min}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.max}$ [ns]	23	23	23	23	23
45	$t_{QHS.max}$ [ns]	2D	2D	2D	2D	2D
46	PLL Relock Time	0F	0F	0F	0F	0F
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51	51	51	51
48	Psi(T-A) DRAM	78	78	78	78	78
49	ΔT_0	32	32	32	32	32
50	ΔT_{2N} (UDIMM) or ΔT_{2Q} (RDIMM)	1D	1D	1D	1D	1D
51	ΔT_{2P}	1E	1E	1E	1E	1E
52	ΔT_{3N}	1B	1B	1B	1B	1B
53	$\Delta T_{3P.fast}$	1E	1E	1E	1E	1E
54	$\Delta T_{3P.slow}$	17	17	17	17	17
55	ΔT_{4R} / ΔT_{4R4W} Sign	28	28	28	28	28
56	ΔT_{5B}	1B	1B	1B	1B	1B
57	ΔT_7	1E	1E	1E	1E	1E
58	Psi(ca) PLL	C4	C4	C4	C4	C4

Product Type		HYS72T256020GR–5–A HYS72T256020HR–5–A	HYS72T256220GR–5–A HYS72T256220HR–5–A	HYS72T128000GR–5–A HYS72T128000HR–5–A	HYS72T128020GR–5–A HYS72T128020HR–5–A	HYS72T64000GR–5–A HYS72T64000HR–5–A
Organization		**2 GByte**	**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200R–333**				
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
59	Psi(ca) REG	8C	8C	8C	8C	8C
60	ΔT_{PLL}	59	59	59	59	59
61	ΔT_{REG} / Toggle Rate	5C	5C	5C	5C	5C
62	SPD Revision	11	11	11	11	11
63	Checksum of Bytes 0-62	C3	C3	C0	47	45
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37	37
74	Product Type, Char 2	32	32	32	32	32
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	32	32	31	31	36
77	Product Type, Char 5	35	35	32	32	34
78	Product Type, Char 6	36	36	38	38	30
79	Product Type, Char 7	30	32	30	30	30
80	Product Type, Char 8	32	32	30	32	30
81	Product Type, Char 9	30	30	30	30	47 / 48
82	Product Type, Char 10	47 / 48	47 / 48	47 / 48	47 / 48	52
83	Product Type, Char 11	52	52	52	52	35
84	Product Type, Char 12	35	35	35	35	41
85	Product Type, Char 13	41	41	41	41	20
86	Product Type, Char 14	20	20	20	20	20
87	Product Type, Char 15	20	20	20	20	20
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	0x	0x	2x	2x	2x

Product Type		HYS72T256020GR–5–A HYS72T256020HR–5–A	HYS72T256220GR–5–A HYS72T256220HR–5–A	HYS72T128000GR–5–A HYS72T128000HR–5–A	HYS72T128020GR–5–A HYS72T128020HR–5–A	HYS72T64000GR–5–A HYS72T64000HR–5–A
Organization		**2 GByte**	**2 GByte**	**1 GByte**	**1 GByte**	**512 MB**
		×72	**×72**	**×72**	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**1 Rank (×4)**	**2 Ranks (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200R–333**				
Jedec SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

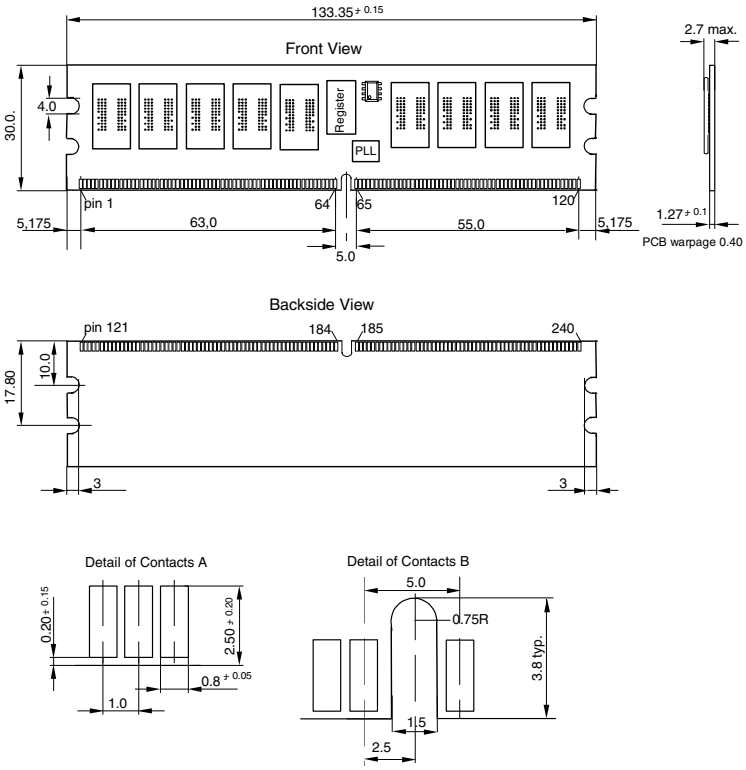
7.0 Package Outline

7.1 Raw Card A

Module Package

DDR2 Registered DIMM Modules Raw Card A

one physical rank, 9 components x8 organised



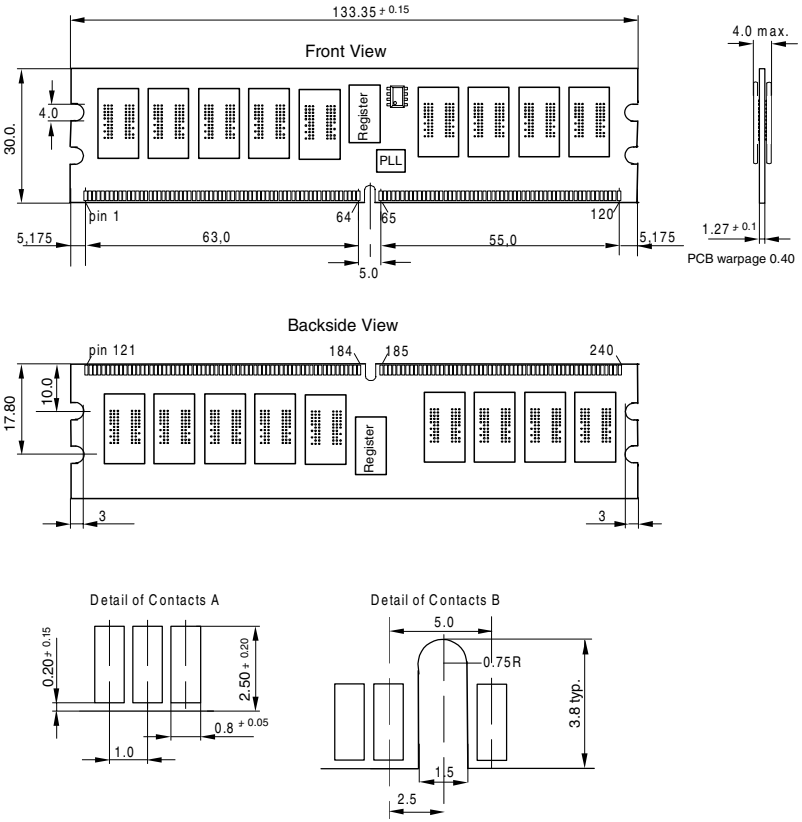
note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO-237)

7.2 Raw Card B

Module Package

DDR2 Registered DIMM Modules Raw Card B

two one physical rank, 18 components x8 organised



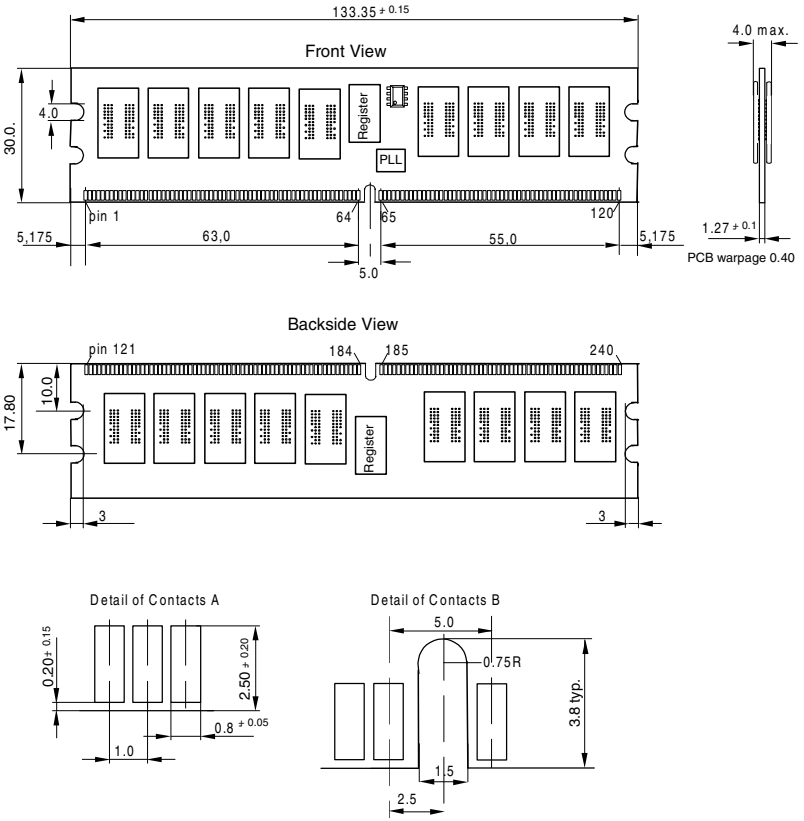
note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO-237)

7.3 Raw Card C

Module Package

DDR2 Registered DIMM Modules Raw Card C

one physical rank, 18 components x4 organised



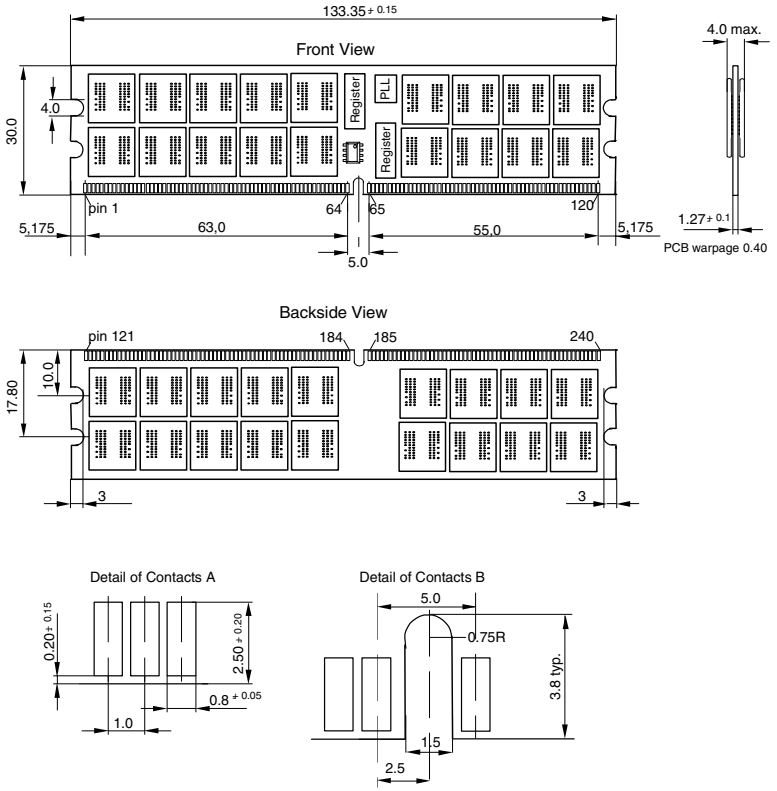
note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO-237)

7.4 Raw Card (tbd)

Module Package

DDR2 Registered DIMM Modules Raw Card (tbd.)

two physical ranks, 36 components x4 organised - planar version



note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO237)

8.0 Nomenclature (Modules & Components)

8.1 DDR2 DIMM Modules

	1	2	3	4	5	6	7	8	9	10	11
Example:	HYS	72	T	128	0	2	0	G	R	-5	-A

1	INFINEON Prefix	HYS for DIMM Modules	7	Product Variations	0 = standard 2 = dual die package
2	Module Data Width	64 = Non-ECC Modules 72 = ECC Modules	8	Package	G= BGA components
3	DRAM Technology	T = DDR2	9	Module Type	R = Registered DIMMs U = Unbuffered DIMMs DL = Small Outline DIMMs
4	Memory Density per I/O	64 = 64 Mb 128 = 128 Mb 256 = 256 Mb	10	Speed Grade	-5 = PC2-3200 (DDR2-400) -3.7 = PC2-4300 (DDR2-533) -3 = PC2-5400 (DDR2-667)
5	Raw Card Generation	0 = first generation	11	Die Revision	A = 1st Generation B = 2nd Generation C = 3rd Generation
6	Number of Memory Ranks	0 = One Rank 2 = Two Ranks	Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes.		

8.2 DDR2 Memory Components

	1	2	3	4	5	6	7	8	9
Example:	HYB	18	T	512	40	0	A	C	-5

1	INFINEON Component Prefix	HYB for DRAM Components	6	Product Variations	0 = standard 2 = dual die package
2	Power Supply Voltage	18 = 1.8 V Power Supply	7	Die Revision	A = 1st Generation B = 2nd Generation C = 3rd Generation
3	DRAM Technology	T = DDR2	8	Package Type	C = BGA package F = BGA package (lead and halogen free)
4	Memory Density	256 = 256 Mb 512 = 512 Mb 1G = 1024Mb	9	Speed Grade	-5 =...DDR2-400 -3.7 =.DDR2-533 -3 =...DDR2-667
5	Memory Organisation	40 = x4, 4 data in/outputs 80 = x8, 8 data in/outputs 16 = x16, 16 data in/outputs			