Calling Line Identification Receiver With Call Waiting

Features

- Compatible with Bellcore TR-NWT-000030 & SR-TSV-002476
- Bellcore "CPE Alerting Signal (CAS)" detection
- BELL 202 FSK demodulation
- Ring detection input and output
- Carrier detection output
- Low battery detection input and output
- Power down mode
- High input sensitivity
- 3.58MHz crystal or ceramic resonator

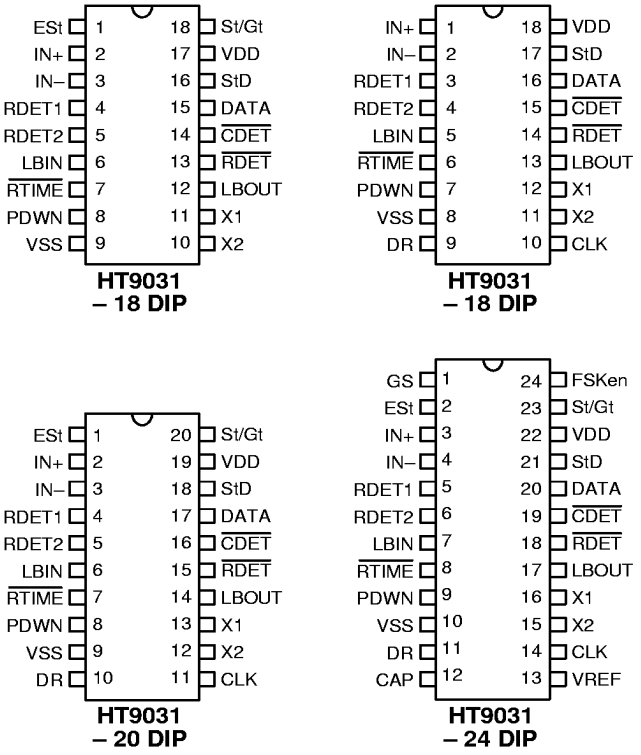
Applications

- Feature phones
- Adjunct boxes
- Fax and answering machines
- Computer interface products

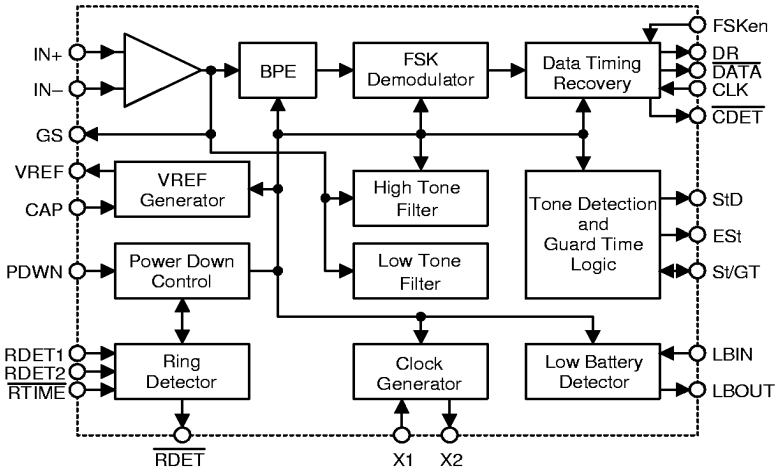
General Description

The HT9031 calling line identification receiver is a low power CMOS integrated circuit designed for receiving physical layer signals transmitted according to Bellcore TR-NWT-000030 & SR-TSV-002476 specifications. The device provides 1200 baud rate BELL 202 FSK demodulation. A 3-wire synchronous serial FSK data interface allows a micro controller to extract 8-bit data words from the device. The primary application for this device is in products that are to be used to receive and display the calling number, or message waiting indicator sent to subscribers from central office facilities. The device also provides a low battery detection circuit, a power down circuit, a carrier detection circuit and a ring detection circuit for easier system applications.

Package Information



Block Diagram



Pin Description

Pin Name	I/O	Description
IN+	I	Non-inverting input of the input Op-amp
IN–	I	Inverting input of the input Op-amp
GS	O	Gain select of the input Op-amp It is recommended that the Op-amp is set to a unity gain.
VREF	O	This reference voltage pin is normally set at VDD/2 to bias the input Op-amp.
CAP	—	A 0.1μF decoupling capacitor should be connected across this pin and VSS pin.
RDET1	I	It detects ring energy on the line through an attenuating network and enables the oscillator and ring detection circuitry.
RDET2	I	It couples ring signal to the precision ring detector through an attenuating network. $\overline{\text{RDET}}$="0" if a valid ring signal is detected.
LBIN	I	Input for low battery detector
$\overline{\text{RTIME}}$	O	An RC network may be connected to this pin in order to hold this pin voltage below 2.2V between the peaks of the ringing signal. This pin controls internal power up and activates partial circuitry needed to determine whether the incoming ring is valid or not.
PDWN	I	A logic "1" on this pin puts the chip in power down mode. When a logic "0" is on this pin, the chip is activated.
VSS	—	Power supply ground
X2	O	A 3.58MHz crystal or ceramic resonator should be connected to this pin and X1.
X1	I	A 3.58MHz crystal or ceramic resonator should be connected to this pin and X2.
LBOUT	O	This pin will be set to "1" when the voltage on LBIN pin is lower than the internal reference voltage. Otherwise this pin stays at "0".
FSKen	I	The pin internally pulled low by a 100KΩ can enable FSK demodulator circuit. When the FSK signal is not expected, a logic "0" should be put on this pin to disable the FSK demodulator and hence prevent the demodulator from reacting to extraneous signals such as speech, CAS signals and DTMF signals which are in the same frequency band as the FSK signal.
CLK	I	This is a clock pin internally pulled high by a 100KΩ. This pin, along with both DATA and $\overline{\text{DR}}$ pins, forms a 3-wire FSK interface circuit to and from a micro controller.
DATA	O	Serial data output corresponding to the FSK input A logic "1" on this pin represents mark; a logic "0" space.
$\overline{\text{DR}}$	O	This data ready pin is active low. It goes low after the demodulator demodulates the last bit of each word. Hence, it can be used to interrupt a micro controller and identifies the data (8-bit) boundary on the serial output stream.
$\overline{\text{RDET}}$	O	This open drain output goes low when a valid ringing signal is detected. When connected to PDWN pin, this pin can be used for auto power up.

Pin Name	I/O	Description
$\overline{\text{CDET}}$	O	This open drain output goes low indicating that a valid carrier is present on the line. An hysteresis is built-in to allow for a momentary drop out of the carrier. When connected to PDWN pin, this pin can be used for auto power up.
StD	O	CAS signal delayed steering output When high, it indicates that a guard time qualified alert signal has been detected.
ESt	O	CAS signal early steering output This is a active high signal to indicate that a valid CAS signal has been detected. This pin can be used in conjuction with St/GT and external circuitry to implement detect and non-detect guard times.
St/GT	I/O	CAS signal steering input/guard time A voltage greater than V_{TGT} detected at St causes the device to register the detected tone pair and update the output latch. On the other hand, a voltage less than V_{TGT} at this input frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant; its state is a function of ESt and the voltage on St.
VDD	—	Positive power supply

Absolute Maximum Ratings

Voltages referenced to VSS, except where noted.

DC Supply Voltage.....–0.5V to 6.0V
Power Dissipation.....25mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range .....–40°C to 150°C

DC Electrical Characteristics

(Crystal=3.58MHz, Ta=0~70°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	DC Supply Voltage	—	—	3.5	5	5.5	V
I_{STBY}	Stand-by Current	5V	PDWN=1, $\overline{\text{RTIME}}$=1 All outputs unloaded	—	—	1	μA
I_{DD1}	Operating Current	5V	PDWN=1, $\overline{\text{RTIME}}$=0 All outputs unloaded	—	1	—	mA
I_{DD2}	Operating Current	5V	PDWN=0, $\overline{\text{RTIME}}$=0 or 1, All outputs unloaded	—	3.5	—	mA
V_{IL}	Input Low Voltage	5V	—	—	—	$0.2V_{DD}$	V
V_{IH}	Input High Voltage	5V	—	$0.8V_{DD}$	—	—	V
I_{OL}	Output High Sourcing Current	5V	$V_{OH}=0.9V_{DD}$	0.8	—	—	mA
I_{OH}	Output Low Sinking Current	5V	$V_{OL}=0.1V_{DD}$	2	—	—	mA

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
I_{IN}	Input Leakage Current	5V	—	—	—	±1	μA
V_{T-}	Input Low Threshold Voltage	5V	—	—	2.2	—	V
V_{T+}	Input High Threshold Voltage	5V	—	—	2.9	—	V
V_{RD2}	RDET2 Threshold Voltage	5V	—	—	1.2	—	V
I_{OZ}	St/GT Output High-Z Current	5V	—	—	—	5	μA
V_{TGT}	St/GT Threshold Voltage	5V	—	$0.5V_{DD}$–0.05	—	$0.5V_{DD}$+0.05	V
V_{REF}	Reference Output Voltage	5V	No load	$0.5V_{DD}$–0.05	—	$0.5V_{DD}$+0.05	V

AC Electrical Characteristics

Gain Setting Amplifier

VDD=5V, VSS=0V, Crystal=3.58MHz, Ta=0 to 70°C, 0dBm=0.7746Vrms@600Ω

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{IN}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$	—	—	1	μA
R_{IN}	Input Resistance	—	—	10	—	MΩ
V_{OS}	Input Offset Voltage	—	—	—	25	mV
PSRR	Power Supply Rejection Ratio	1KHz ripple on V_{DD}	—	40	—	dB
CMRR	Common Mode Rejection	$V_{CMmin} \le V_{IN} \le V_{CMmax}$	—	40	—	dB
A_{VOL}	DC Open Loop Voltage Gain	—	—	32	—	dB
fc	Unity Gain Bandwidth	—	—	0.3	—	MHz
V_O	Output Voltage Swing	Load≥50KΩ	0.5	—	V_{DD}–0.5	V_{PP}
C_L	Max. Capacitive Load(GS)	—	—	—	100	pF
R_L	Max. Resistive Load(GS)	—	50	—	—	KΩ
V_{CM}	Common Mode Range Voltage	—	1	—	V_{DD}–1.0	V

FSK Detection

VDD=5V, VSS=0V, Crystal=3.58MHz, Ta=25°C, C_L=50pF, 0dBm=0.7746Vrms@600Ω

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Input Detection Level	—	–37.78	—	–5.78	dBm
	Transmission Rate	—	1188	1200	1212	baud
	Input Frequency Detection	Mark Space	1188 2178	1200 2200	1212 2222	Hz Hz
SNR	Input Noise Tolerance	—	—	20	—	dB

CPE Alerting Signal Detection

VDD=5V, VSS=0V, Crystal=3.58MHz, Ta=25°C, C_L=50pF, 0dBm=0.7746Vrms@600Ω

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_L	Low Tone Frequency	—	—	2130	—	Hz
f_H	High Tone Frequency	—	—	2750	—	Hz
f_{DA}	Frequency Deviation Accept	Range within which tones are accepted	1.1	—	—	%
f_{DR}	Frequency Deviation Reject	Range outside which tones are rejected	3.5	—	—	%
	Accept Signal Level per Tone	see note 4	–37.78	—	0.22	dBm
	Reject Signal Level per Tone	V_{DD}=5V see note 3	—	—	–43.78	dBm
	Positive and Negative Twist Accept	see note 5	7	—	—	dB
	Noise Tolerance	see note 1,2	—	20	—	dB
t_{DP}	Present Detect Time	—	5	16	22	ms
t_{DA}	Absent Detect Time	—	—	4	8	ms

Note:

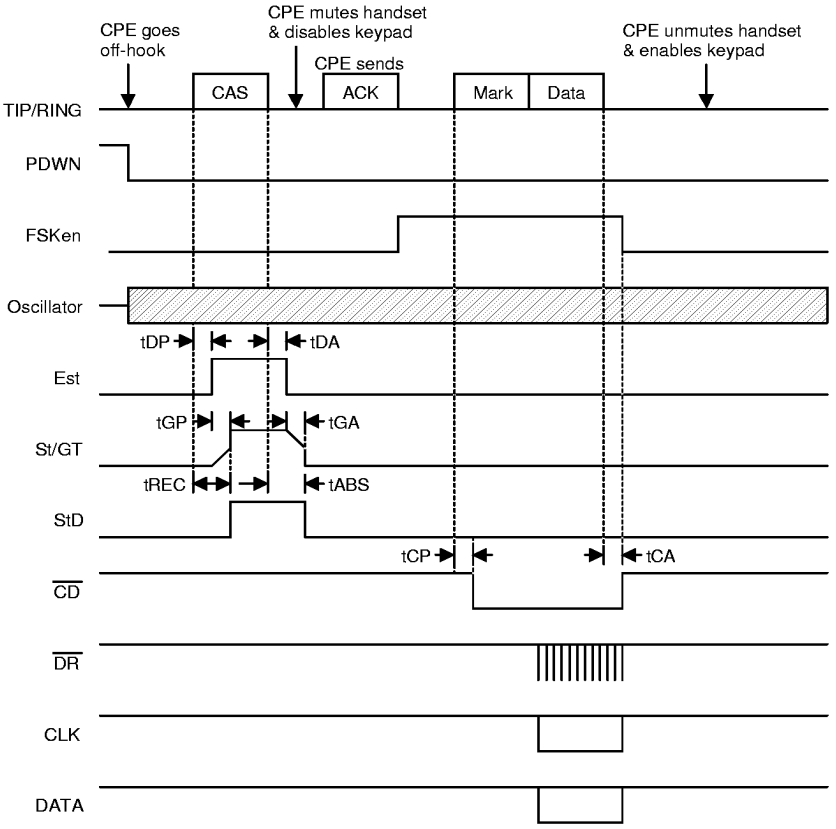
1. Both tones are at the nominal frequncies. Both tones have the same amplitude.
2. Noise tolerance is present only when CAS tones are present. Random noise is band limited to 300–3400Hz.
3. The maximum reject level will decrease by 1dB for every 1dB decrease in V_{DD} from 5V, and increase by 1dB for every 1dB V_{DD} increase over 5V.
4. dBm=decibels above or below a reference power of 1mW into 600Ω, 0dBm=0.7746Vrms@600Ω. Signal level is per tone.
5. Twist=20log($f_H$amplitude / f_L amplitude)

3-Wire Interface Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PU}	Power–Up Time	—	—	2	—	ms
t_{PD}	Power–Down Time	—	—	100	—	μs
t_{CP}	Input FSK to $\overline{CDET}$ Low Delay	—	—	—	25	ms
t_{CA}	Input FSK to $\overline{CDET}$ High Delay	—	8	—	—	ms
	$\overline{CDET}$ Hysteresis	—	8	—	—	ms
f_{CLK}	CLK Frequency	—	—	1	—	MHz
	CLK Duty Cycle	—	—	50	—	%
t_{R1}	CLK Rise Time	—	—	—	20	ns
t_{DDS}	CLK Low Setup to $\overline{DR}$	—	500	—	—	ns
t_{DDH}	CLK Low Hold Time $\overline{DR}$	—	500	—	—	ns
t_{RL}	$\overline{DR}$ Low Time	—	415	416	417	μs

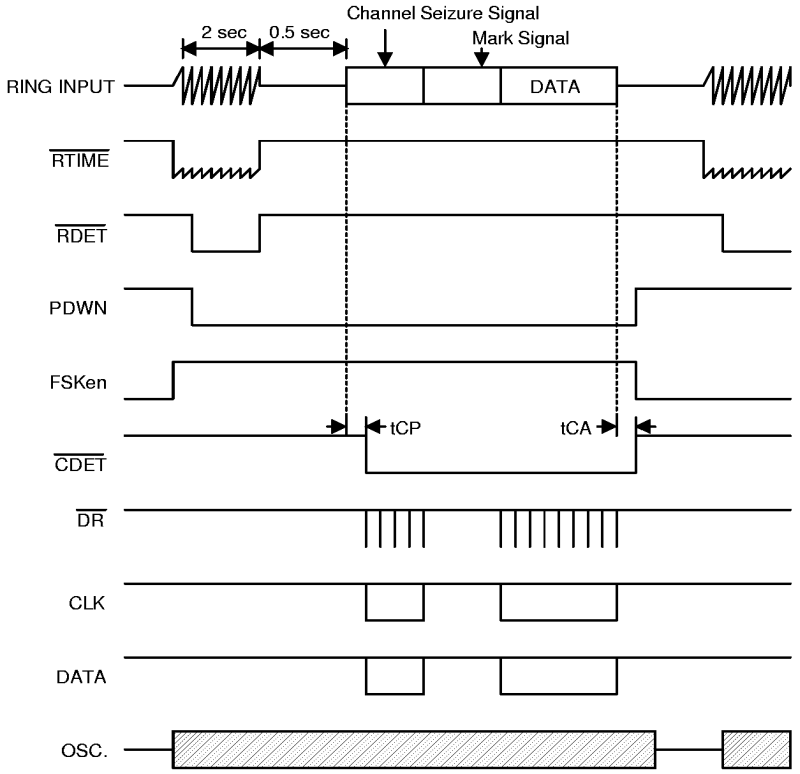
Timing Diagram

Timing for Bellcore Off-hook Data Transmission



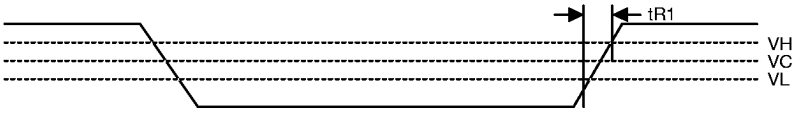
Notes:
1. Non-FSK signals such as CAS, speech and DTMF tones are in the same frequency band as FSK. They will be demodulated and give false data. The FSKen pin should be set low to disable the FSK demodulator when FSK is not expected.
2. FSKen may be set high as soon as the CPE has finished sending the acknowledgement signal ACK. tr-nwt-000575 specifies that ACK=DTMF D for non-ADSI CPE, ACK=DTMF A for ADSI CPE.
3. FSKen should be set low when carry detect pin has become inactive.
4. The total recognition time is tREC=tGP+tDP, where tGP is the tone present guard time and tDP is the tone present detect time.
5. The total tone absent time is tABS=tGA+tDA, where tGA is the tone absent guard time and tDA is the tone absent detect time.

Timing for Belleore On-hook Data Transmission Associated with Ringing



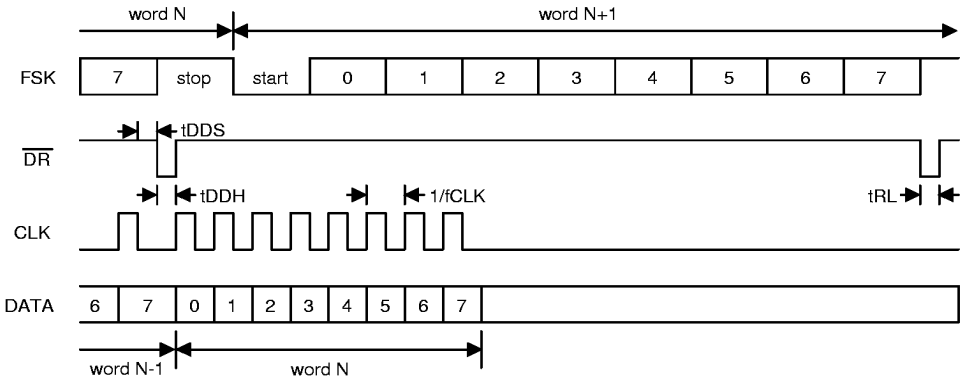
Notes:
1. The designer may choose to enable the chip only after the end of ringing to conserve power in a battery operated application. Carry detect output is not activated by ringing.
2. The designer may choose to set FSKen always high while the machine is on-hook. Setting FSKen low prevents the FSK demodulator from reacting to other in-band signals such as spech, CAS or DTMF tones.

CLK Input Timing



VH=0.9*VDD, VL=0.1*VDD, VC=0.5*VDD

Serial Data Interface Timing



Application Circuit