HT9020

Call Progress Tone Decoder & ABR Controller

Features

- Low cost 32768Hz crystal
- Low power consumption
- Operating voltage: 2.5V to 5.5V (CPT mode)
  2.0V to 5.5V (ABR mode)
- Call progress tone decoder
  - Fully decoded tristate call progress status output
  - Works with traditional precision or PBX call progress tones
- Busy redial controller
  - Repeat times: 3, 10 or 15 times
    (2, 5, 15 times by mask option)
  - 4.65, 32.6 and 62.8 sec break time
    (16.3sec by mask option)
  - Auto-terminate after 30 times (default) ringback tone receipt

General Description

The HT9020 provides two modes; Call progress tone decoder and Busy redial controller, to support the application fields.

Standard call progress tone decoder

This feature detects a specified input signal and then outputs relative envelopes during a 2.32sec interval. Three tristate output pins (DIAL, RBK, BUSY) indicate the presence of a dial tone, ringback tone or busy/reorder tone respectively, so it provides information that enables the microprocessor to decide whether to initiate, continue or terminate calls.

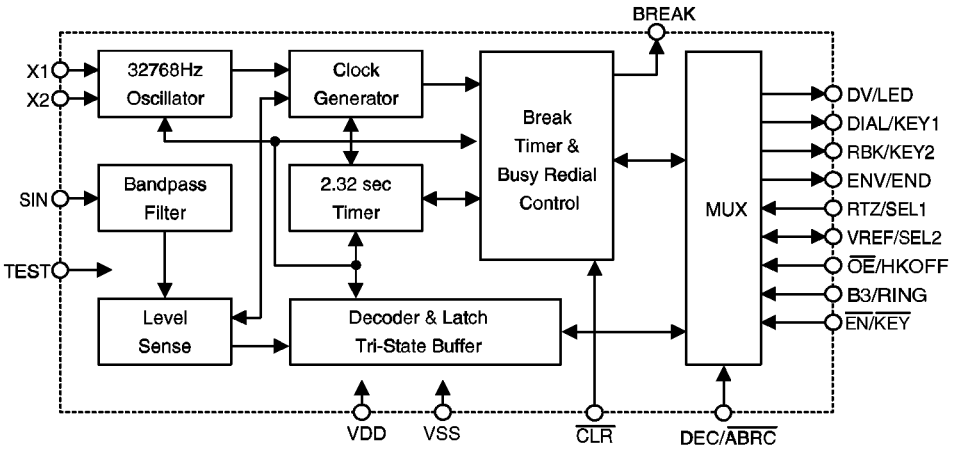
Busy redial controller

This feature implements a busy redial function. After decoding, if the line is busy, this device forces the dialer to break for 62.8 sec, then triggers the redial key after the dial tone receipt. If the receiver is still busy, the redial sequence will be repeated 10 times. If the receiver is ringing, the redial sequence will be terminated after 30 times of ringback tone receipt.

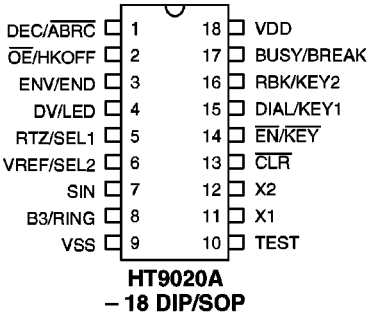
Selection Table

Function / Part No.	Operating Voltage	OSC Frequency	CPT Decoder	ABR Repeat Times	ABR Break Time	Package
HT9020A	CPT mode 2.5V~5.5V ABR mode 2.0V~5.5V	32768Hz	Full decoded	3/10/15 times [2/5/15 by metal option]	4.65/32.6/62.8 sec [16.3 sec by metal option]	18 DIP/SOP
HT9020B	CPT mode 2.5V~5.5V	32768Hz	CPT envelope only	—	—	8 DIP

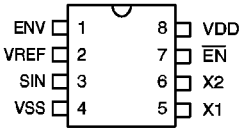
Block Diagram



Pin Assignment



HT9020A
– 18 DIP/SOP



HT9020B
– 8 DIP

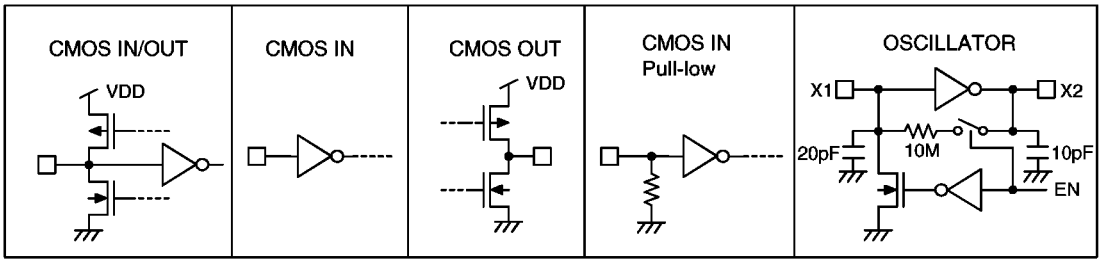
Pin Description

Pin Name	I/O	Internal Connection	Description
DEC/$\overline{\text{ABRC}}$	I	CMOS IN	When this pin is connected to V_{DD}, the chip is in the call progress tone decoder mode (**CPTD mode**) When this pin is connected to V_{SS}, the chip is in the auto busy redial controller mode (**ABRC mode**)
$\overline{\text{OE}}$/HKOFF	I	CMOS IN	**CPTD mode:** DIAL, RBK, BUSY and ENV pin tristate output control pin. $\overline{\text{OE}}$=V_{DD}: Tristate output selected **ABRC mode:** Off hook sense pin HKOFF=V_{DD}: Reset controller and disable ABR operation

Pin Name	I/O	Internal Connection	Description
ENV/END	O	CMOS OUT	**CPTD mode:** While an input signal is within specification, this pin will output the envelope relative to the input signal with a typical 40ms timing delay. **ABRC mode:** This is an ABR finished indicating signal output pin. When an ABR counter is full, this pin will output a 100ms pulse.
DV/LED	O	CMOS OUT	**CPTD mode:** The call progress tone is decoded in this ready output pin. This pin can be used to trigger a microcontroller to read the latched data at DIAL, RBK and BUSY **ABRC mode:** ABR indicating signal output. While ABR is active, this pin will output a 0.86Hz, 25% duty cycle clock.
RTZ/SEL1	I	CMOS IN	**CPTD mode:** Output data return to zero select pin RTZ=V_{DD}; The outputs of DIAL, RBK and BUSY will be cleared when the input signal is out of specification while in the 2.32 sec time window. RTZ=V_{SS}; The outputs of DIAL, RBK and BUSY will be latched until the next valid data is received. **ABRC mode:** Numbers of the busy redial and time of break selection pin.
VREF/SEL2	I/O	CMOS I/O (VREF:O SEL2:I)	**CPTD mode:** 1/2 V_{DD} reference voltage output pin When $\overline{EN}$=V_{DD}, the device will be turned off and VREF disabled. All outputs will be pulled low to reduce power consumption. **ABRC mode:** Number of the busy redial and time of break selection pin.
SIN	I	CMOS IN	AC coupled analog signal input pin
B3/RING	I	CMOS IN	**CPTD mode:** Received busy tone pattern select pin B3=V_{DD}; BUSY will be set after three successive busy tones are received. B3=V_{SS}; BUSY will be set immediately after a busy tone is received. **ABRC mode:** Ringer detection input pin
VSS	—	—	Negative power supply 2.5~5.5V for CPT mode operation 2.0~5.5V for ABR mode operation
VDD	—	—	Positive power supply, 2.5~5.5V for normal operation
BUSY/ BREAK	O	CMOS OUT	**CPTD mode:** BUSY=HIGH: The detected input signal is a busy or reorder tone **ABRC mode:** When in ABR mode, the BREAK pin will be high. After a busy tone is detected it will return low. When the break timer has timed out, it will return high.

Pin Name	I/O	Internal Connection	Description
RBK/KEY2	O	CMOS OUT	**CPTD mode:** RBK=HIGH: The detected input signal is a ringback tone. **ABRC mode:** Transmission gate input or output pin. Used to trigger the row and column pin of the redial key when a dial tone is received. It will output a 100ms pulse.
DIAL/KEY1	O	CMOS OUT	**CPTD mode:** DIAL=HIGH; The detected input signal is a dial tone. **ABRC mode:** Transmission gate input or output pin. Used to trigger the row and column pin of the redial key when a dial tone is received. It will output a 100ms pulse.
$\overline{EN}/\overline{KEY}$	I	CMOS IN	**CPTD mode:** $\overline{EN}$=V_{SS}; Normal operation mode $\overline{EN}$=V_{DD}; Device disabled. The oscillator stops and all output pins are pulled low or high impedance. **ABRC mode:** The pin is schmitt trigger input structure. Active low. Applying a negative going pulse to this pin can toggle the auto-busy-redial function.
$\overline{CLR}$	I	CMOS IN	When $\overline{CLR}$ is low and BREAK is high, the tone decoder is reset. This pin can be connected to the mute pin of the dialer IC for tone elimination.
X1	I	OSCILLATOR	The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on-chip. Connect a standard 32.768kHz crystal or ceramic resonator.
X2	O	OSCILLATOR	X1 and X2 terminals implement the oscillator function. The oscillator is turned off in the standby mode, and is actuated whenever a keyboard entry is detected.
TEST	I	CMOS IN Pull-low	For testing only, active high

Approximate internal connection circuits



Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 6V
Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature ..... –55°C to 150°C
Operating Temperature ..... –20°C to 75°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	CPT mode	2.5	—	5.5	V
			ABR mode	2.0	—	5.5	V
I_{DD}	Operating Current	5V	Functions enabled	—	—	2	mA
		2.5V	No load	—	—	0.8	mA
I_{STB}	Standby Current	2.5V	Functions disabled or $\overline{EN}$=1	—	—	1	μA
GDV	Detection Level	5V	f_{IN}=305~640Hz	–36	—	0	dBm
		2.5V	ENV=1	–42	—	–8	dBm
GRL	Rejection Level	—	All frequency, ENV=0	—	—	–50	dBm
f_{RL} f_{RH}	Rejection Out-band Frequency	—	V≤ 0 dBm, ENV=0	— 800	—	200 —	Hz
t_{DD}	Detection Signal Time	—	In-band signal input, ENV=1	40	—	—	ms
t_{RD}	Rejection Noise Time	—	Any signal input, ENV=0	—	—	20	ms
t_{DH} t_{DL}	Envelope Output Delay Time	—	Time to output high Time to output low	—	40	—	ms
t_{DV}	Data Valid Output Time	—	Time to output high/low	1.05	1.16	1.2	sec
t_{SU}	Data Setup Time	—	—	3	4	5	ms
t_I	Interval Time	—	Internal signal	—	2.32	—	sec
t_{IP}	Interval Pause Time	—	Internal signal	8		—	ms
t_{CL}	Clear Time	—	—	—	250	—	ns
t_{ST}	OSC Start Up Time	—	—	—	0.8	2	sec
Z_I	Input Impedance	—	f_{IN}=200~3.4kHz	1.0	—	—	MΩ
V_{REF}	Reference Voltage	—	No load	2.4	2.5	2.6	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Z_{REF}	Output Impedance	—	—	—	10	20	MΩ
V_{IH}	Logic Input High Voltage	5V	—	3.5	—	—	V
V_{IL}	Logic Input Low Voltage	5V	—	—	—	1.5	V
I_{IH}	Logic Input High Current	5V	V_{IH}=5.0V	—	—	0.1	μA
I_{IL}	Logic Input Low Current	5V	V_{IL}=0V	–0.1	—	—	
I_{OH}	Output High Current	5V	V_{OH}=4.5V	—	—	–0.5	mA
I_{OL}	Output Low Current	5V	V_{OL}=0.5V	2.0	—	—	mA
I_{LKH}	Output Disable Leakage Current	5V	V_{LKH}=5.0V	—	—	0.1	μA
I_{LKL}		5V	V_{LKL}=0V	–0.1	—	—	μA
I_{SO}	Pull Down Current	5V	—	—	25	35	μA
I_{DR}	Pull Up Current	5V	—	—	25	35	μA
GDL	Detection Level	2.5V	f_{IN}=305~640Hz	–42	—	–8	dBm
		5.0V		–36	—	0	dBm
GRL	Rejection Level	5V	All frequency	—	—	–50	dBm
f_{ROL}	Rejection Out-band Low Frequency	5V	V<0 dBm, ENV=0	—	—	200	Hz
f_{ROH}	Rejection Out-band High Frequency	5V	V<0 dBm, ENV=0	800	—	—	Hz
t_{DD1}	Detection Time	5V	In-band dial tone	2.1	3.32	3.0	sec
t_{DD2}	Detection Time	5V	In-band dial tone	6.5	7.0	8.0	sec
t_{DB}	Detection Busy Time	5V	In-band busy tone	6.8	7.5	8.2	sec
t_{DR}	Detection Ringer Time	5V	30 Times ringback tone (2 sec On/4 sec Off)	150	180	210	sec
t_{DN}	Detection Time	5V	No signal	25	30.2	35	sec
t_{DE}	Detection Enable Time	5V	—	0.2	30.2	35	sec
t_{TO}	RELI, O Turn on Time	5V	—	80	100	120	ms
t_O	ABREND Output Time	5V	—	80	100	120	ms
t_{B1}	Break Time (t_{B1}+2.3sec)	5V	After a busy tone is detected	60.0	62.8	65.0	sec
t_{B2}		5V	After no signal is detected	62.0	65.1	68.0	sec
RON	Transition on Resistor	5V	V_{RDLI}=5.0V, V_{RDLO}=0V	—	500	100	Ω
ROFF	Gate Output off Resistor	5V	V_{RDLI}=0V, V_{RDLO}=5.0V	10	—	—	MΩ

Functional Description

Decoder

The HT9020 call progress tone decoder (DEC/$\overline{ABRC}$=V_{DD}) can be used in the U.S.A. and many other countries in the world. The signal format, truth table and timing of the decoder are shown below.

The signal format of the call progress tone

Tone	Frequency	Condition
Precision Dial Tone	350Hz + 440Hz	Continuous
Old Dial Tone	120Hz(or 133Hz, ..) + 600Hz	Continuous
Precision Busy Tone	480Hz + 620Hz	0.5sec On and 0.5sec Off
Old Busy Tone	120Hz + 600Hz	0.5sec On and 0.5sec Off
Precision Reorder Tone	480Hz + 620Hz	0.3sec On and 0.2sec Off
Old Reorder Tone	120Hz + 600Hz	0.2sec On and 0.3sec Off or 0.25sec On and 0.25sec Off
Precision Ring-back Tone	440Hz + 480Hz	2sec On and 4sec Off
Old Ring-back Tone	40Hz (or the others) + 420Hz	2sec On and 4sec Off

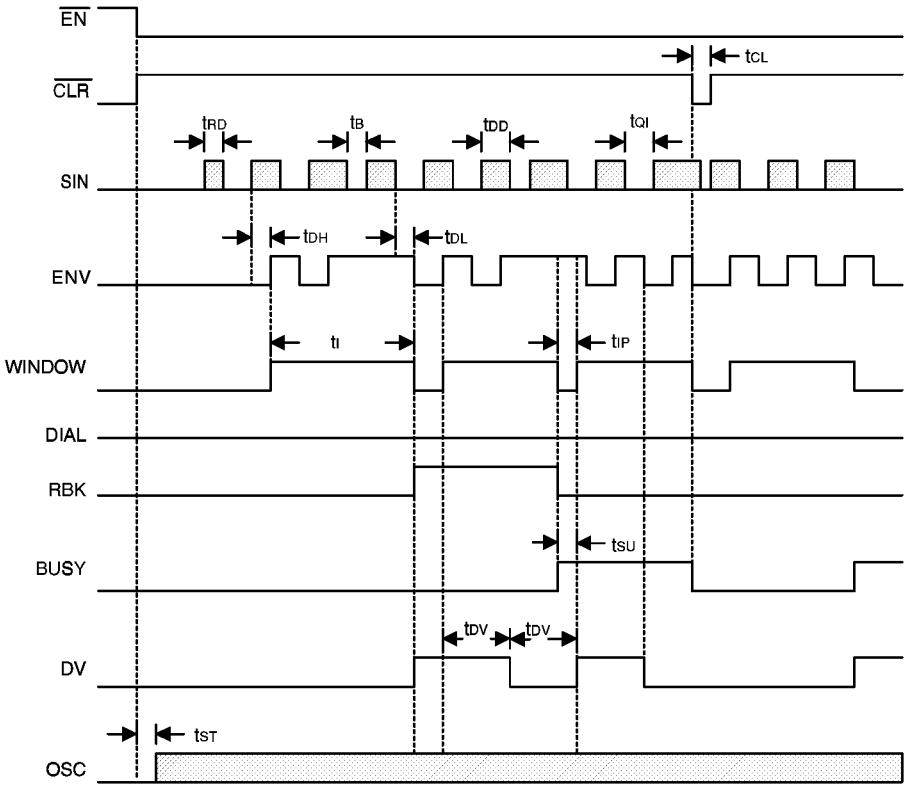
The truth table of the decoder

Tone	Transition No.	DIAL	RBK	BUSY	DV	$\overline{OE}$/HKOFF
Initial	—	0	0	0	0	0
Dial	1	1	0	0	1	0
Ringback	2~4	0	1	0	1	0
Busy/Reorder	5~16	0	0	1	1	0
Overflow	over 16	0	0	0	1	0
Output Disable	—	Hi-Z	Hi-Z	Hi-Z	*	1

Notes: Hi-Z: Hi impedance

*: previous state

Decoder timing diagrams



ABR controller

Initial state:

- RDLO=Hi-Impedance
- RDLI=Hi-Impedance
- BREAK=Low
- ABRI=Low

If a negative transition is received on the ABR pin, then the Auto-busy-dial function will be executed, and the LED pin will output a 0.86Hz (duty=0.25) clock. If the device detects a dial tone, KEY1 and KEY2 pins output a 100ms pulse to trigger the redial key of the telephone dialer. The dial tone will be ignored after the redial key is triggered.

If a busy/reorder tone for three successive windows is received or the line signal is off for 30.2secs or a dial tone appears again for more than 7 secs after the number is dialed-out, the device will turn on the internal register to implement the following control:

- Turn off the filter
- BREAK pin output low for on-hook switch control
- The on-hook timer starts counting the break time

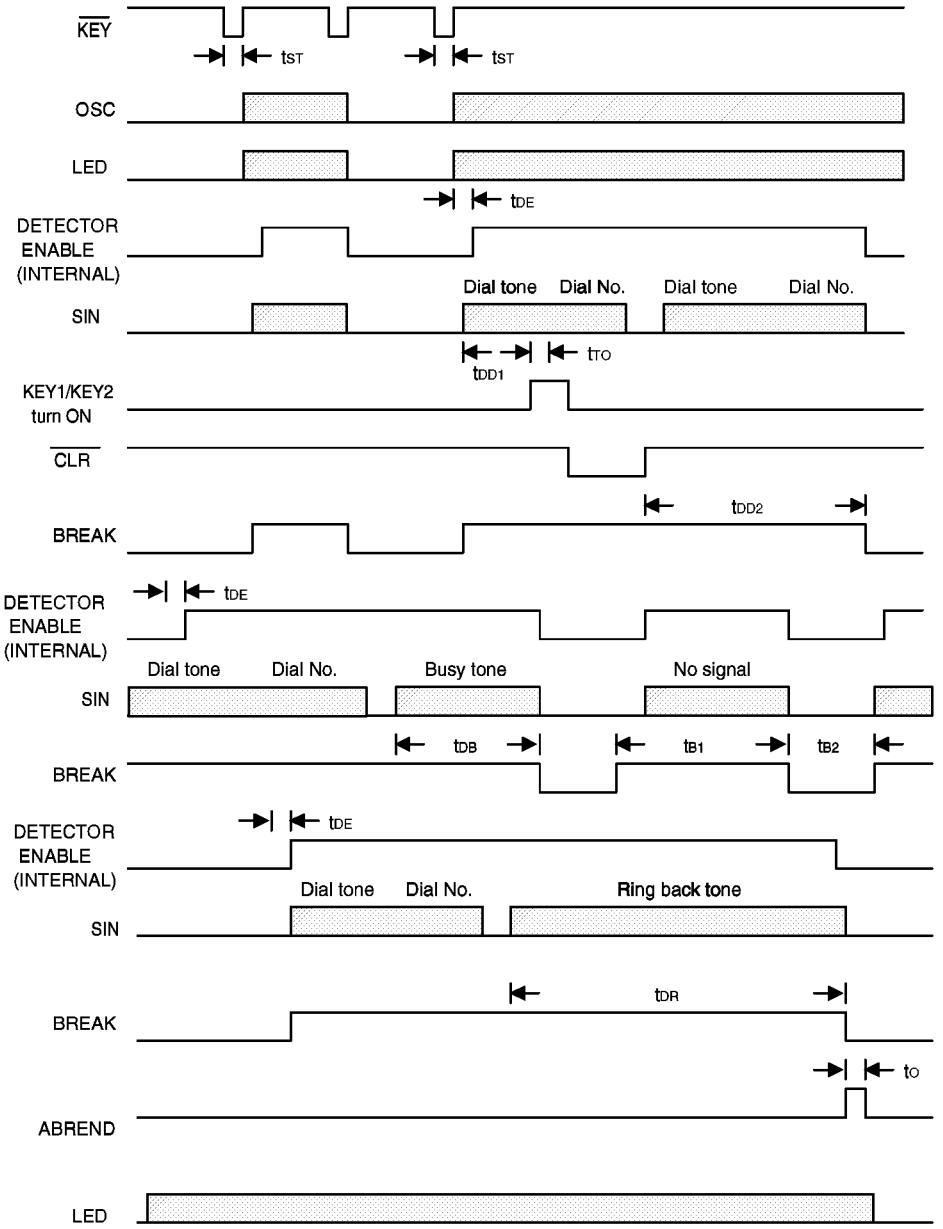
After the break timer has timed-out, the redial will be executed again. If the repeat-number ends, the OVER pin will output a 100ms high pulse to automatically reset to the initial state.

If the receiver does not answer within 30 cycles, a ringback tone is produced, and the OVER pin will output a 100ms high pulse to automatically reset to the initial state.

The break time and repeat number setting

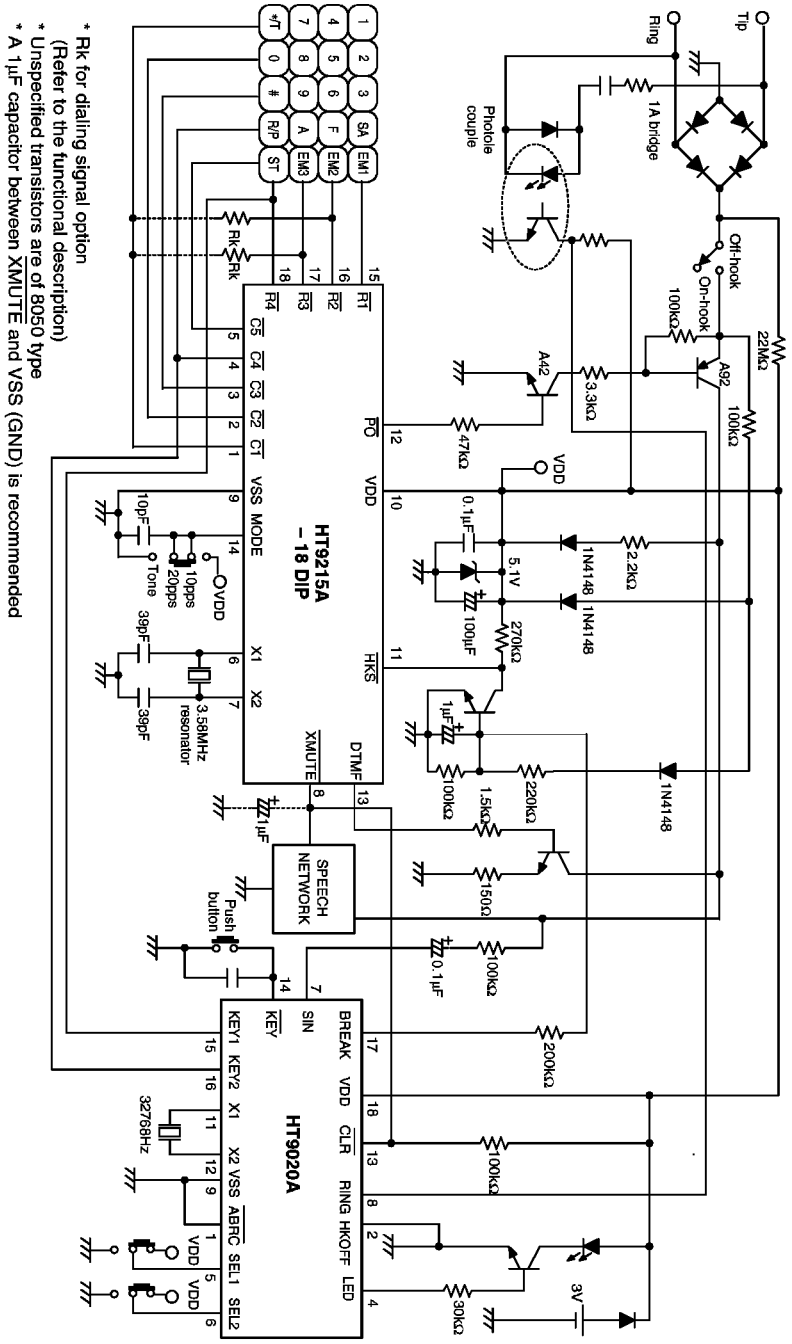
SEL1	SEL2	Repeat No. (times)	Break Time (seconds)	
			t_{B1}	t_{B2}
0	0	10	62.8	84.9
0	1	10	32.6	34.9
1	0	3	62.8	64.9
1	1	15	4.65	6.97

ABR controller timing diagrams



Application Circuits

Application Circuit 1



Application Circuit 2