HM64YLB36512 Series

16M Synchronous Late Write Fast Static RAM
(512-kword × 36-bit)

HITACHI

ADE-203-1336A (Z)

Preliminary
Rev. 0.1
Aug. 30, 2002

Description

The HM64YLB36512 is a synchronous fast static RAM organized as 512-kword × 36-bit. It has realized high speed access time by employing the most advanced CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in standard 119-bump BGA.

Note: All power supply and ground pins must be connected for proper operation of the device.

Features

- 2.5 V ± 5 % operation and 1.5 V (V_{DDQ})
- 16M bit density
- Synchronous register to register operation
- Mode selectable between late write and associative late write (late select)
- Late select mode: Late SAS select, selects which half of 72-bit core data to return on reads
- Late select mode: SAS serves as way select
- Byte write control (4 byte write selects, one for each 9-bit)
- Optional ×18 configuration
- HSTL compatible I/O
- Programmable impedance output drivers
- Differential HSTL clock inputs
- Asynchronous $\overline{\text{G}}$ output control
- Asynchronous sleep mode
- FC-BGA 119pin package with SRAM JEDEC standard pinout
- Limited set of boundary scan JTAG IEEE 1149.1 compatible

Ordering Information

Type No.	Organization	Access time	Cycle time	Package
HM64YLB36512BP-28	512k × 36	1.6 ns	2.8 ns	119-bump 1.27 mm 14 mm × 22 mm BGA (BP-119E)
HM64YLB36512BP-33	512k × 36	1.6 ns	3.3 ns	

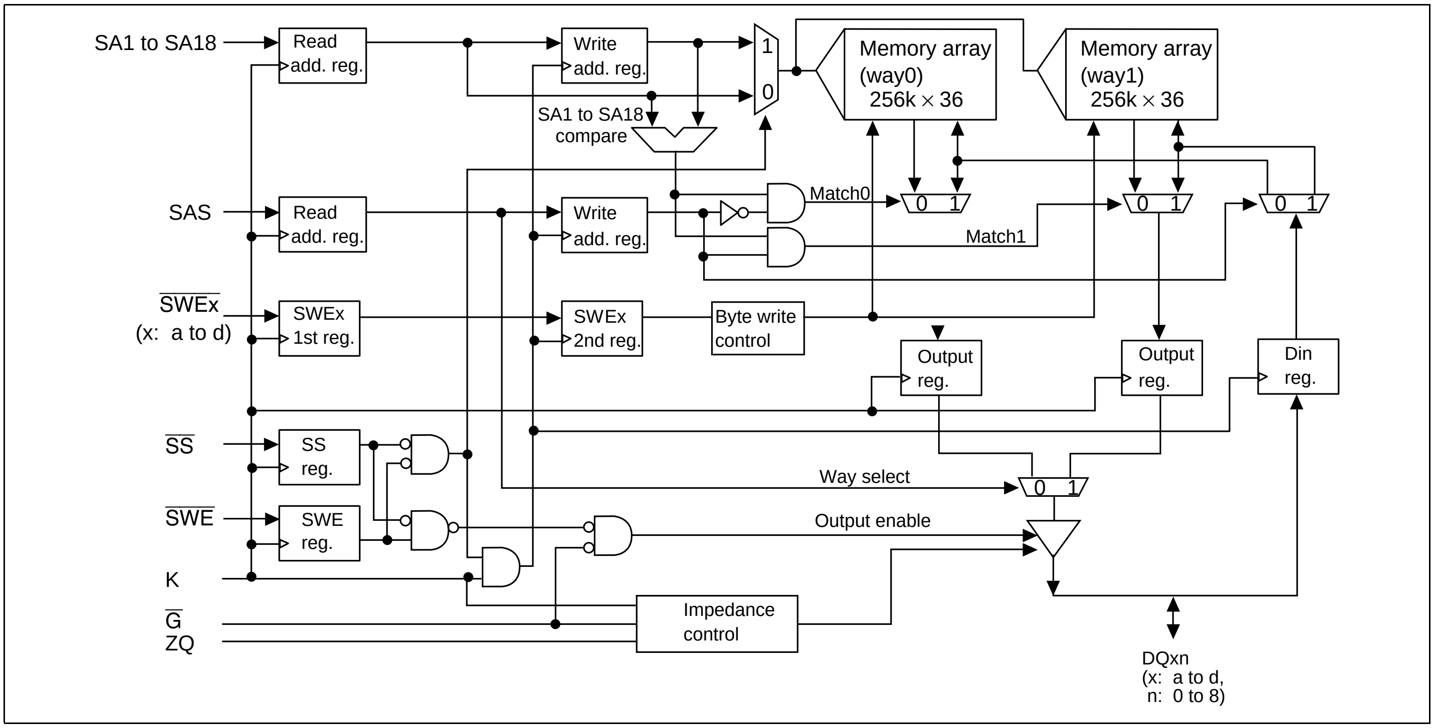
Notes HM: Hitachi Memory prefix, 64: External Cache SRAM, Y: V_{DD} = 2.5 V, L: Dual Mode SRAM, B: V_{DDQ} = 1.5 V

Pin Arrangement

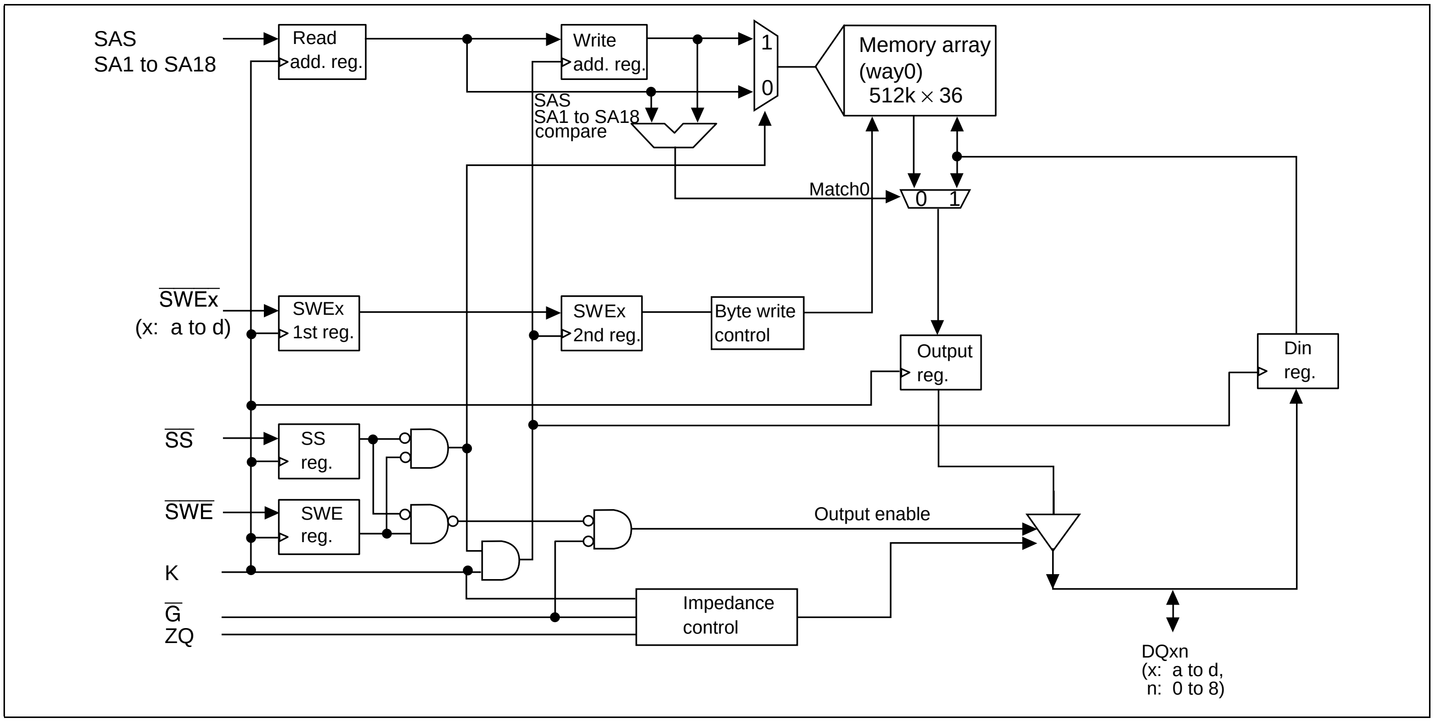
	1	2	3	4	5	6	7
A	V_{DDQ}	SA14	SA13	NC	SA6	SA7	V_{DDQ}
B	NC	SA15	SA12	NC	SA5	SA9	NC
C	NC	SA16	SA11	V_{DD}	SA4	SA8	NC
D	DQc7	DQc8	V_{SS}	ZQ	V_{SS}	DQb8	DQb7
E	DQc5	DQc6	V_{SS}	$\overline{SS}$	V_{SS}	DQb6	DQb5
F	V_{DDQ}	DQc4	V_{SS}	$\overline{G}$	V_{SS}	DQb4	V_{DDQ}
G	DQc3	DQc2	$\overline{SWEc}$	NC	$\overline{SWEb}$	DQb2	DQb3
H	DQc1	DQc0	V_{SS}	NC	V_{SS}	DQb0	DQb1
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd1	DQd0	V_{SS}	K	V_{SS}	DQa0	DQa1
L	DQd3	DQd2	$\overline{SWEd}$	$\overline{K}$	$\overline{SWEa}$	DQa2	DQa3
M	V_{DDQ}	DQd4	V_{SS}	$\overline{SWE}$	V_{SS}	DQa4	V_{DDQ}
N	DQd5	DQd6	V_{SS}	SA17	V_{SS}	DQa6	DQa5
P	DQd7	DQd8	V_{SS}	SAS	V_{SS}	DQa8	DQa7
R	NC	SA10	M1	V_{DD}	M2	SA1	NC
T	NC	NC	SA18	SA3	SA2	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

(Top view)

Block Diagram (Late Select Mode)



Block Diagram (Late Write Mode)



Pin Descriptions

Name	I/O type	Descriptions	Notes
V_{DD}	Supply	Core power supply	
V_{SS}	Supply	Ground	
V_{DDQ}	Supply	Output power supply	
V_{REF}	Supply	Input reference, provides input reference voltage	
K	Input	Clock input, active high	
$\overline{K}$	Input	Clock input, active low	
$\overline{SS}$	Input	Synchronous chip select	
$\overline{SWE}$	Input	Synchronous write enable	
SAn	Input	Synchronous address input	n: 1 to 18
SAS	Input	Late select: Synchronous way select Late write: Synchronous address input	
$\overline{SWEx}$	Input	Synchronous byte write enables	x: a to d
$\overline{G}$	Input	Asynchronous output enable	
ZZ	Input	Power down mode select	
ZQ	Input	Output impedance control	1
DQxn	I/O	Synchronous data input/output	x: a to d n: 0 to 8
M1, M2	Input	Output protocol mode select	
TMS	Input	Boundary scan test mode select	
TCK	Input	Boundary scan test clock	
TDI	Input	Boundary scan test data input	
TDO	Output	Boundary scan test data output	
NC	—	No connection	

M1	M2	Protocol	Notes
V_{SS}	V_{SS}	Synchronous register to register operation (late select mode)	2
V_{SS}	V_{DD}	Synchronous register to register operation (late write mode)	3

Notes: 1. ZQ is to be connected to V_{SS} via a resistance RQ where $175\ \Omega \le RQ \le 300\ \Omega$. If ZQ = V_{DDQ} or open, output buffer impedance will be maximum.

2. Mode control pins M1 and M2 are used to select different read protocols.

These mode control input pins are set at power-up and will not change the states during the SRAM operates.

Late select mode: Single clock, late SAS select, pipelined read protocol

Late write mode: Single clock, pipelined read protocol

3. Mode control pin M2 can be set to V_{DDQ} instead of V_{DD}.

Truth Table

ZZ	$\overline{\text{SS}}$	$\overline{\text{G}}$	$\overline{\text{SWE}}$	$\overline{\text{SWEa}}$	$\overline{\text{SWEb}}$	$\overline{\text{SWEc}}$	$\overline{\text{SWEd}}$	K	$\overline{\text{K}}$	Operation	DQ (n)	DQ (n+1)
H	×	×	×	×	×	×	×	×	×	Sleep mode	High-Z	High-Z
L	H	×	×	×	×	×	×	L-H	H-L	Dead (not selected)	×	High-Z
L	×	H	H	×	×	×	×	×	×	Dead (dummy read)	High-Z	×
L	L	L	H	×	×	×	×	L-H	H-L	Read	×	Dout (a, b, c, d) 0 to 8
L	L	×	L	L	L	L	L	L-H	H-L	Write a, b, c, d byte	High-Z	Din (a, b, c, d) 0 to 8
L	L	×	L	H	L	L	L	L-H	H-L	Write b, c, d byte	High-Z	Din (b, c, d) 0 to 8
L	L	×	L	L	H	L	L	L-H	H-L	Write a, c, d byte	High-Z	Din (a, c, d) 0 to 8
L	L	×	L	L	L	H	L	L-H	H-L	Write a, b, d byte	High-Z	Din (a, b, d) 0 to 8
L	L	×	L	L	L	L	H	L-H	H-L	Write a, b, c byte	High-Z	Din (a, b, c) 0 to 8
L	L	×	L	H	H	L	L	L-H	H-L	Write c, d byte	High-Z	Din (c, d) 0 to 8
L	L	×	L	L	H	H	L	L-H	H-L	Write a, d byte	High-Z	Din (a, d) 0 to 8
L	L	×	L	L	L	H	H	L-H	H-L	Write a, b byte	High-Z	Din (a, b) 0 to 8
L	L	×	L	H	L	L	H	L-H	H-L	Write b, c byte	High-Z	Din (b, c) 0 to 8
L	L	×	L	H	H	H	L	L-H	H-L	Write d byte	High-Z	Din (d) 0 to 8
L	L	×	L	H	H	L	H	L-H	H-L	Write c byte	High-Z	Din (c) 0 to 8
L	L	×	L	H	L	H	H	L-H	H-L	Write b byte	High-Z	Din (b) 0 to 8
L	L	×	L	L	H	H	H	L-H	H-L	Write a byte	High-Z	Din (a) 0 to 8

Notes: 1. H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

2. $\overline{\text{SWE}}$, $\overline{\text{SS}}$, $\overline{\text{SWEa}}$ to $\overline{\text{SWEd}}$, SA and SAS are sampled at the rising edge of K clock.

Programmable Impedance Output Drivers

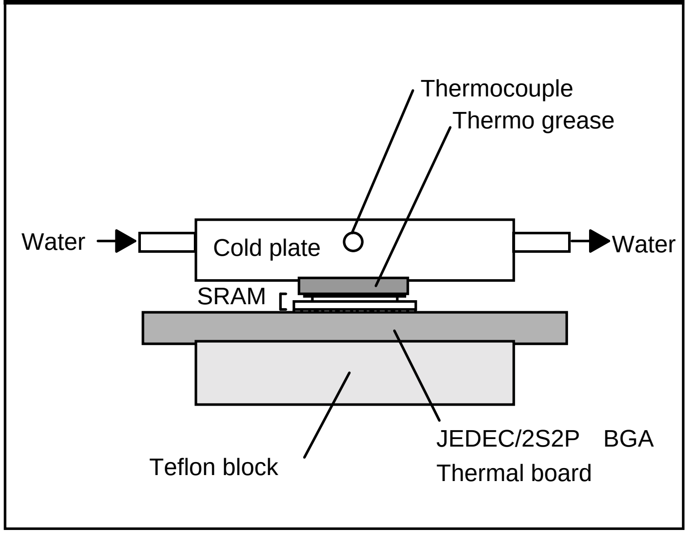
Output buffer impedance can be programmed by terminating the ZQ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is 250 Ω typical. If the status of ZQ pin is open, output impedance is maximum value. Maximum impedance also occurs with ZQ connected to V_{DDQ}. The impedance update of the output driver occurs when the SRAM is in high-Z. Write and deselect operations will synchronously switch the SRAM into and out of high-Z, therefore will trigger an update. The user may choose to invoke asynchronous $\overline{\text{G}}$ updates by providing a $\overline{\text{G}}$ setup and hold about the K clock, to guarantee the proper update. At power up, the output impedance defaults to minimum impedance. It will take 4096 cycles for the impedance to be completely updated if the programmed impedance is much higher than minimum impedance.

Absolute Maximum Ratings

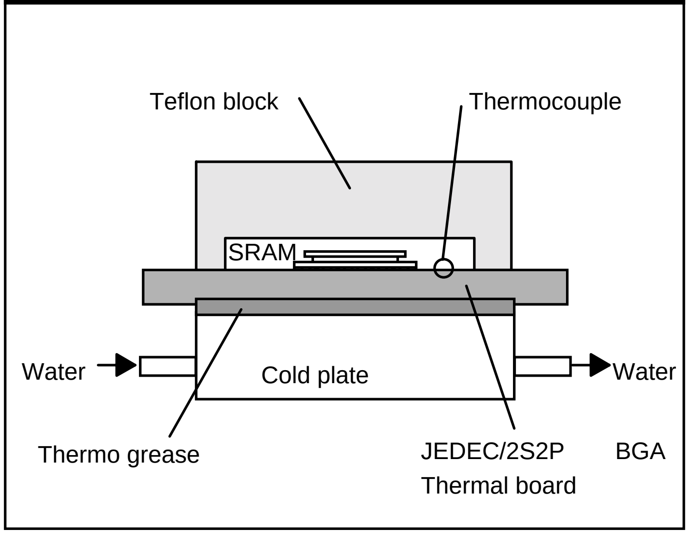
Parameter	Symbol	Rating	Unit	Notes
Input voltage on any pin	V_{IN}	–0.5 to V_{DDQ} + 0.5	V	1, 4
Core supply voltage	V_{DD}	–0.5 to +3.13	V	1
Output supply voltage	V_{DDQ}	–0.5 to +2.1	V	1, 4
Operating temperature	T_{OPR}	0 to +85	°C	
Storage temperature	T_{STG}	–55 to +125	°C	
Output short-circuit current	I_{OUT}	25	mA	
Latch up current	I_{LI}	200	mA	
Package junction to top thermal resistance	θJ-top	6.5	°C/W	5
Package junction to board thermal resistance	θJ-board	12	°C/W	5

Notes:
1. All voltage is referenced to V_{SS}.
2. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted the operation conditions. Exposure to higher voltages than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}.
   Remember, according to the absolute maximum ratings table, V_{DDQ} is not to exceed 2.1V, whatever the instantaneous value of V_{DDQ}.
5. See figure below.

θJ-top



θJ-board



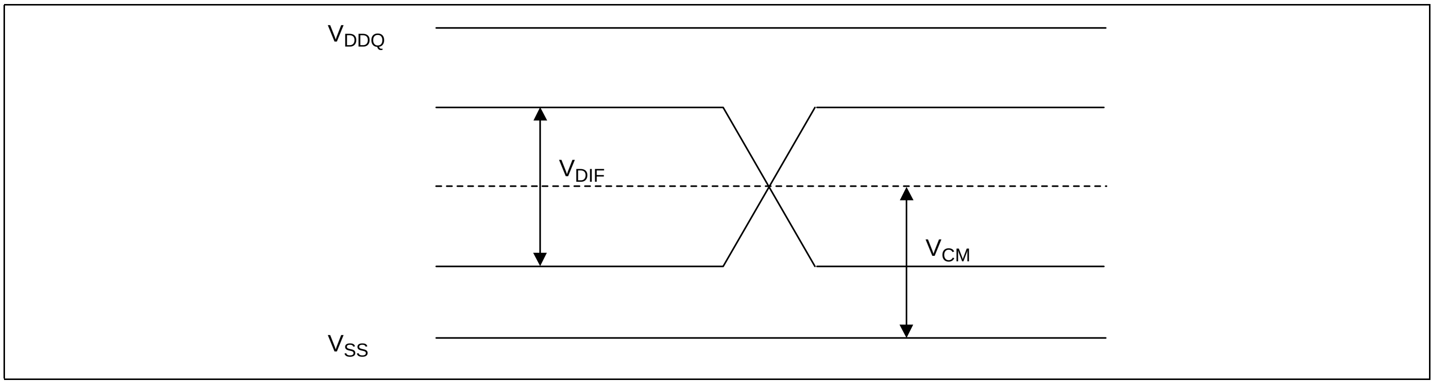
Note: The following the DC and AC specifications shown in the tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (Ta = 0 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage: Core	V_{DD}	2.38	2.50	2.63	V	
Power supply voltage: I/O	V_{DDQ}	1.40	1.50	1.60	V	
Input reference voltage: I/O	V_{REF}	0.60	0.75	0.90	V	1
Input high voltage	V_{IH}	V_{REF} + 0.10	—	V_{DDQ} + 0.30	V	4
Input low voltage	V_{IL}	–0.30	—	V_{REF} – 0.10	V	4
Clock differential voltage	V_{DIF}	0.10	—	V_{DDQ} + 0.30	V	2, 3
Clock common mode voltage	V_{CM}	0.60	—	0.90	V	3

Notes: 1. Peak to peak AC component superimposed on V_{REF} may not exceed 5 % of V_{REF}.
2. Minimum differential input voltage required for differential input clock operation.
3. See figure below.
4. V_{REF} = 0.75 V (typ).

Differential Voltage / Common Mode Voltage



DC Characteristics (Ta = 0 to +85°C, V_{DD} = 2.5 V ± 5 %)

Parameter	Symbol	Min	Max	Unit	Notes
Input leakage current	I_{LI}	—	2	µA	1
Output leakage current	I_{LO}	—	5	µA	2
Standby current	I_{SBZZ}	—	150	mA	3
V_{DD} operating current, excluding output drivers	I_{DD}	—	450	mA	4
Quiescent active power supply current	I_{DD2}	—	200	mA	5
Maximum power dissipation, including output drivers	P	—	2.3	W	6

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output low voltage	V_{OL}	V_{SS}	—	V_{SS} + 0.4	V	7
Output high voltage	V_{OH}	V_{DDQ} – 0.4	—	V_{DDQ}	V	8
ZQ pin connect resistance	RQ	—	250	—	Ω	
Output “Low” current	I_{OL}	(V_{DDQ}/2)/{(RQ/5) – 15 %}		(V_{DDQ}/2)/{(RQ/5) + 15 %}	mA	9, 11
Output “High” current	I_{OH}	(V_{DDQ}/2)/{(RQ/5) + 15 %}		(V_{DDQ}/2)/{(RQ/5) – 15 %}	mA	10, 11

Notes:
1. $0 \leq V_{IN} \leq V_{DDQ}$ for all input pins (except V_{REF}, ZQ, M1, M2 pin)
2. $0 \leq V_{OUT} \leq V_{DDQ}$, DQ in high-Z
3. All inputs (except clock) are held at either V_{IH} or V_{IL}, ZZ is held at V_{IH}, I_{OUT} = 0 mA. Specification is guaranteed at 75°C junction temperature.
4. I_{OUT} = 0 mA, read 50 % / write 50 %, V_{DD} = V_{DD} max, frequency = min. cycle
5. I_{OUT} = 0 mA, read 50 % / write 50 %, V_{DD} = V_{DD} max, frequency = 3 MHz
6. Output drives a 12pF load and switches every cycle. This parameter should be used by the SRAM designer to determine electrical and package requirements for the SRAM device.
7. RQ = 250 Ω, I_{OL} = 6.8 mA
8. RQ = 250 Ω, I_{OH} = –6.8 mA
9. Measured at V_{OL} = 1/2 V_{DDQ}
10. Measured at V_{OH} = 1/2 V_{DDQ}
11. The total external capacitance of ZQ pin must be less than 7.5 pF.

AC Characteristics (Ta = 0 to +85°C, V_{DD} = 2.5 V ± 5 %)

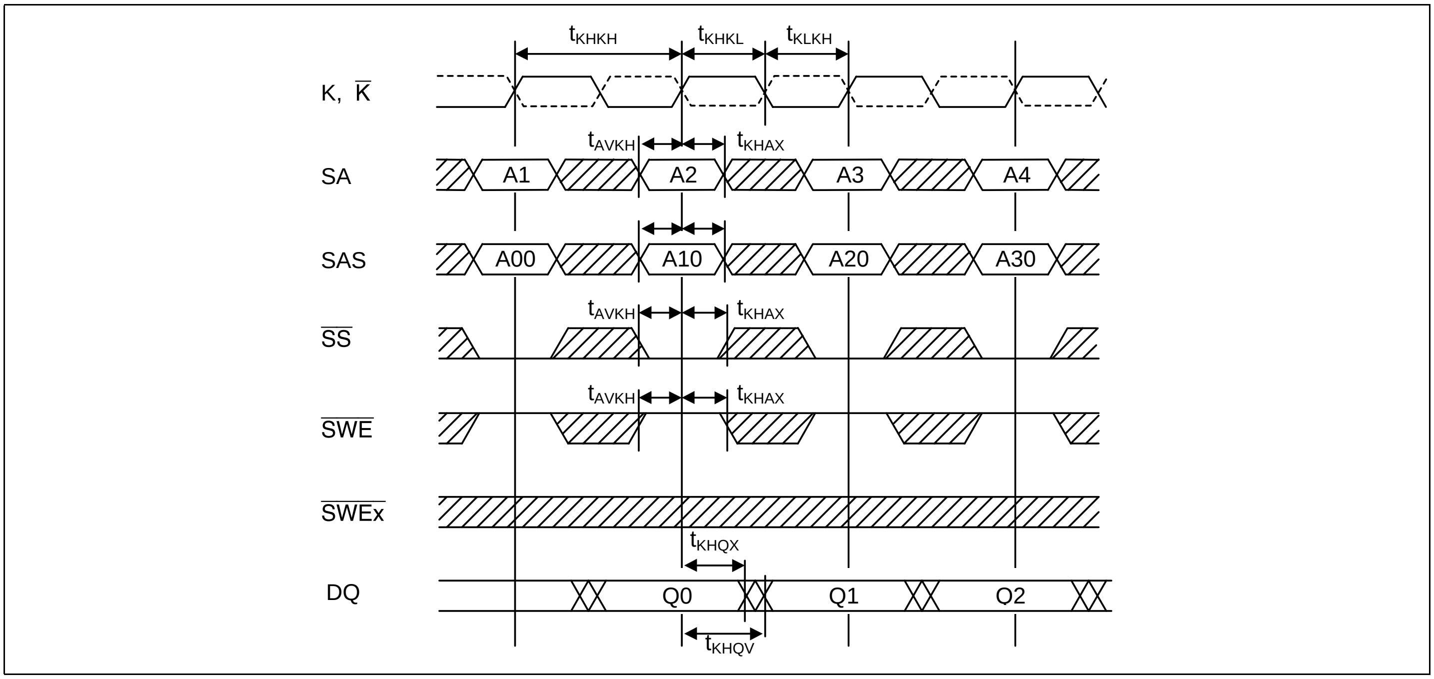
Single Differential Clock Register-Register Mode

		HM64YLB36512BP					
		-28		-33			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
CK clock cycle time	t_{KHKH}	2.8	—	3.3	—	ns	
CK clock high width	t_{KHKL}	1.2	—	1.3	—	ns	
CK clock low width	t_{KLKH}	1.2	—	1.3	—	ns	
Address setup time	t_{AVKH}	0.3	—	0.3	—	ns	2
Data setup time	t_{DVKH}	0.3	—	0.3	—	ns	2
Address hold time	t_{KHAX}	0.6	—	0.6	—	ns	
Data hold time	t_{KHDX}	0.6	—	0.6	—	ns	
Clock high to output valid	t_{KHQV}	—	1.6	—	1.6	ns	1
Clock high to output hold	t_{KHQX}	0.65	—	0.65	—	ns	1, 6
Clock high to output low-Z ($\overline{SS}$ control)	t_{KHQX2}	0.65	—	0.65	—	ns	1, 4, 6
Clock high to output high-Z	t_{KHQZ}	0.65	2.0	0.65	2.0	ns	1, 3, 6
Output enable low to output low-Z	t_{GLQX}	0.1	—	0.1	—	ns	1, 4, 6
Output enable low to output valid	t_{GLQV}	—	2.0	—	2.0	ns	1, 4
Output enable high to output high-Z	t_{GHQZ}	—	2.0	—	2.0	ns	1, 3
Sleep mode recovery time	t_{ZZR}	20.0	—	20.0	—	ns	5
Sleep mode enable time	t_{ZZE}	—	15.0	—	15.0	ns	1, 3, 5

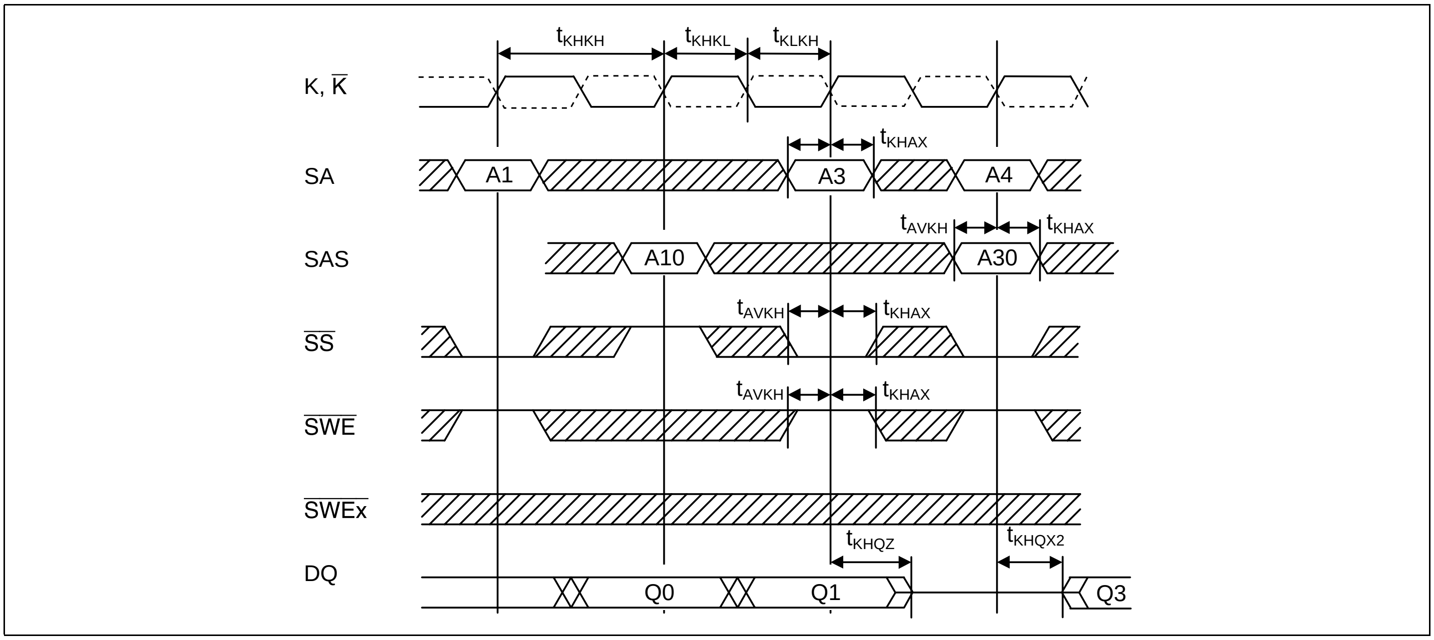
Notes:
1. See figure in ”AC Test Conditions”.
2. Parameters may be guaranteed by design, i.e., without tester guardband.
3. Transitions are measured ±50 mV of output high impedance from output low impedance.
4. Transitions are measured ±50 mV from steady state voltage.
5. When ZZ is switching, clock input K must be at the same logic level for the reliable operation.
6. Minimum value is verified by design and tested without guardband.

Late Select Mode

Read Cycle-1

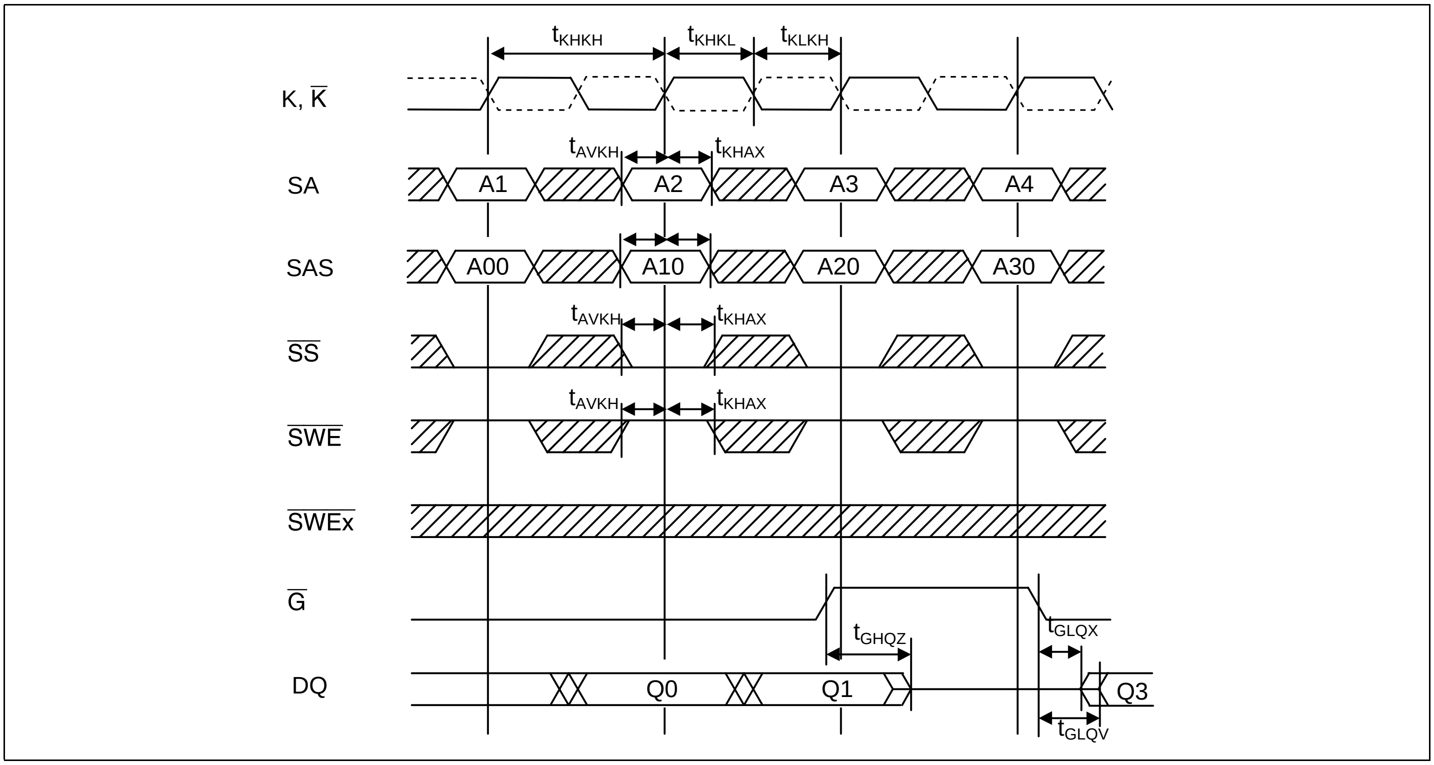


Read Cycle-2 ($\overline{SS}$ Controlled)



Notes: $\overline{G}$, ZZ = V_{IL}, x: a to d

Read Cycle-3 ($\overline{G}$ Controlled)

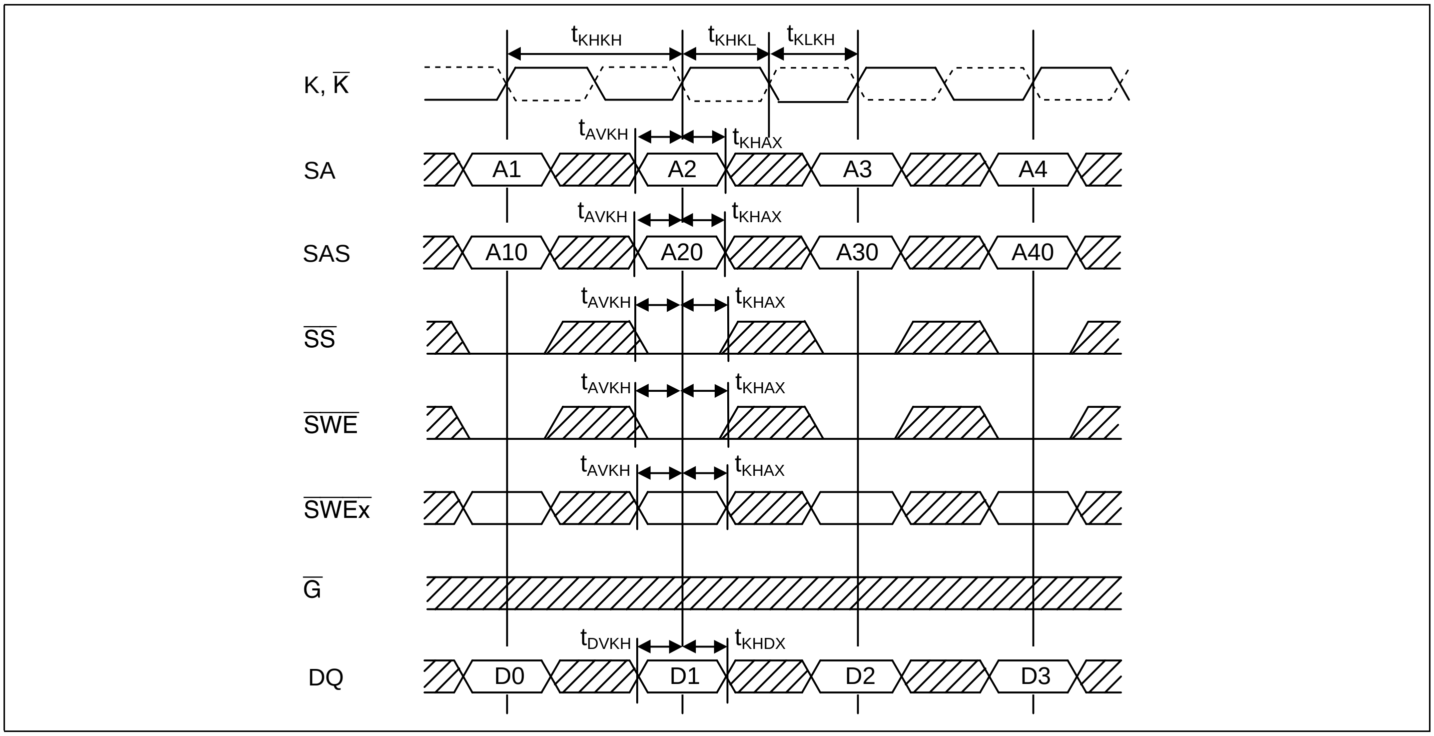


Read operation (late select mode)

During read cycle, N-1 bits of address (SA) are registered during the first rising clock edge. The Nth bit of address (SAS) is registered one clock edge later (the second edge). The setup time requirements for all address bits are the same. SAS is used as the Nth bit of address on both read and write.

The internal array is read between this first edge and second edge, and data is captured in the output register at the second clock edge. This requires the Nth address bit (SAS) to be used as a MUX select before the output register. Alternatively, the Nth address bit can be registered, and used as MUX select during the data drive cycle. In that case, the output drive should still have a monotonic edge transition (no glitches due to logic switch).

Write Cycle

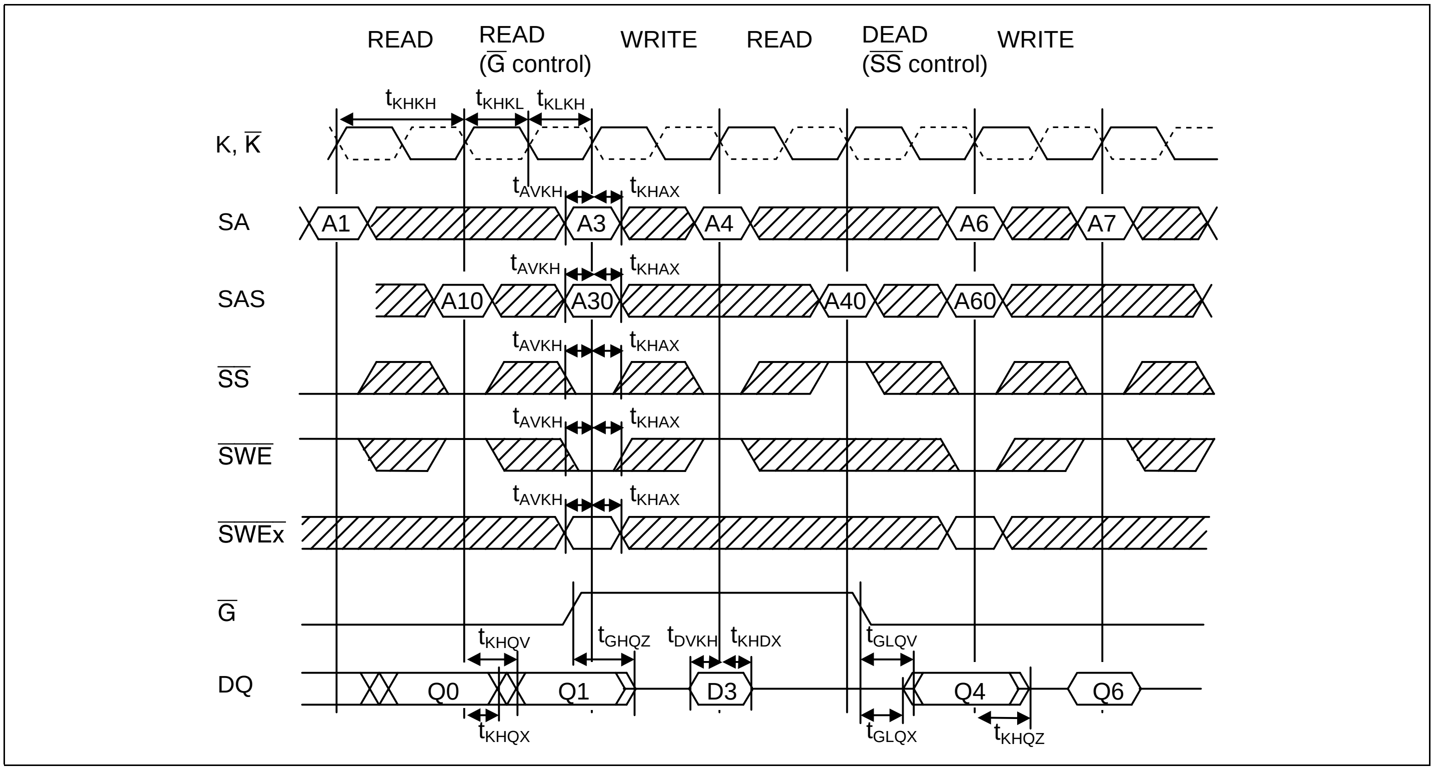


Notes: ZZ = V_{IL}, x: a to d

Write operation (late write and late select mode)

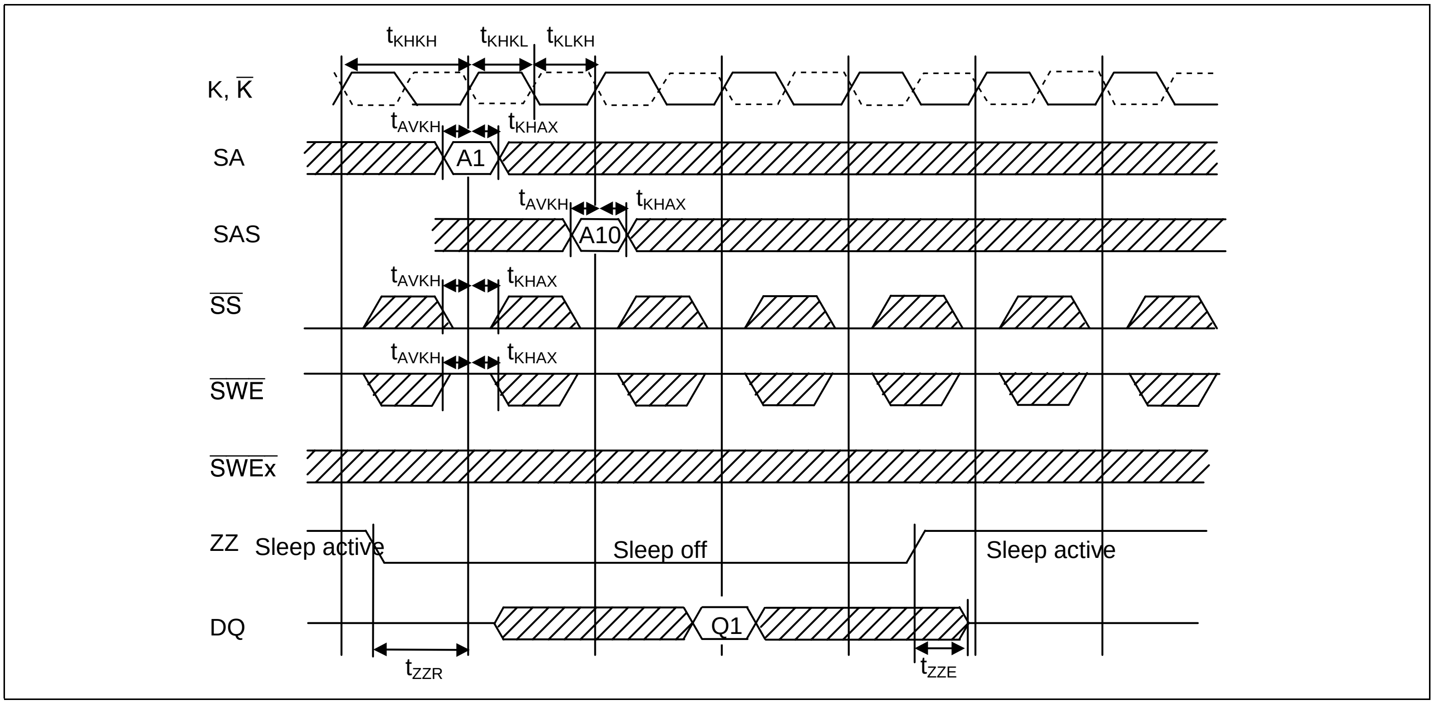
During writes, the write data follows the write address by one cycle. All N bits of address are presented during the same cycle. Any subsequent read to this address should get the latest data. Because in the actual implementation the data will be written into the SRAM array only after the next write address is received, a one-entry buffer is needed to hold the write data and to allow bypassing of data from the write buffer to the output if there is a read of the same address.

Read-Write Cycle



Notes: ZZ = V_{IL}, x: a to d

ZZ Control

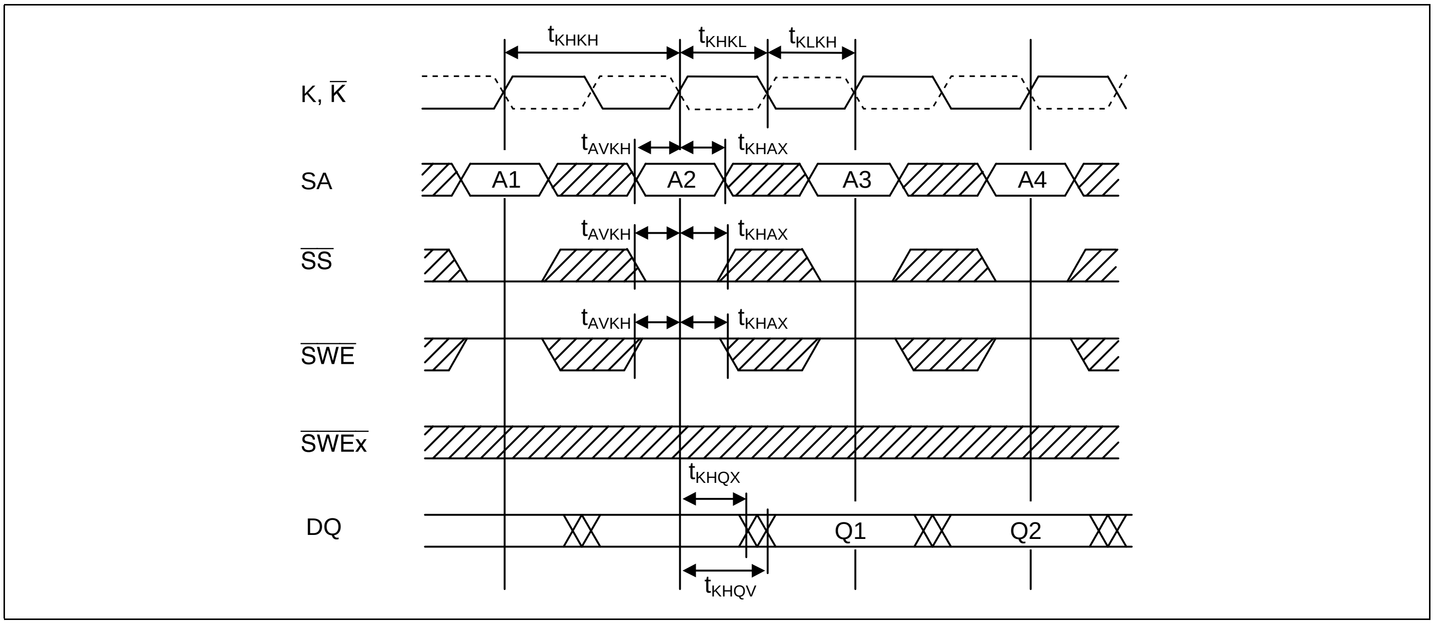


Notes: $\overline{G} = V_{IL}$, x: a to d

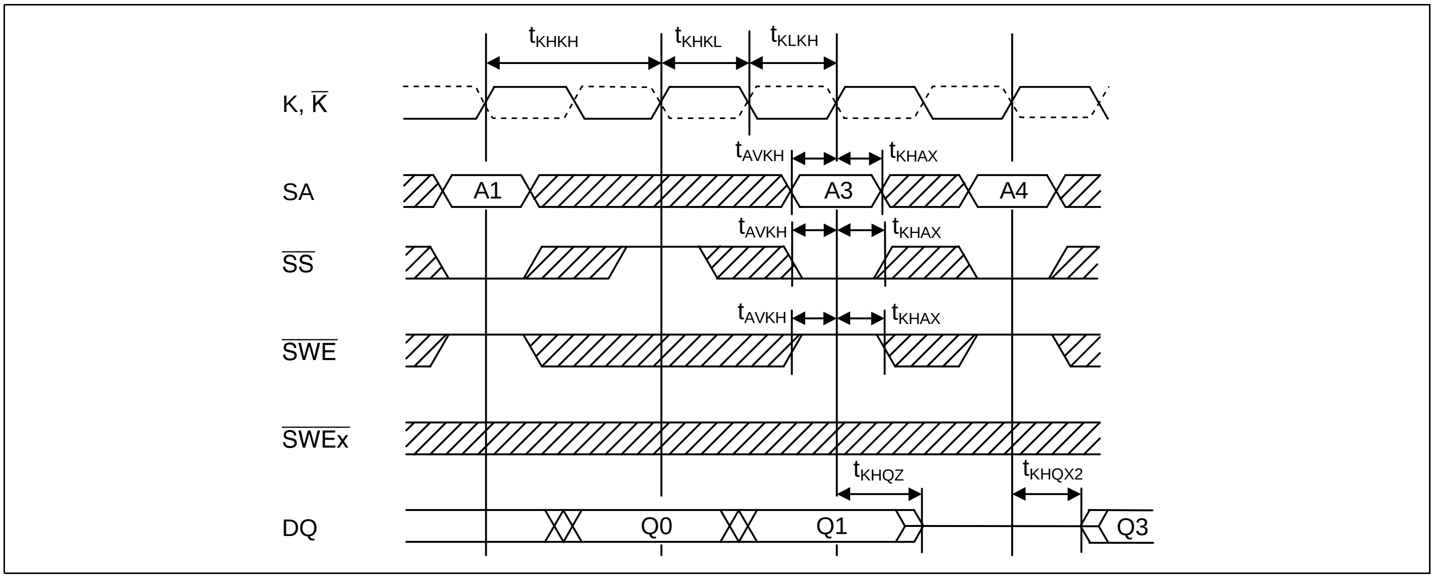
When ZZ is switching, clock input K must be at the same logic level for the reliable operation.

Late Write Mode

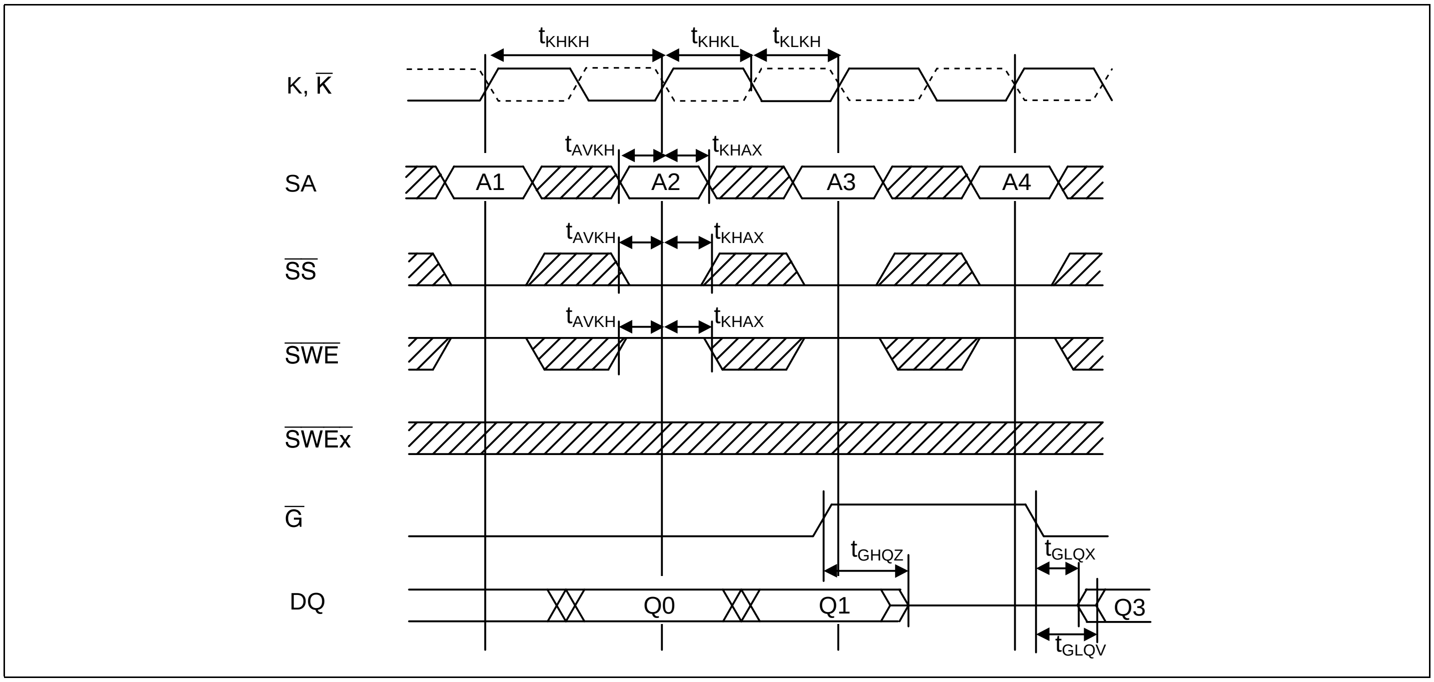
Read Cycle-1



Read Cycle-2 (SS̄ Control)



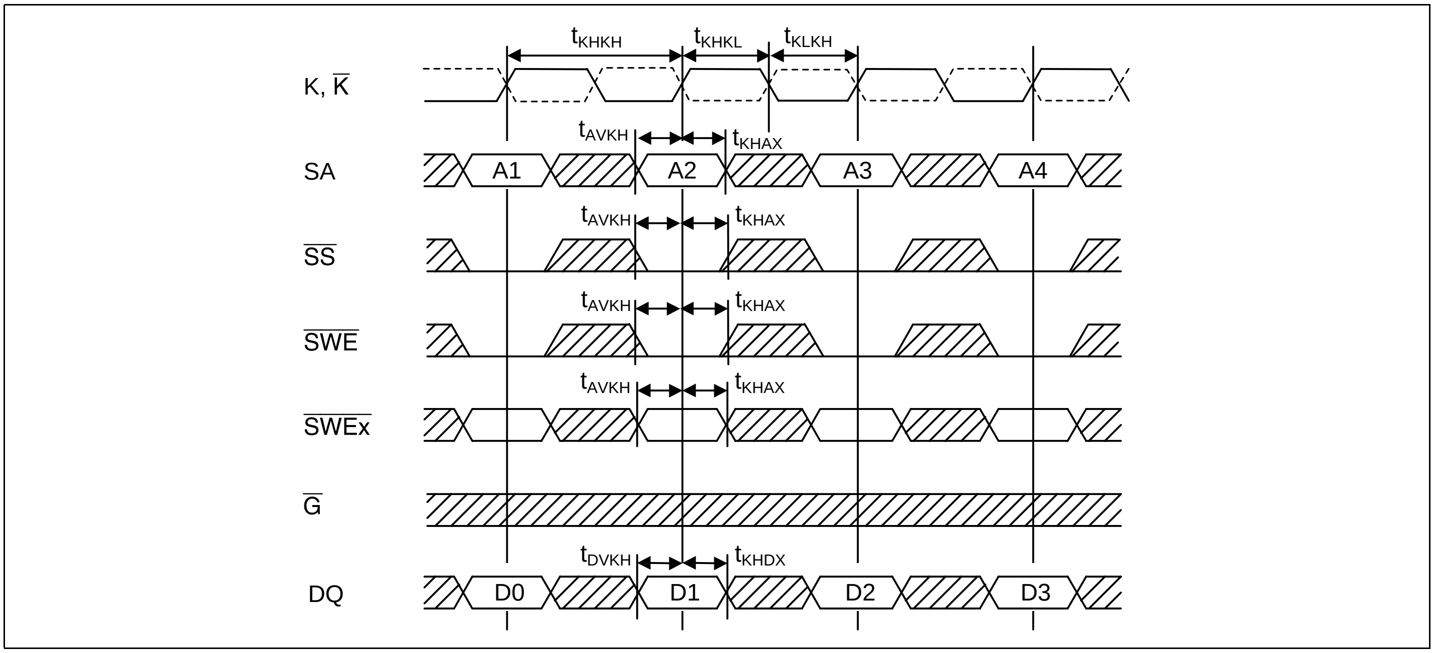
Read Cycle-3 ($\overline{G}$ Controlled)



Read operation (late write mode)

During read cycle, the address is registered during the first rising clock edge, the internal array is read between this first edge and second edge, and data is captured in the output register.

Write Cycle

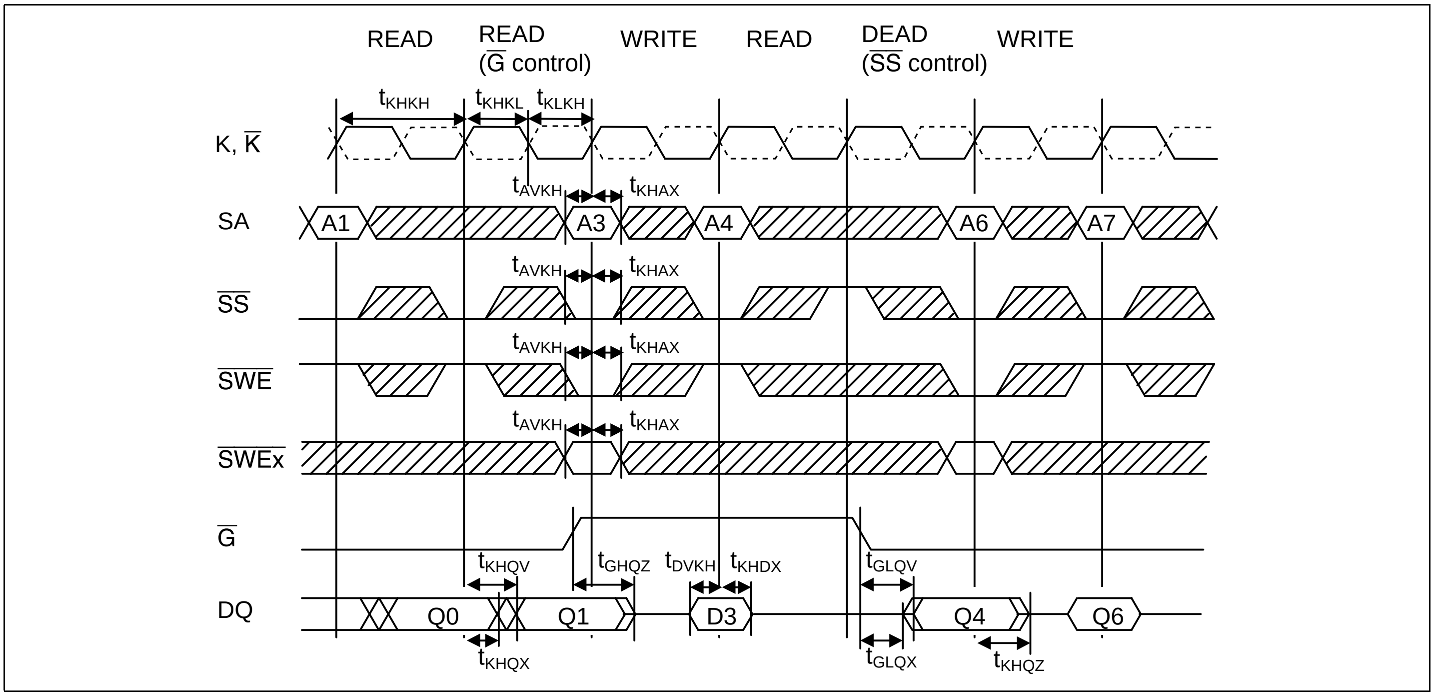


Notes: ZZ = V_{IL}, x: a to d

Write operation (late write and late select mode)

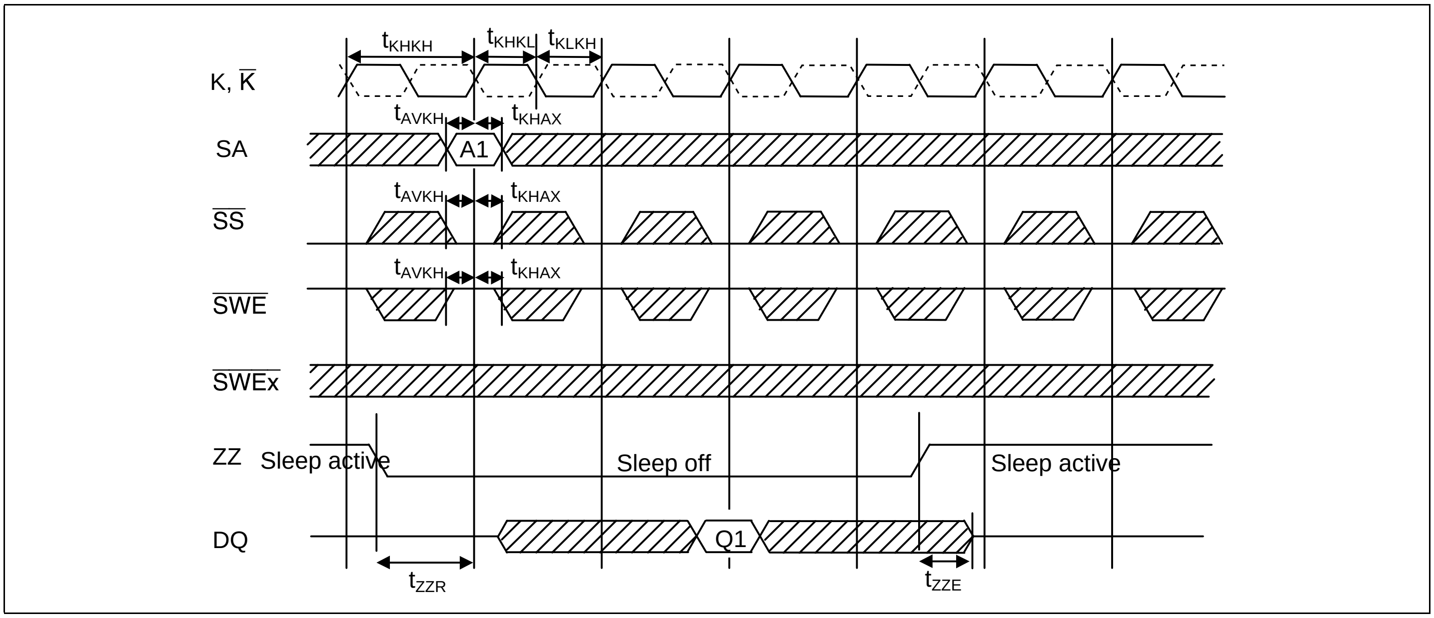
During write cycle, the write data follows the write address by one cycle. All N bits of address are presented during the same cycle. Any subsequent read to this address should get the latest data. Because in the actual implementation the data will be written into the SRAM array only after the next write address is received, a one-entry buffer is needed to hold the write data and to allow bypassing of data from the write buffer to the output if there is a read of the same address.

Read-Write Cycle



Notes: ZZ = V_{IL}, x: a to d

ZZ Control



Notes: $\overline{G}$ = V_{IL}, x: a to d

When ZZ is switching, clock input K must be at the same logic level for the reliable operation.

Input Capacitance (V_{DD} = 2.5 V, V_{DDQ} = 1.5 V, Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Pin name	Notes
Input capacitance	C_{IN}	—	4	pF	SAn, SAS, $\overline{SS}$, $\overline{SWE}$, $\overline{SWEx}$	1, 3
Clock input capacitance	C_{CLK}	—	5	pF	K, $\overline{K}$	1, 2, 3
I/O capacitance	C_{IO}	—	5	pF	DQxn	1, 3

Notes: 1. This parameter is sampled and not 100 % tested.

2. Exclude $\overline{G}$

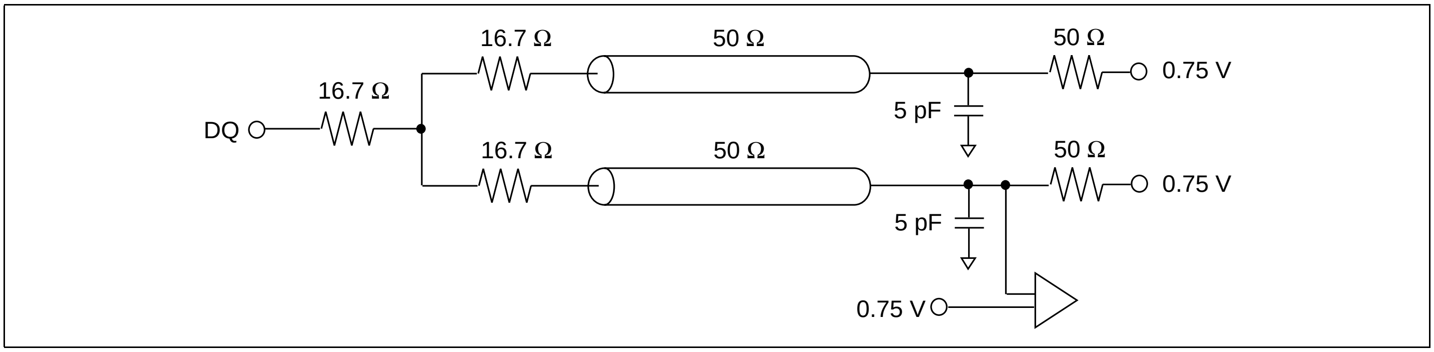
3. Connect pins to GND, except V_{DD}, V_{DDQ}, and the measured pin.

AC Test Conditions

Parameter	Symbol	Conditions	Unit	Note
Input and output timing reference levels	V_{REF}	0.75	V	
Input signal amplitude	V_{IL}, V_{IH}	0.25 to 1.25	V	
Input rise / fall time	tr, tf	0.5 (10 % to 90 %)	ns	
Clock input timing reference level		Differential cross point		
V_{DIF} to clock		0.75	V	
V_{CM} to clock		0.75	V	
Output loading conditions		See figure below		

Note: Parameters are tested with RQ = 250 Ω and V_{DDQ} = 1.5 V.

Output Loading Conditions



Boundary Scan Test Access Port Operations

Overview
In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1 compliance The HM64YLB series contains a TAP controller. Instruction register, Boundary scans register, Bypass register and ID register.

Test Access Port Pins

Symbol I/O	Name
TCK	Test clock
TMS	Test mode select
TDI	Test data in
TDO	Test data out

Notes: This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1.
To disable the TAP, TCK must be connected to V_{SS}. TDO should be left unconnected.
To test boundary scan, ZZ pin need to be kept below V_{REF} – 0.4 V.

TAP DC Operating Characteristics (Ta = 0 to +85°C)

Parameter	Symbol	Min	Max	Notes
Boundary scan input high voltage	V_{IH}	1.4 V	3.6 V	
Boundary scan input low voltage	V_{IL}	–0.3 V	0.8 V	
Boundary scan input leakage current	I_{LI}	–10 µA	+10 µA	1
Boundary scan output low voltage	V_{OL}	—	0.2 V	2
Boundary scan output high voltage	V_{OH}	2.1 V	—	3
Boundary scan output leakage current	I_{LO}	–5 µA	+5 µA	4

Notes:
1. $0 \le V_{IN} \le 3.6$ V for all logic input pin
2. I_{OL} = 2 mA at V_{DD} = 2.5 V.
3. I_{OH} = –2 mA at V_{DD} = 2.5 V.
4. $0 \le V_{OUT} \le V_{DD}$, TDO in high-Z

TAP AC Operating Characteristics (Ta = 0 to +85°C)

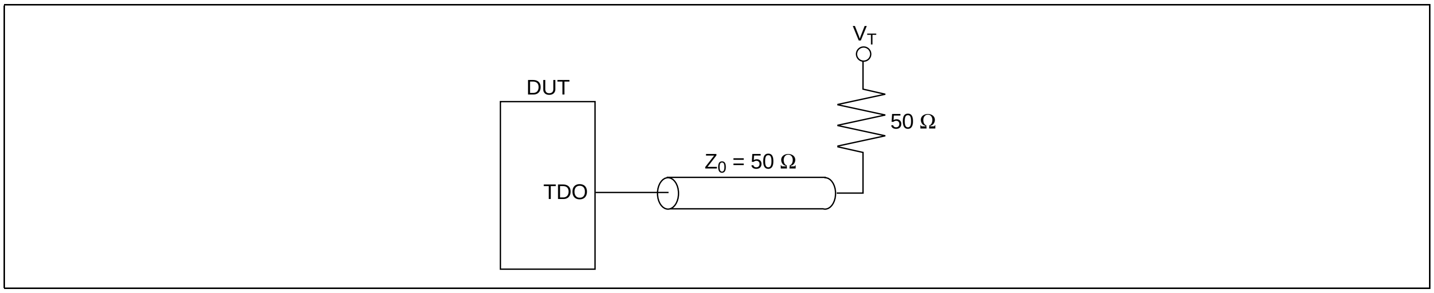
Parameter	Symbol	Min	Max	Unit	Note
Test clock cycle time	t_{THTH}	67	—	ns	
Test clock high pulse width	t_{THTL}	30	—	ns	
Test clock low pulse width	t_{TLTH}	30	—	ns	
Test mode select setup	t_{MVTH}	10	—	ns	
Test mode select hold	t_{THMX}	10	—	ns	
Capture setup	t_{CS}	10	—	ns	1
Capture hold	t_{CH}	10	—	ns	1
TDI valid to TCK high	t_{DVTH}	10	—	ns	
TCK high to TDI don’t care	t_{THDX}	10	—	ns	
TCK low to TDO unknown	t_{TLQX}	0	—	ns	
TCK low to TDO valid	t_{TLQV}	—	20	ns	

Note: 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

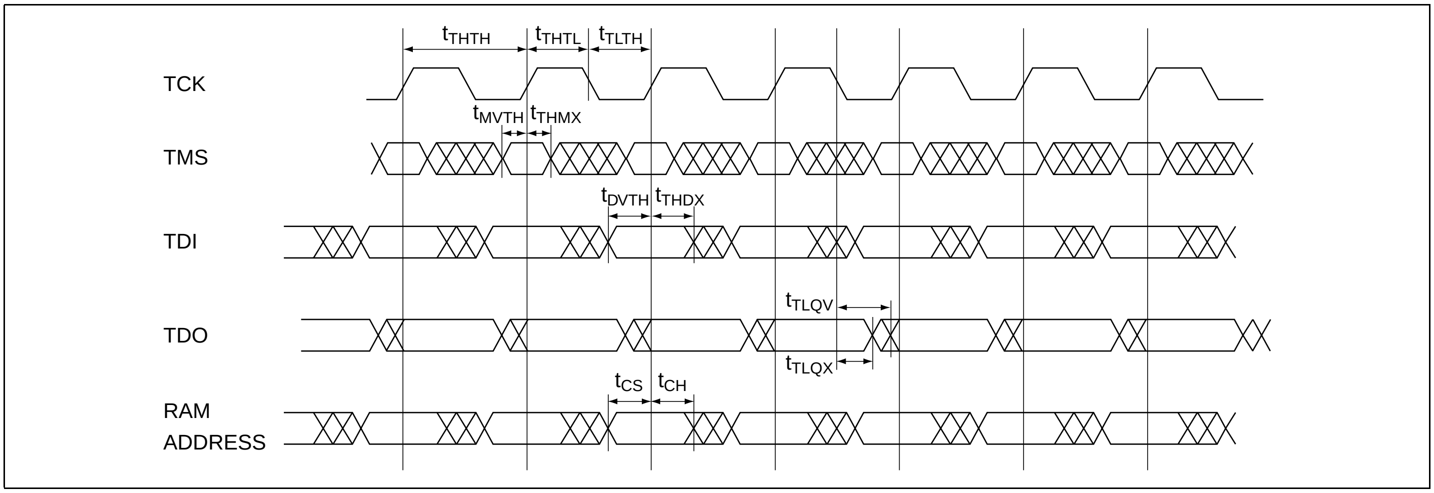
TAP AC Test Conditions (V_{DD} = 2.5 V)

• Temperature	0°C ≤ Ta ≤ +85°C
• Input timing measurement reference level	1.1 V
• Input pulse levels	0 to 2.5 V
• Input rise/fall time	1.5 ns typical (10 % to 90 %)
• Output timing measurement reference level	1.25 V
• Test load termination supply voltage (V_T)	1.25 V
• Output load	See figure below

Boundary Scan AC Test Load



TAP Controller Timing Diagram



Test Access Port Registers

Register Name	Length	Symbol	Note
Instruction register	3 bits	IR [2:0]	
Bypass register	1 bits	BP	
ID register	32 bits	ID [31:0]	
Boundary scan register	70 bits	BS [70:1]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	PRIVATE	Do not use. They are reserved for vendor use only
1	1	1	BYPASS	

Note: This device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

Boundary Scan Order (HM64YLB36512)

Bit #	Bump ID	Signal name
1	5R	M2
2	4P	SAS
3	4T	SA3
4	6R	SA1
5	5T	SA2
6	7T	ZZ
7	6P	DQa8
8	7P	DQa7
9	6N	DQa6
10	7N	DQa5
11	6M	DQa4
12	6L	DQa2
13	7L	DQa3
14	6K	DQa0
15	7K	DQa1
16	5L	$\overline{\text{SWEa}}$
17	4L	$\overline{\text{K}}$
18	4K	K
19	4F	$\overline{\text{G}}$
20	5G	$\overline{\text{SWEb}}$
21	7H	DQb1
22	6H	DQb0
23	7G	DQb3
24	6G	DQb2
25	6F	DQb4
26	7E	DQb5
27	6E	DQb6
28	7D	DQb7
29	6D	DQb8
30	6A	SA7
31	6C	SA8
32	5C	SA4
33	5A	SA6
34	6B	SA9
35	5B	SA5
36	3B	SA12
37	2B	SA15
38	3A	SA13
39	3C	SA11
40	2C	SA16
41	2A	SA14
42	2D	DQc8
43	1D	DQc7
44	2E	DQc6
45	1E	DQc5
46	2F	DQc4
47	2G	DQc2
48	1G	DQc3
49	2H	DQc0
50	1H	DQc1
51	3G	$\overline{\text{SWEc}}$
52	4D	ZQ
53	4E	$\overline{\text{SS}}$
54	4G	NC
55	4H	NC
56	4M	$\overline{\text{SWE}}$
57	3L	$\overline{\text{SWEd}}$
58	1K	DQd1
59	2K	DQd0
60	1L	DQd3
61	2L	DQd2
62	2M	DQd4
63	1N	DQd5
64	2N	DQd6
65	1P	DQd7
66	2P	DQd8
67	3T	SA18
68	2R	SA10
69	4N	SA17
70	3R	M1

Notes: 1. Bit#1 is the first scan bit to exit the chip.

2. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a “Place Holder”. Place holder registers are internally connected to V_{SS}.

3. In boundary scan mode, differential input K and $\overline{\text{K}}$ are referenced to each other and must be at the opposite logic levels for the reliable operation.

4. ZZ must remain V_{IL} during boundary scan.

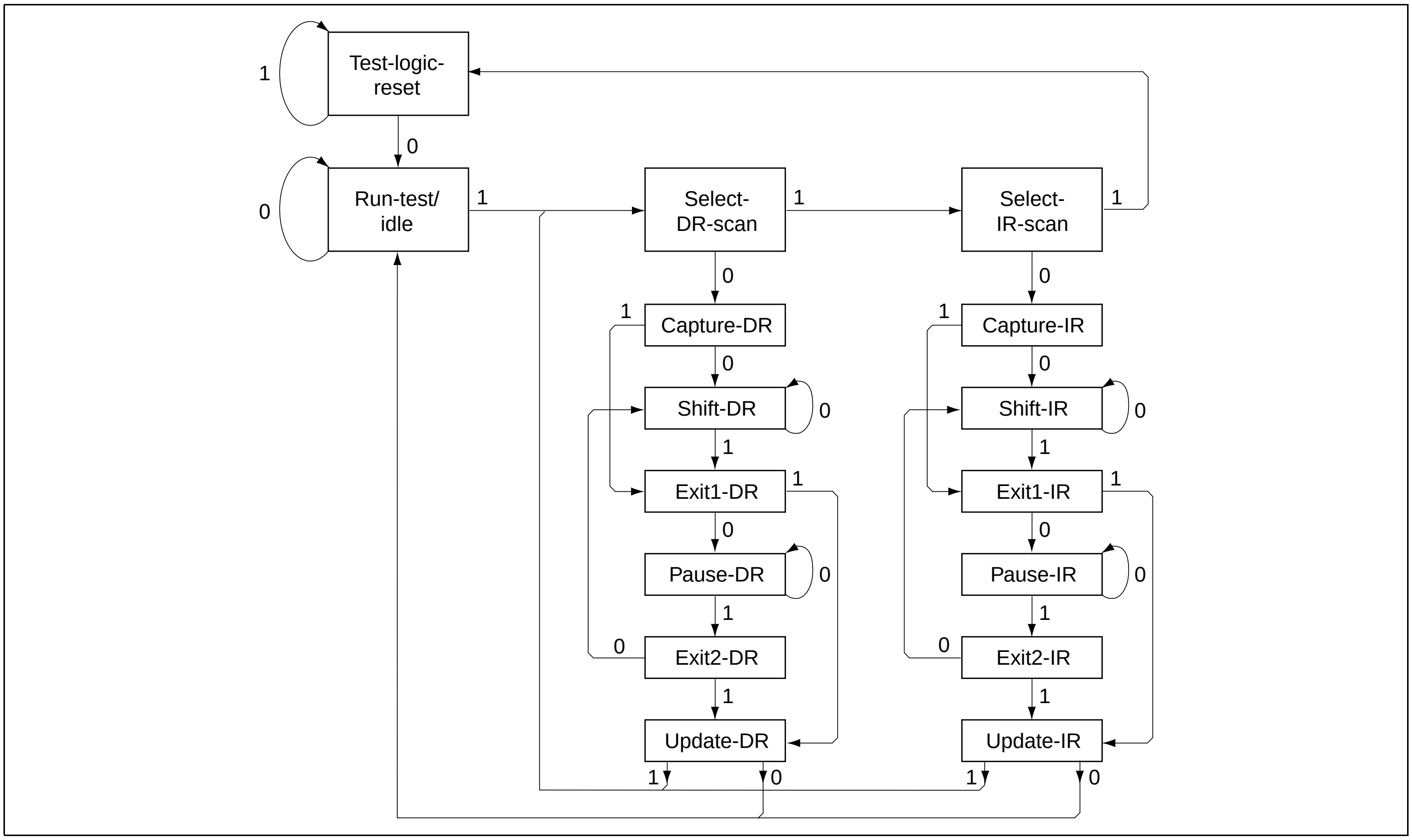
5. In boundary scan mode, ZQ must be driven to V_{DDQ} or V_{SS} supply rail to ensure consistent results.

6. M1 and M2 must be driven to V_{DD}, V_{DDQ} or V_{SS} supply rail to ensure consistent results.

ID Register

Part	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Vendor JEDEC Code (11:1)	Start Bit (0)
HM64YLB36512	0000	0011100100	xxxxxx	00000000111	1

TAP Controller State Diagram



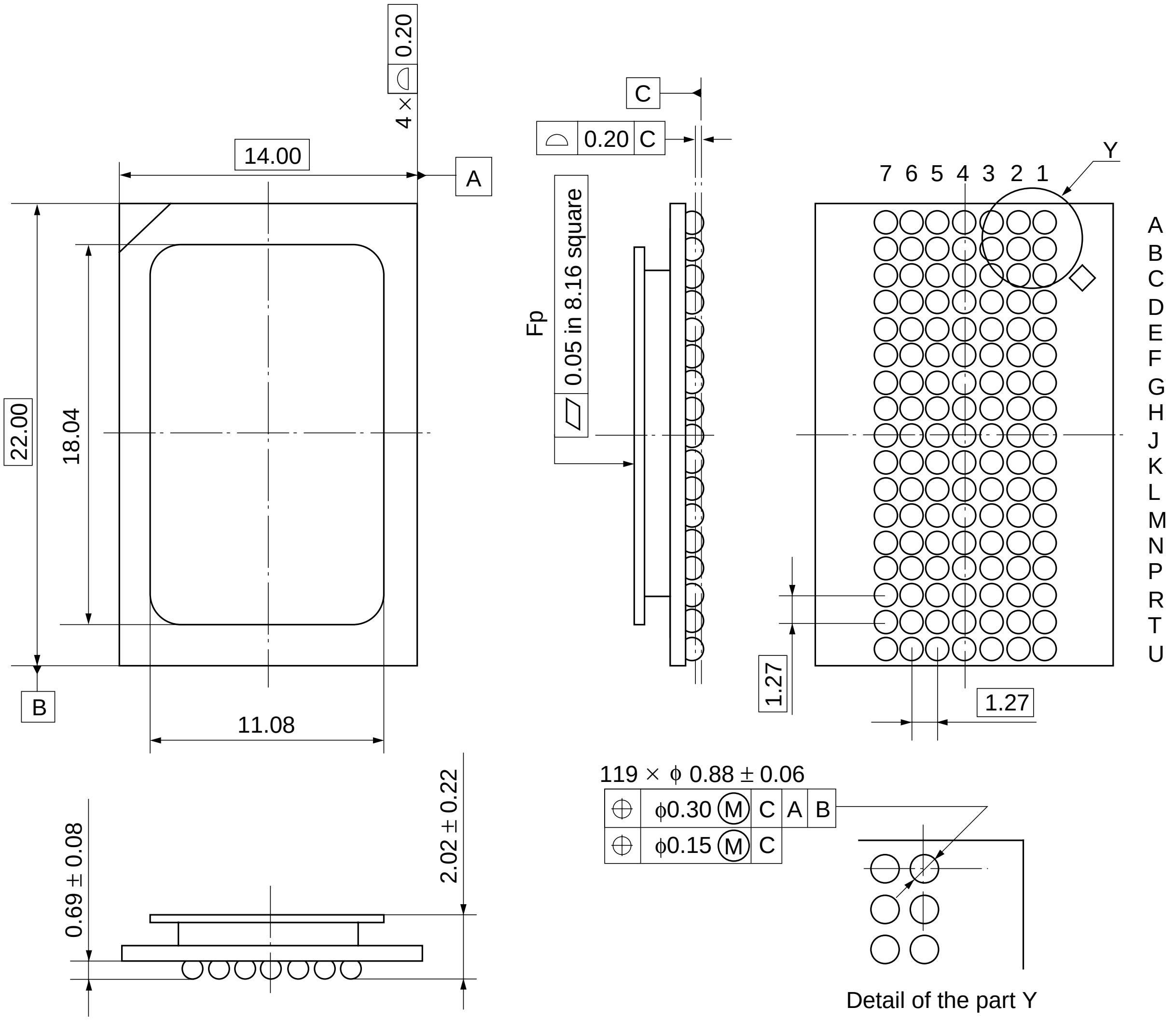
Notes: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

No matter what the original state of the controller, it will enter Test-logic-reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions

HM64YLB36512BP Series (BP-119E)

Unit: mm



Hitachi Code	BP-119E
JEDEC	TBD
JEITA	TBD
Mass (reference value)	TBD

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