

HM514400A Series

HM514400AL Series Low Power Version

HM514400ASL Series Super Low Power Version

Preliminary

T-46-23-18

1,048,576-Word x 4-Bit Dynamic Random Access Memory

DESCRIPTION

The Hitachi HM514400A is a CMOS dynamic RAM organized 1,048,576 word x 4-bit. HM514400A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400A to be packaged in standard 350 mil 20-pin plastic SOJ, standard 300 mil 20-pin plastic SOJ, standard 400 mil 20-pin plastic ZIP, 20-pin plastic TSOP I, 20-pin plastic TSOP I reverse type, 20-pin plastic TSOP II, and 20-pin plastic TSOP II reverse type.

FEATURES

- Single 5V (±10%)
- High Speed
 - Access Time 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
 - Active Mode 605 mW/550 mW/495 mW/440 mW (max)
 - Standby Mode 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles (16 ms, 128 ms, 256 ms)
- 3 Variations of Refresh
 - RAS Only Refresh
 - CAS Before RAS Refresh
 - Hidden Refresh
- Test Function
- Battery Backup Operation
 - HM514400AL Series (L-Version)
- Data Retention Operation
 - HM514400ASL Series (SL-Version)

ORDERING INFORMATION

Part No.	Access Time	Package
HM514400AJ/ALJ/ASLJ-6	60 ns	350 mil 20-pin Plastic SOJ (CP-20DA)
HM514400AJ/ALJ/ASLJ-7	70 ns	
HM514400AJ/ALJ/ASLJ-8	80 ns	
HM514400AJ/ALJ/ASLJ-10	100 ns	
HM514400AS/ALS/ASLS-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM514400AS/ALS/ASLS-7	70 ns	
HM514400AS/ALS/ASLS-8	80 ns	
HM514400AS/ALS/ASLS-10	100 ns	
HM514400AZ/ALZ/ASLZ-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM514400AZ/ALZ/ASLZ-7	70 ns	
HM514400AZ/ALZ/ASLZ-8	80 ns	
HM514400AZ/ALZ/ASLZ-10	100 ns	
HM514400AT/ALT/ASLT-6	60 ns	20-pin Plastic TSOP I (TFP-20DA)
HM514400AT/ALT/ASLT-7	70 ns	
HM514400AT/ALT/ASLT-8	80 ns	
HM514400AT/ALT/ASLT-10	100 ns	
HM514400AR/ALR/ASLR-6	60 ns	20-pin Plastic TSOP I Reverse Type (TFP-20DAR)
HM514400AR/ALR/ASLR-7	70 ns	
HM514400AR/ALR/ASLR-8	80 ns	
HM514400AR/ALR/ASLR-10	100 ns	
HM514400ATT/ALTT/ASLTT-6	60 ns	20-pin Plastic TSOP II (TTP-20D)
HM514400ATT/ALTT/ASLTT-7	70 ns	
HM514400ATT/ALTT/ASLTT-8	80 ns	
HM514400ATT/ALTT/ASLTT-10	100 ns	
HM514400ARR/ALRR/ASLRR-6	60 ns	20-pin Plastic TSOP II Reverse Type (TTP-20DR)
HM514400ARR/ALRR/ASLRR-7	70 ns	
HM514400ARR/ALRR/ASLRR-8	80 ns	
HM514400ARR/ALRR/ASLRR-10	100 ns	

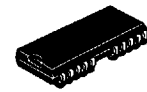
HM514400AJ/ALJ/ALSJ Series



(CP-20DA)

3DCP20DA

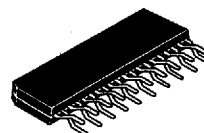
HM514400AS/ALS/ASLS Series



(CP-20D)

3DCP20D

HM514400AZ/ALZ/ASLZ Series



(ZP-20)

3DZP20

HM514400AT/ALT/ASLT Series



(TFP-20DA)

3DTFP20DA

HM514400AR/ALR/ASLR Series



(TFP-20DAR)

3DTFP20DAR

HM514400ATT/ALTT/ASLTT Series



(TTP-20D)

3DTTP20D

HM514400ARR/ALRR/ASLRR Series

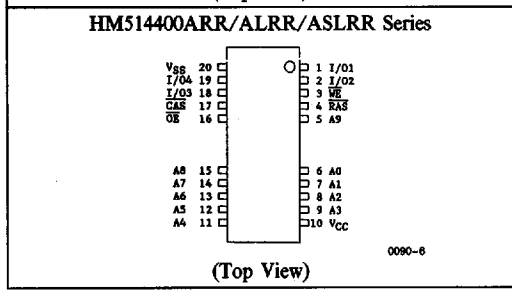
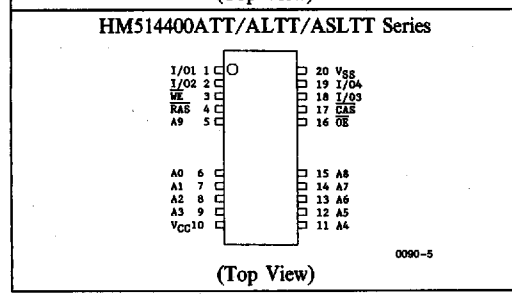
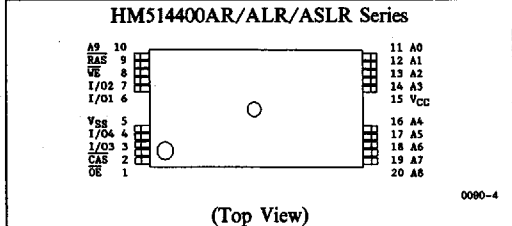
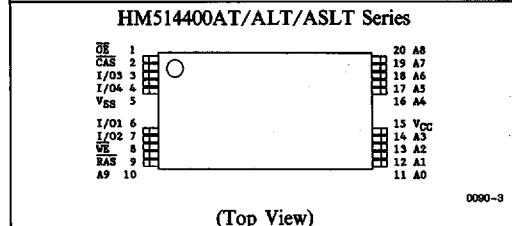
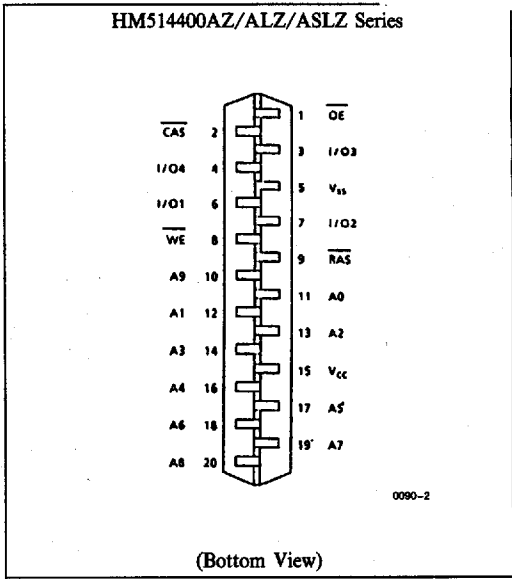
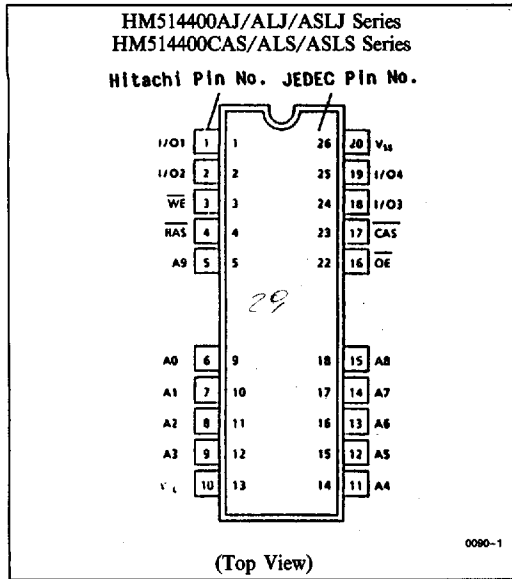


(TTP-20DR)

3DTTP20DR



■ PIN OUT



■ PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₉	Address Input
A ₀ -A ₉	Refresh Address Input
I/O ₁ -I/O ₄	Data-in/Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read/Write Enable
OE	Output Enable
V _{CC}	Power (+ 5V)
V _{SS}	Ground



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■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-1.0 to +7.0	V
Supply Voltage Relative to V _{SS}	V _{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I _{out}	50	mA
Power Dissipation	P _T	1.0	W
Operating Temperature	T _{opr}	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

- Recommended DC Operating Conditions (T_A = 0 to +70°C)
(T_A = 0 to +60°C (SL-Version))

Parameter	Symbol	Min	Typ	Max	Unit	Note	
Supply Voltage	V _{SS}	0	0	0	V		
	V _{CC}	4.5	5.0	5.5	V	1	
		4.0	—	5.5	V	1, 2 (SL-Version)	
Input High Voltage	V _{IH}	2.4	—	6.5	V	1	
Input Low Voltage	(I/O Pin)	V _{IL}	-1.0	—	0.8	V	1
	(Others)	V _{IL}	-2.0	—	0.8	V	1

- Notes: 1. All voltage referenced to V_{SS}.
2. Data retention operation only.

- DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version))

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	110	—	100	—	90	—	80	mA	RAS, CAS Cycling t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface RAS, CAS = V _{IH} , D _{out} = High-Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface RAS, RAS, CAS ≥ V _{CC} - 0.2V, D _{out} = High-Z	
[L-Version] Standby Current	I _{CC2}	—	200	—	200	—	200	—	200	μA	CMOS Interface RAS, CAS = V _{IH} , WE, OE, Address and D _{in} = V _{IH} or V _{IL} , D _{out} = High-Z	4
[SL-Version] Standby Current		—	100	—	100	—	100	—	100	μA	CMOS Interface RAS, CAS = V _{IH} , WE, OE, Address and D _{in} = V _{IH} or V _{IL} , D _{out} = High-Z	4
RAS Only Refresh Current	I _{CC3}	—	110	—	100	—	90	—	80	mA	t _{RC} = Min	2



• DC Electrical Characteristics (continued) ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

($T_A = 0$ to $+60^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$ (SL-Version))

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Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$, $\text{CAS} = V_{IL}$, $D_{out} = \text{Enable}$	1
CAS Before RAS Refresh Current	I_{CC6}	—	110	—	100	—	90	—	80	mA	$t_{RC} = \text{Min}$	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	—	80	mA	$t_{PC} = \text{Min}$	1, 3
[L-Version] Battery Backup Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	—	300	—	300	μA	$t_{RC} = 125 \mu\text{s}$, $t_{RAS} \leq 1 \mu\text{s}$, $\overline{\text{WE}} = V_{IH}$, $\text{CAS} = V_{IL}$, $\overline{\text{OE}}$, Address and $D_{in} = V_{IH}$ or V_{IL} , $D_{out} = \text{High-Z}$	4
[SL-Version] Data Retention Current (Equivalent Refresh Time is 256 ms)	I_{CC10}	—	150	—	150	—	150	—	150	μA	$t_{RC} = 250 \mu\text{s}$, $t_{RAS} \leq 200 \text{ ns}$, $\overline{\text{WE}} = V_{IH}$, $\text{CAS} = V_{IL}$, $\overline{\text{OE}}$, Address and $D_{in} = V_{IH}$ or V_{IL} , $D_{out} = \text{High-Z}$, $4.0\text{V} \leq V_{CC} \leq 5.5\text{V}$	4
Input Leakage Current	I_{LI}	-10	10	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{in} \leq 7\text{V}$	
Output Leakage Current	I_{LO}	-10	10	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{out} \leq 7\text{V}$, $D_{out} = \text{Disable}$	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High $I_{out} = -5 \text{ mA}$	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low $I_{out} = 4.2 \text{ mA}$	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\text{CAS} = V_{IH}$.
 4. $V_{CC} - 0.2\text{V} \leq V_{IH} \leq 6.5\text{V}$ and $0\text{V} \leq V_{IL} \leq 0.2\text{V}$.

• Capacitance ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

- Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\text{CAS} = V_{IH}$ to disable D_{out} .



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• AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) 1, 14, 15, 16

($T_A = 0$ to 60°C , $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (SL-Version))

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
RAS Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
RAS Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
CAS Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
RAS to CAS Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
RAS to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
RAS Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
CAS Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
OE to D _{in} Delay Time	t_{ODD}	15	—	20	—	20	—	25	—	ns	
OE Delay Time from D _{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	
CAS Setup Time from D _{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	
Refresh Period (L-Version)	t_{REF}	—	128	—	128	—	128	—	128	ms	
Refresh Period (SL-Version)	t_{REF}	—	16	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5, 13, 17
Access Time from OE	t_{OAC}	—	15	—	20	—	20	—	25	ns	3, 17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	18
Read Command Hold Time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	18
Column Address to RAS Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	20	0	20	0	25	ns	6
Output Buffer Turn-off to OE	t_{OFF2}	0	15	0	20	0	20	0	25	ns	6
CAS to D _{in} Delay Time	t_{CDD}	15	—	20	—	20	—	25	—	ns	



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Write Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t _{RWC}	150	—	180	—	200	—	245	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	80	—	95	—	105	—	135	—	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	t _{OEH}	15	—	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)	t _{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)	t _{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time in Normal Mode	t _{CPN}	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	t _{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	—	35	—	40	—	45	—	50	ns	3, 13, 17
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPW}	55	—	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t _{PCM}	80	—	95	—	100	—	110	—	ns	



Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode \overline{WE} Setup time	t _{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode \overline{WE} Hold Time	t _{WH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS Precharge Time in Counter Test Cycle	t _{CPT}	40	—	40	—	40	—	50	—	ns	

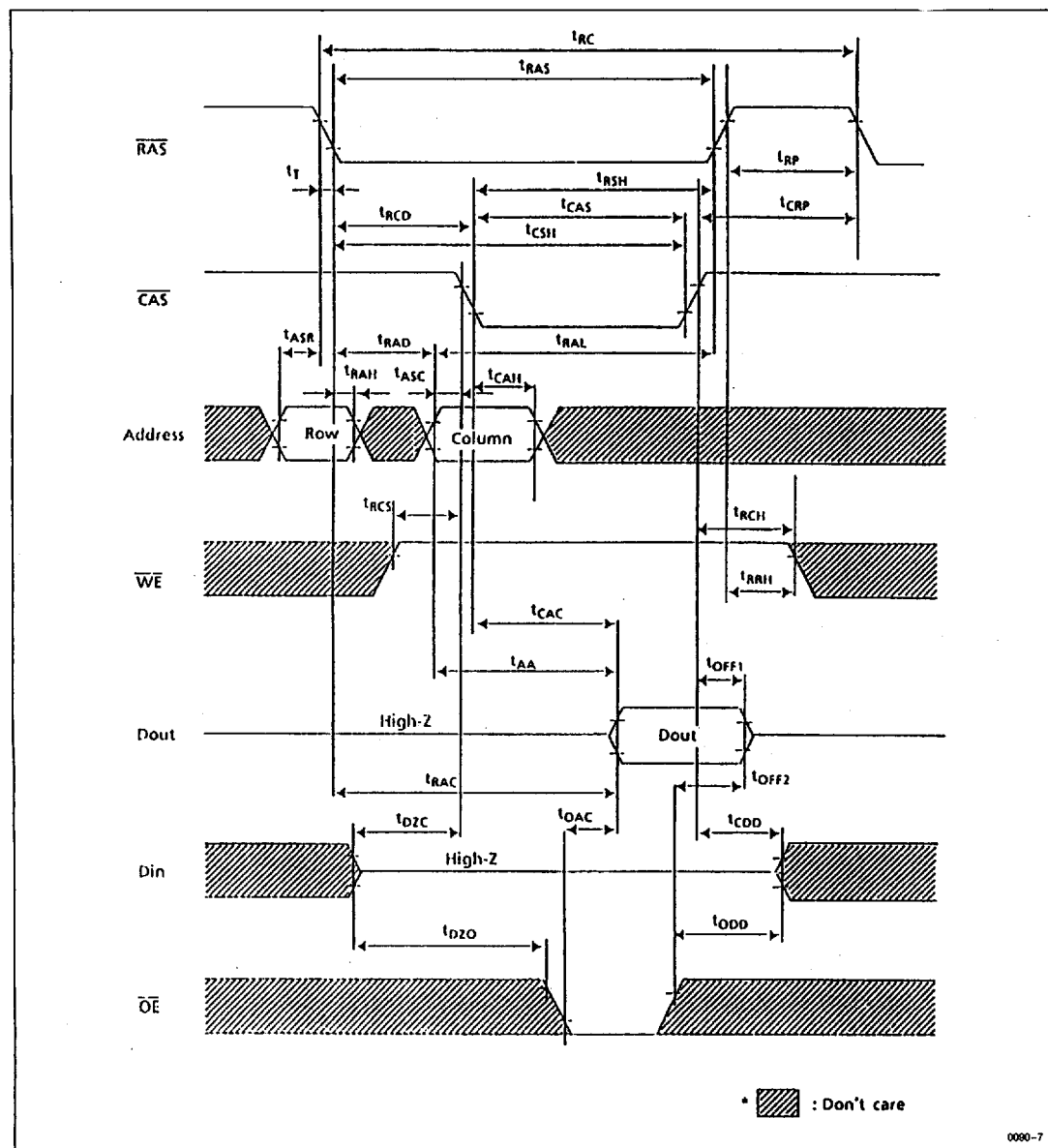
- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to \overline{CAS} leading edge in an early write cycle and to \overline{WE} leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines \overline{RAS} pulse width in fast page mode cycles.
 13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 14. An initial pause of 100 μ s is required after power up followed by a minimum of eight initialization cycles (\overline{RAS} only refresh cycle or \overline{CAS} before \overline{RAS} refresh cycle). If the internal refresh counter is used, a minimum of eight \overline{CAS} before \overline{RAS} refresh cycles is required.
 15. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
 16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits ... CA0. This test mode operation can be performed by \overline{WE} and \overline{CAS} before \overline{RAS} (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a \overline{RAS} only refresh cycle or a \overline{CAS} before \overline{RAS} refresh cycle.
 17. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} , t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.



■ TIMING WAVEFORMS

• Read Cycle

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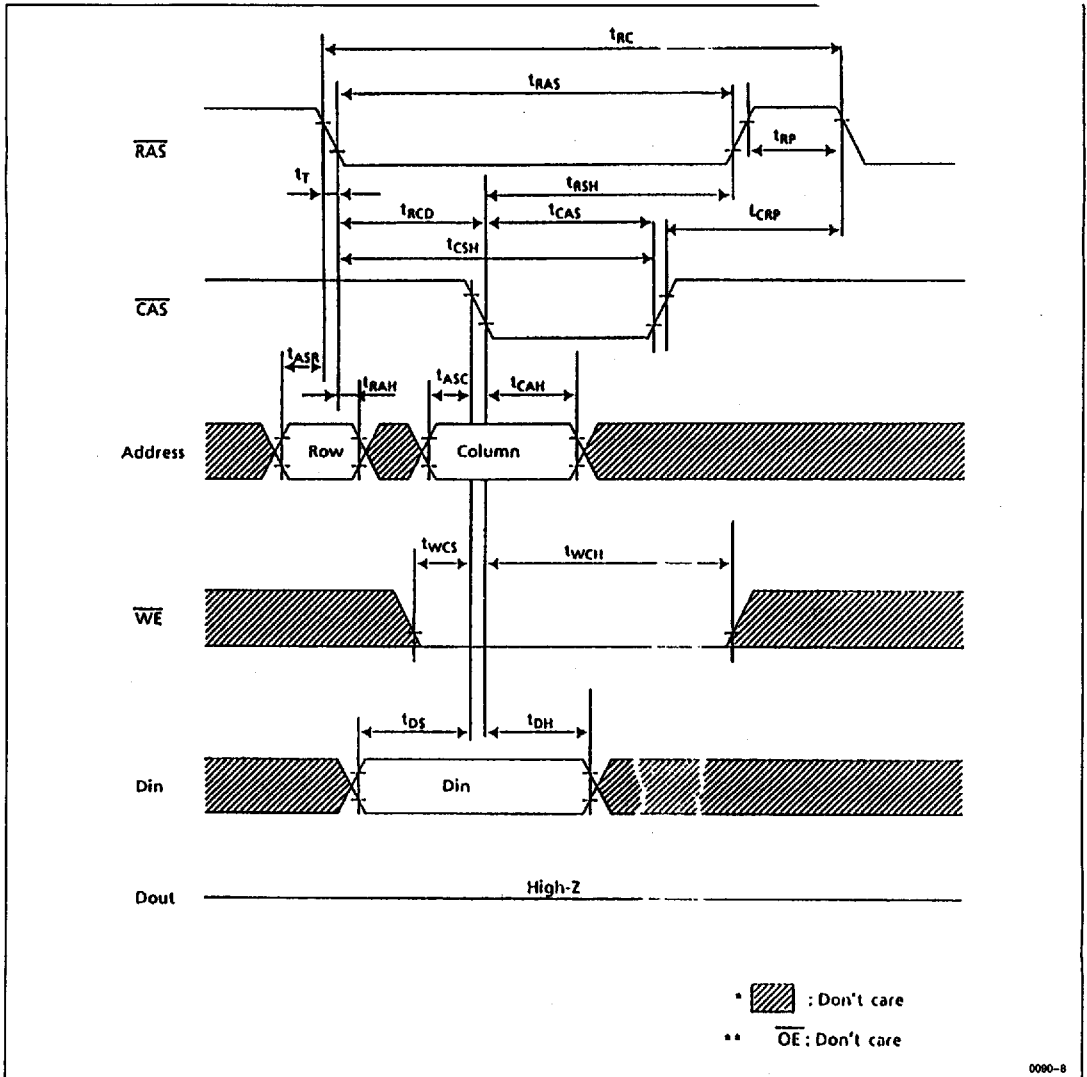
0080-7



HM514400A Series

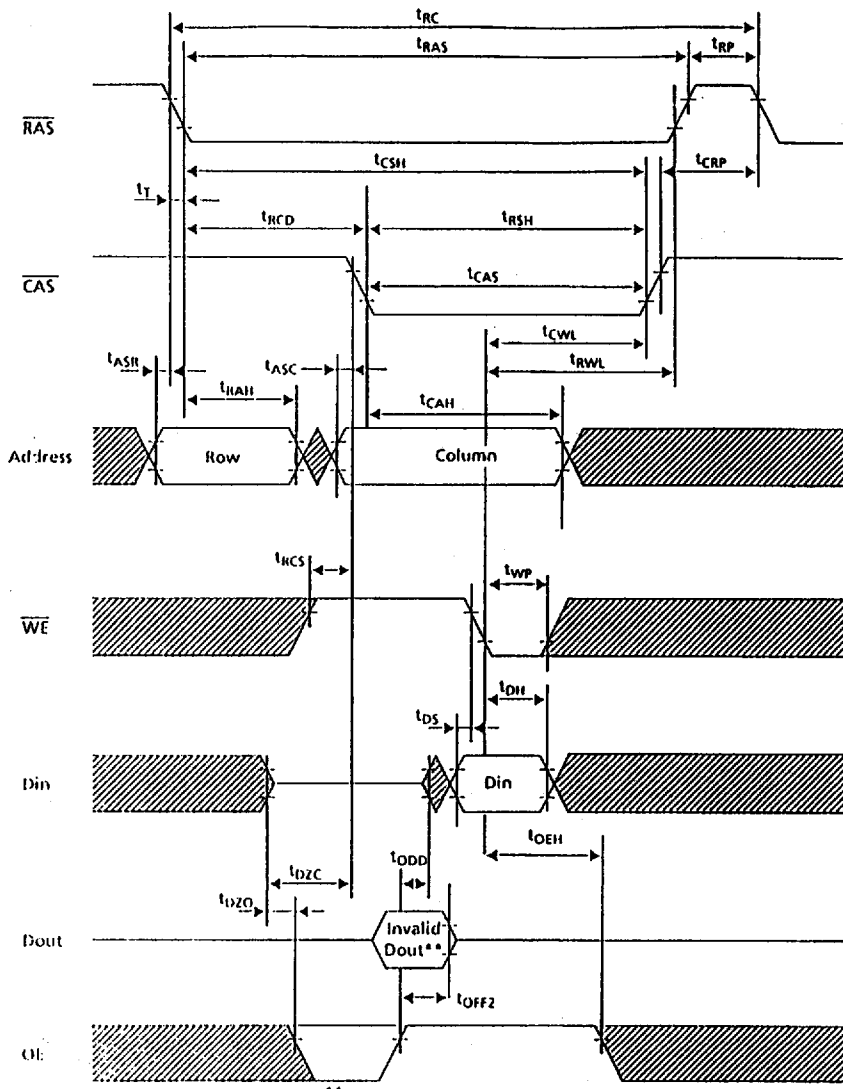
• Early Write Cycle

T-46-23-18



• Delayed Write Cycle

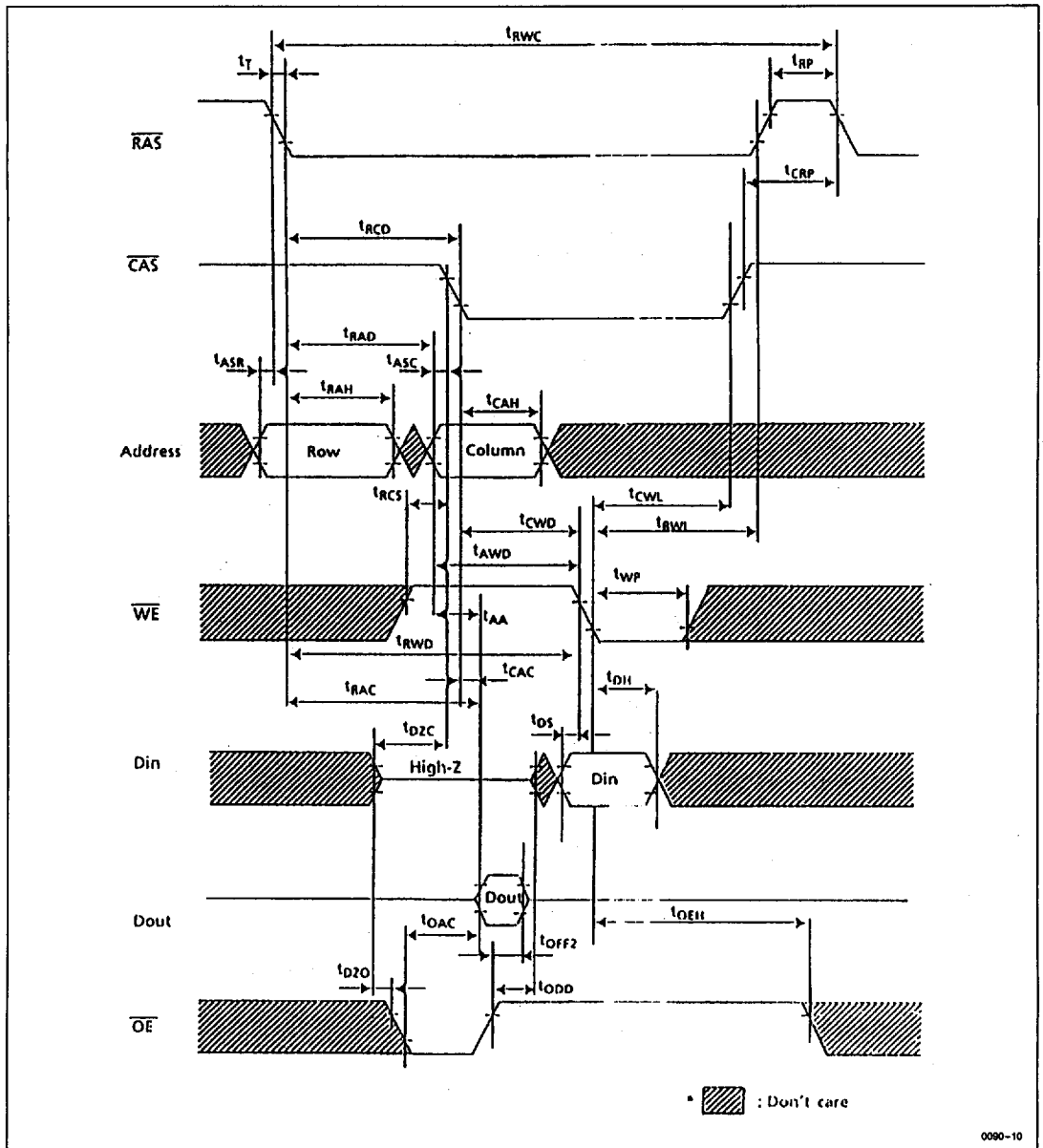
T-46-23-18



* : Don't care
 ** Invalid Dout comes out, when \overline{OE} is low level.

0000-9



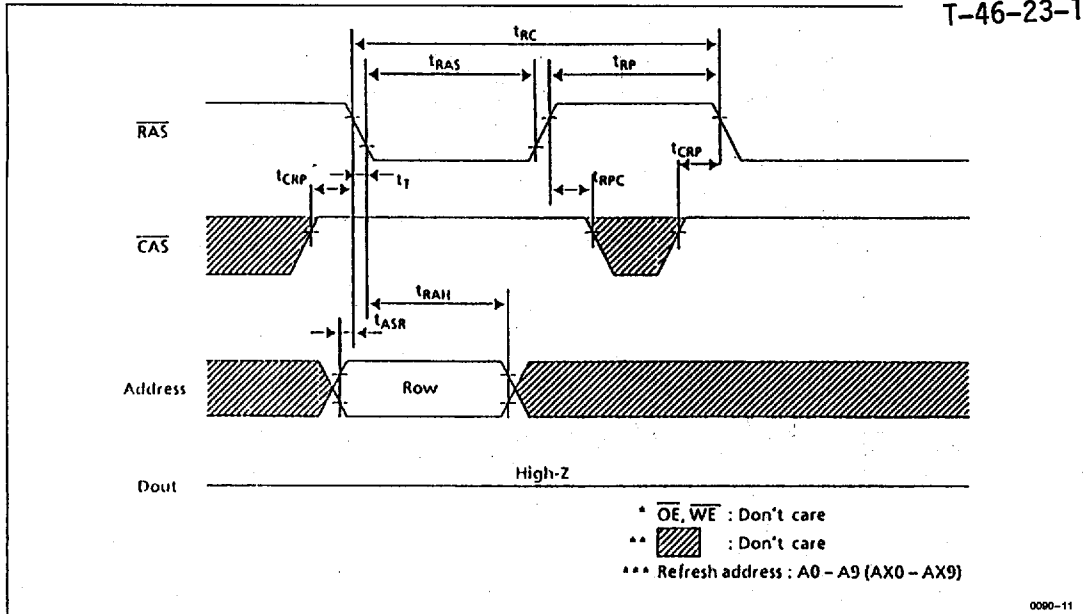


0090-10

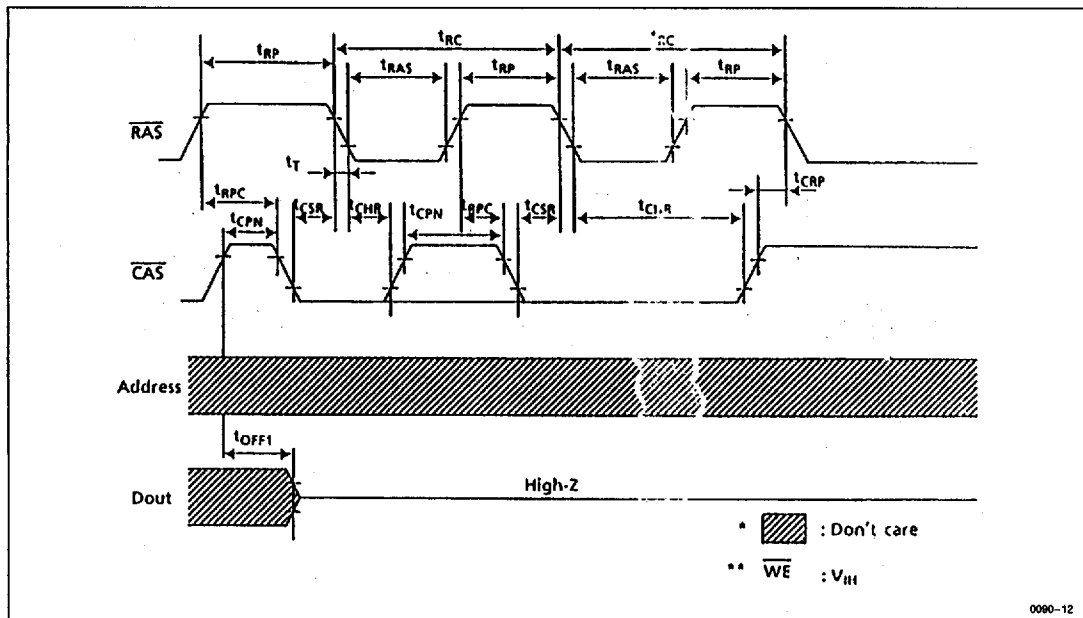


• RAS Only Refresh Cycle

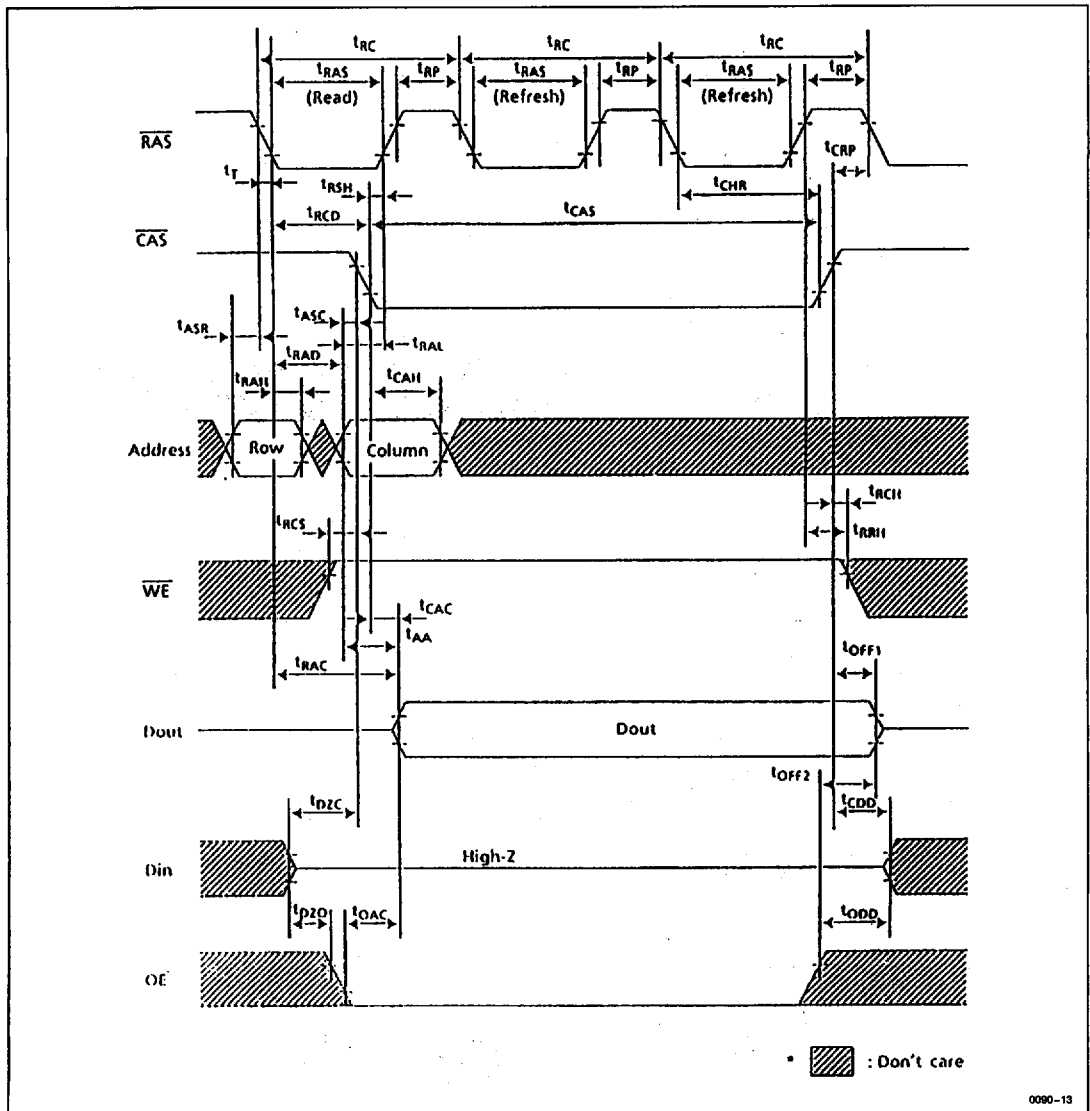
T-46-23-18



• CAS Before RAS Refresh Cycle

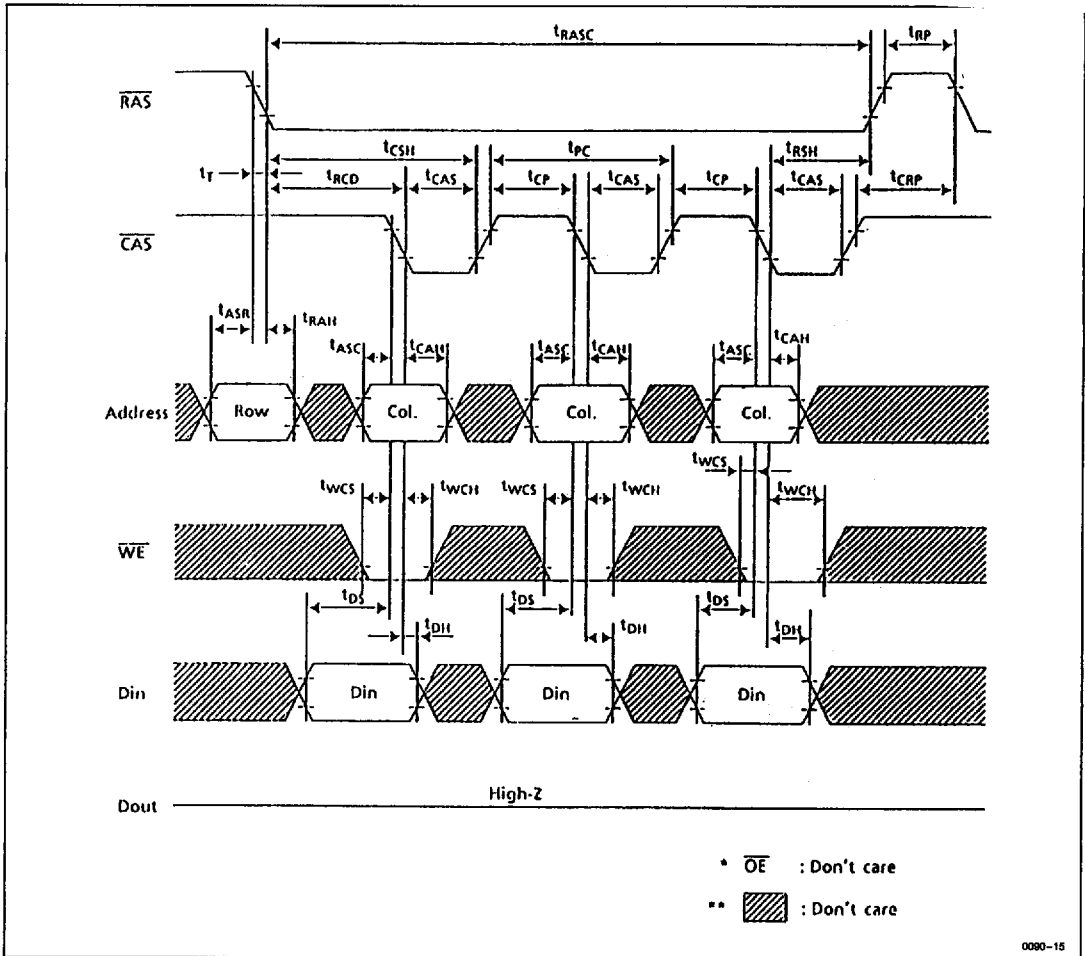


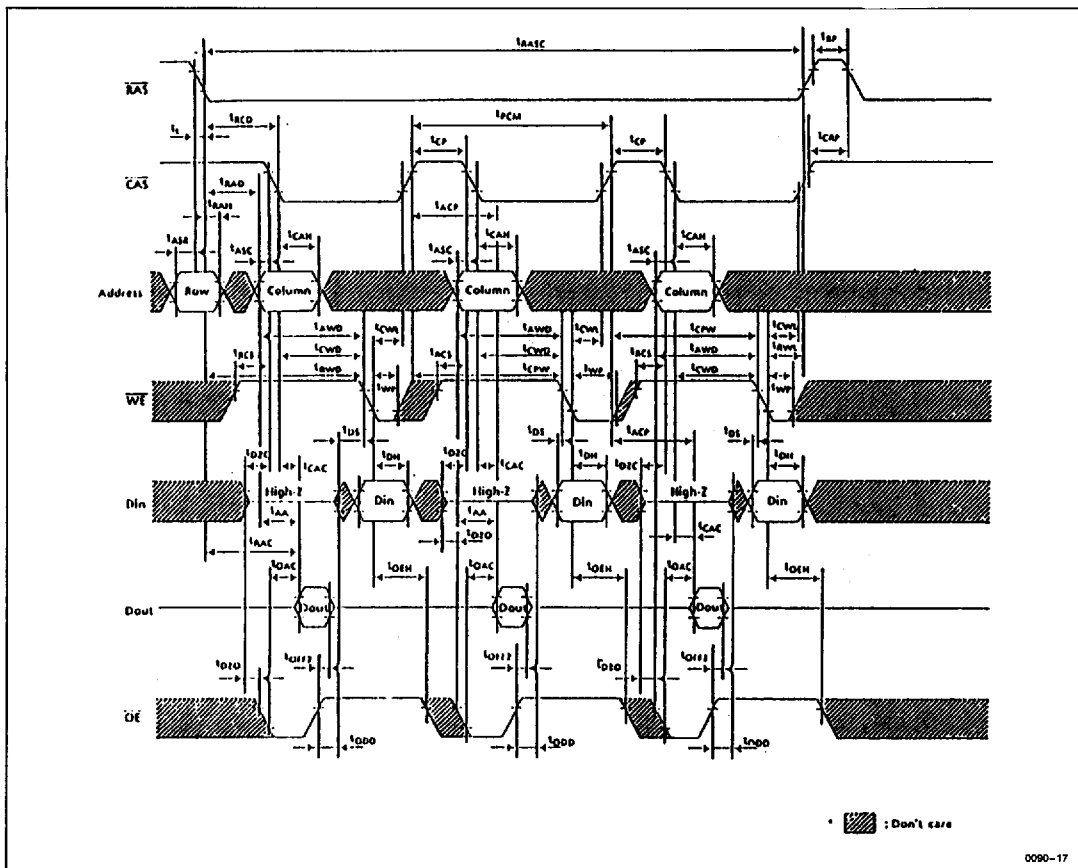
• Hidden Refresh Cycle



0090-13

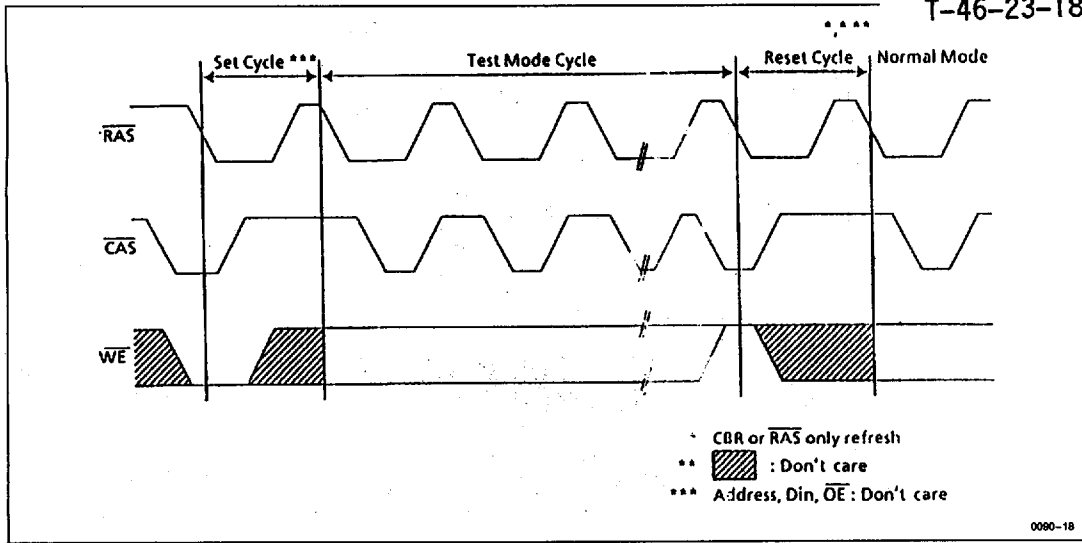




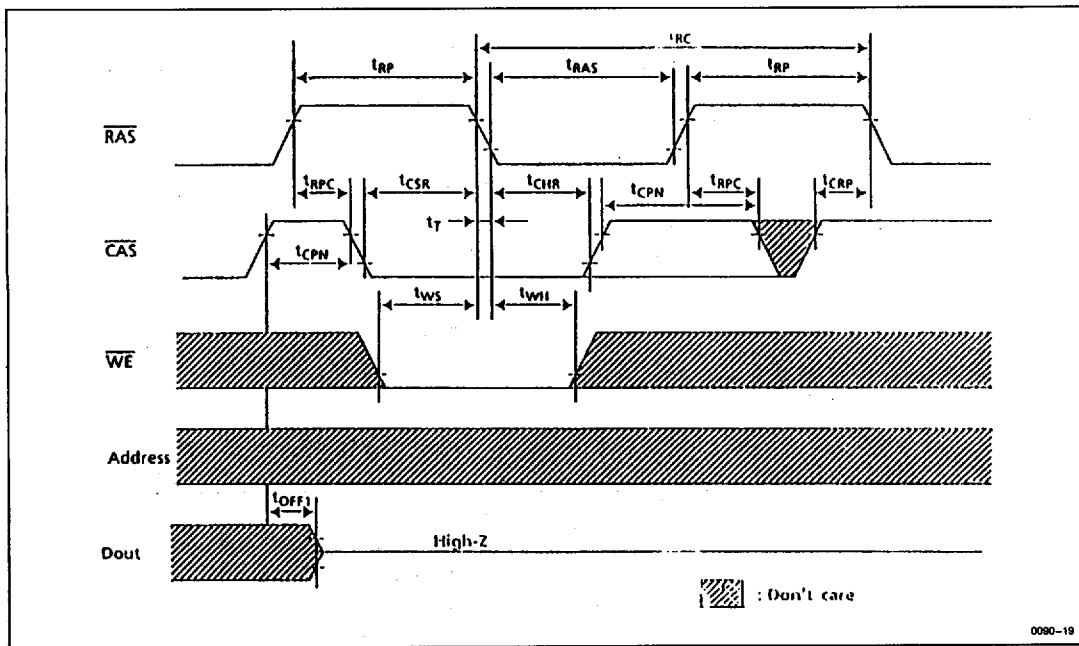


• TEST MODE CYCLE

T-46-23-18

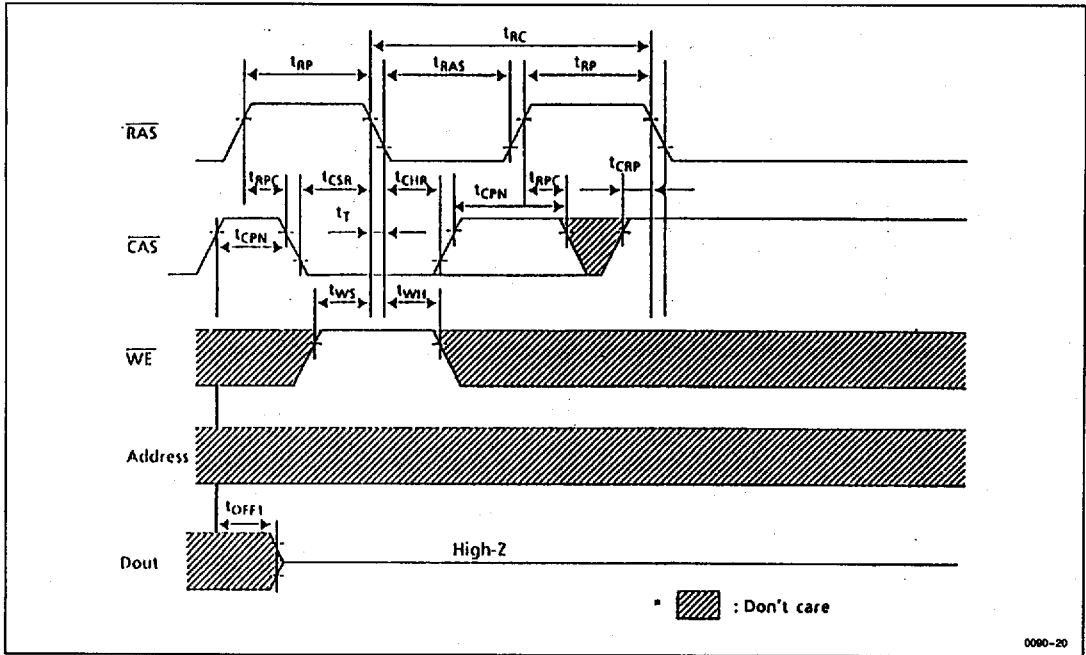


• Test Mode Set Cycle
WE And $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

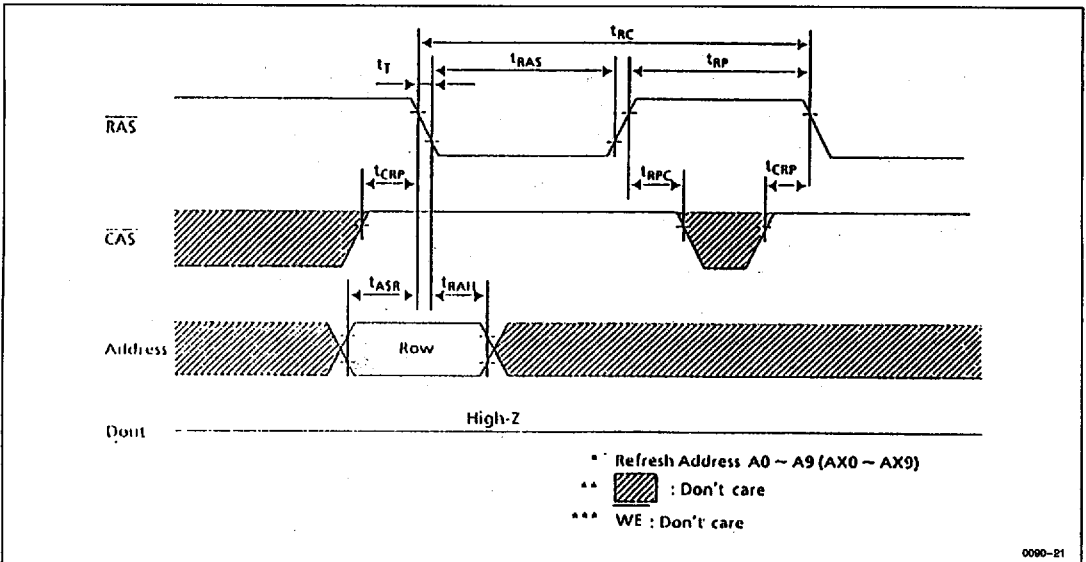


• Test Mode Reset Cycle

CAS Before RAS Refresh Cycle

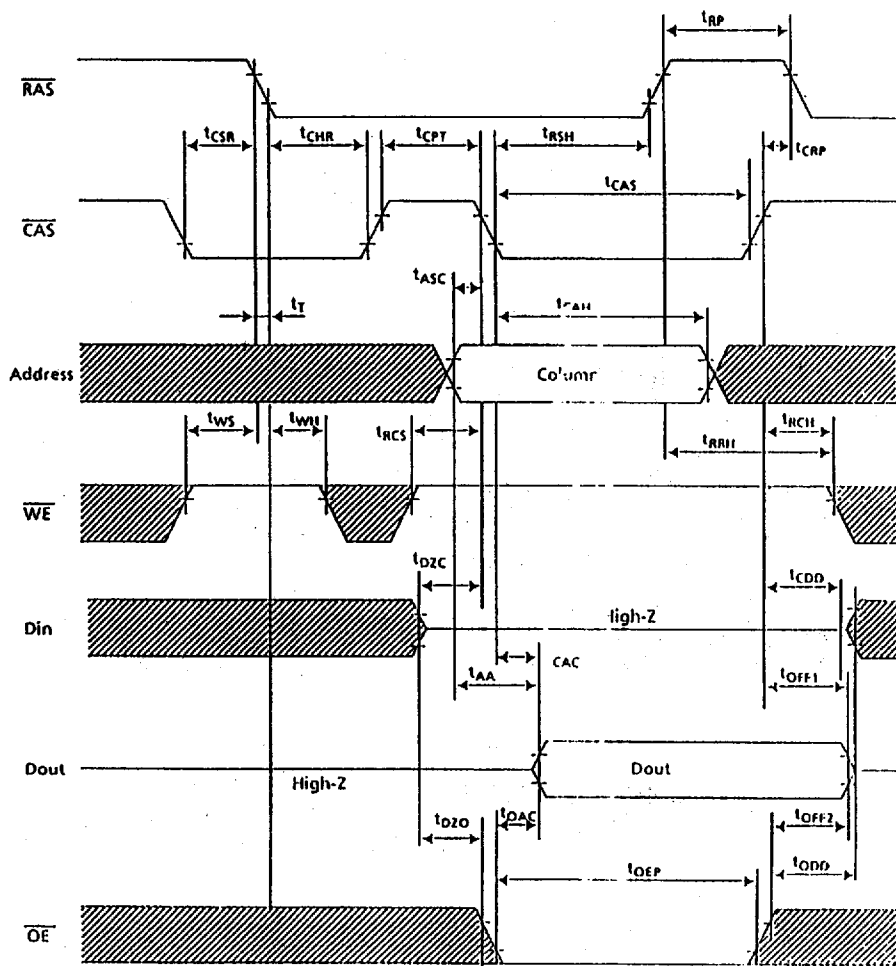


RAS Only Refresh Cycle



CAS Before RAS Refresh Counter Check Cycle (Read)

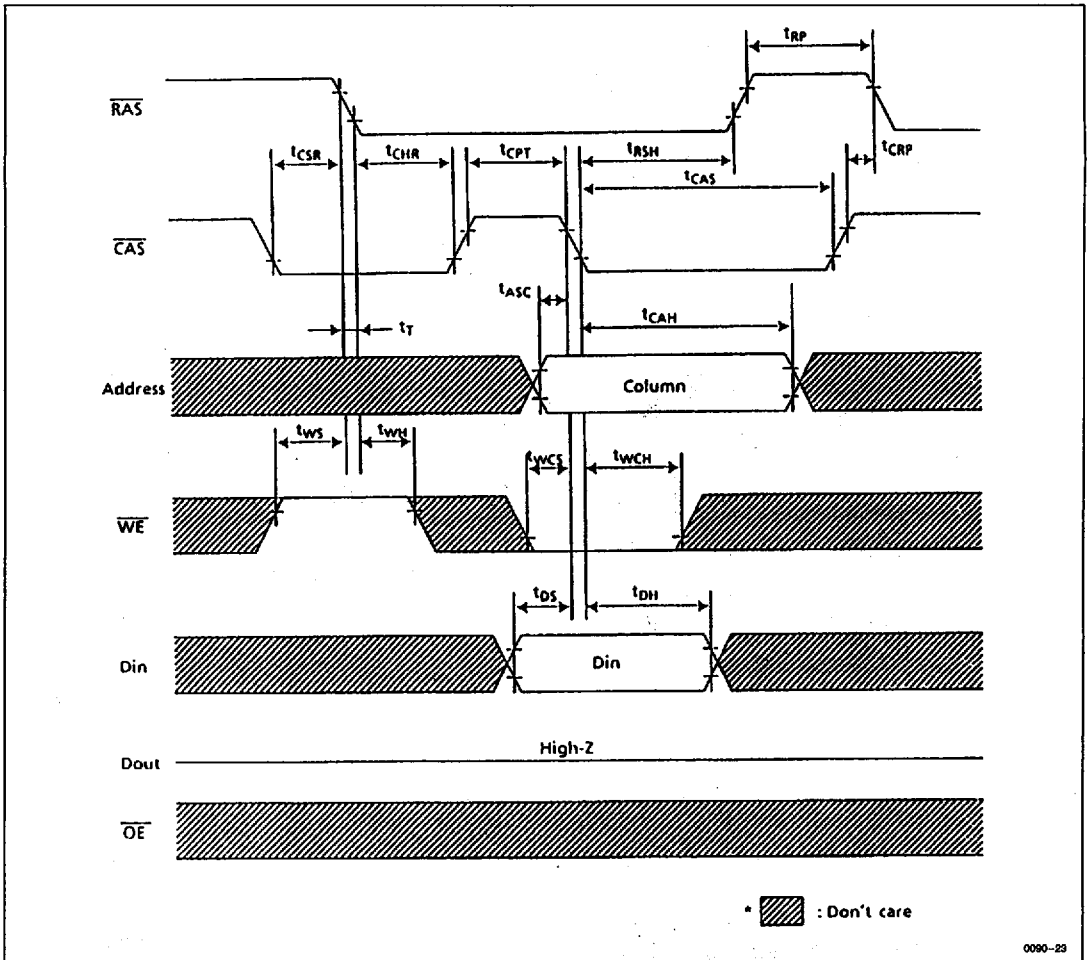
T-46-23-18



• [hatched box] : Don't care

0090-22

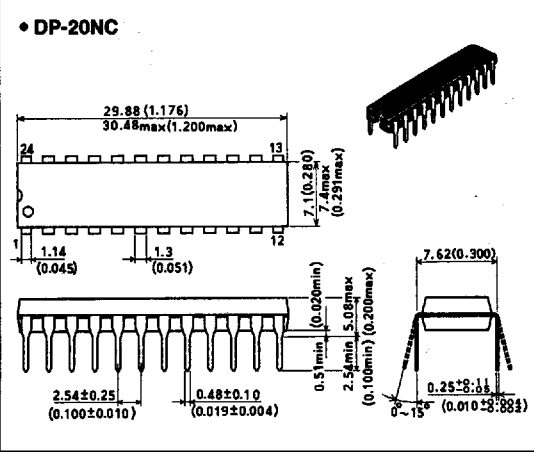
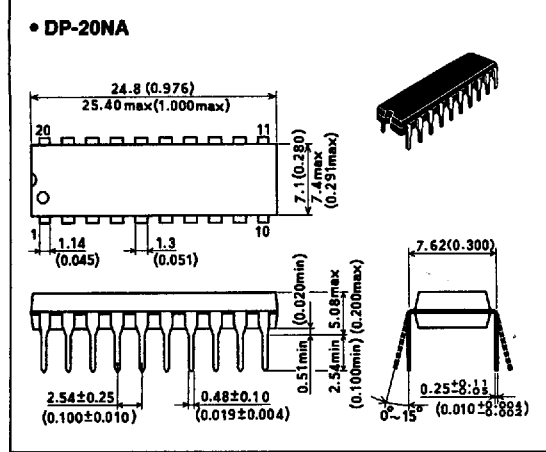
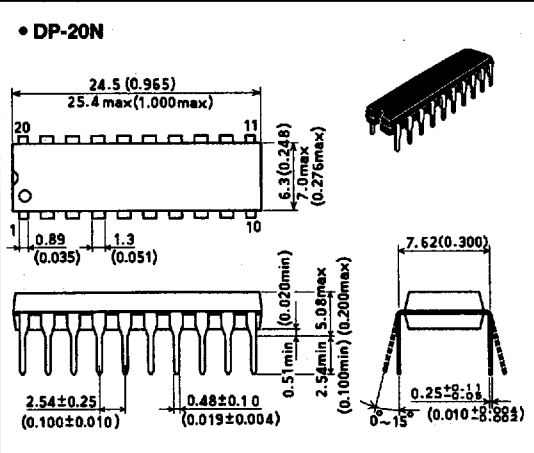
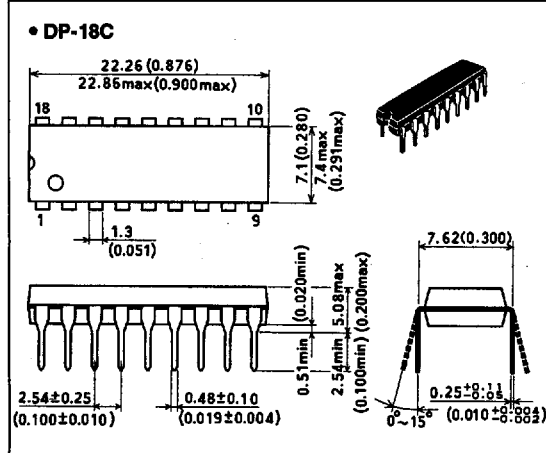
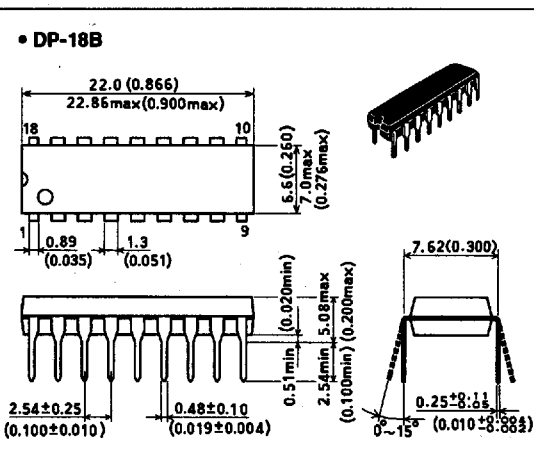
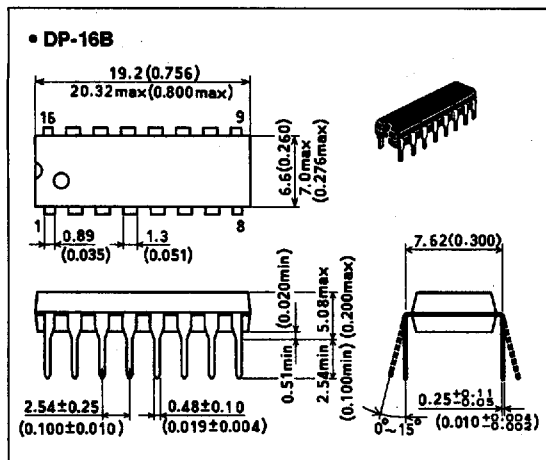




T-90-20

Unit: mm (inch) Scale 3/2

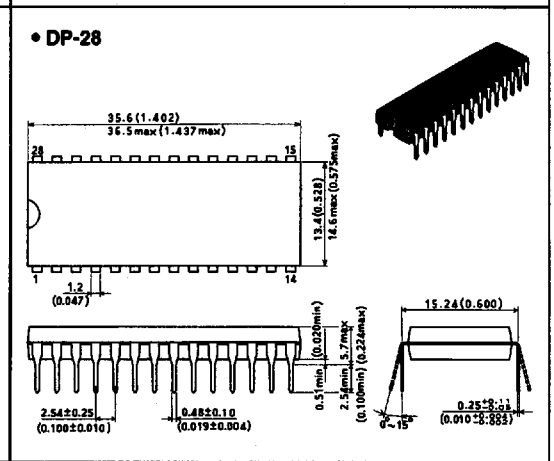
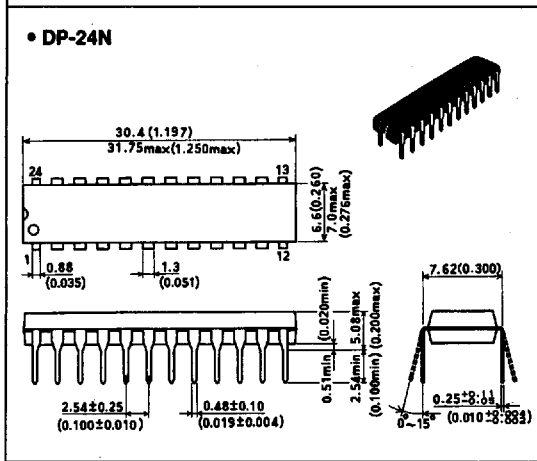
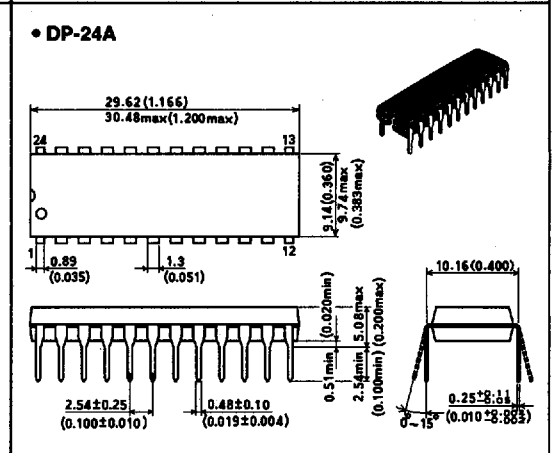
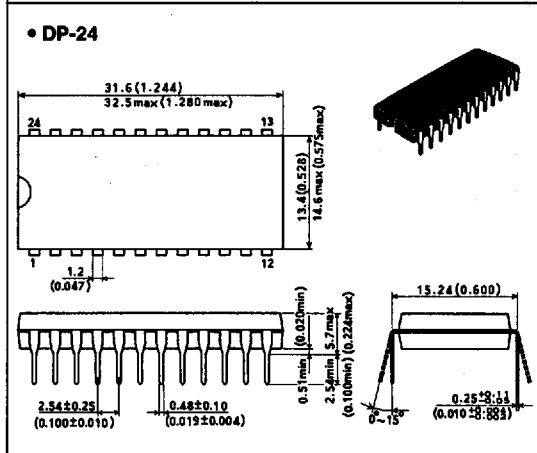
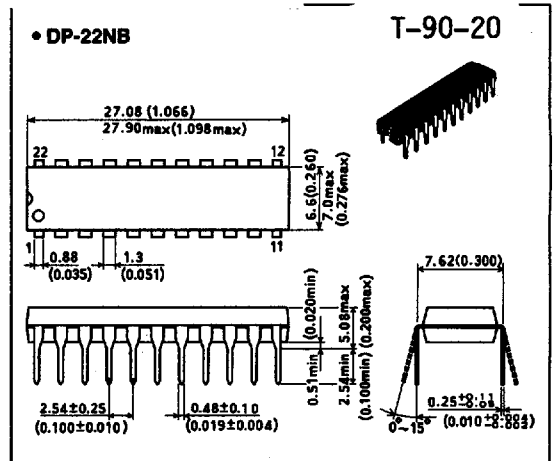
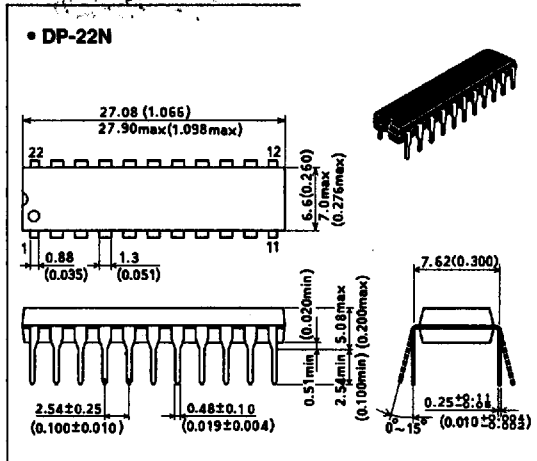
• Dual-in-line Plastic



• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2



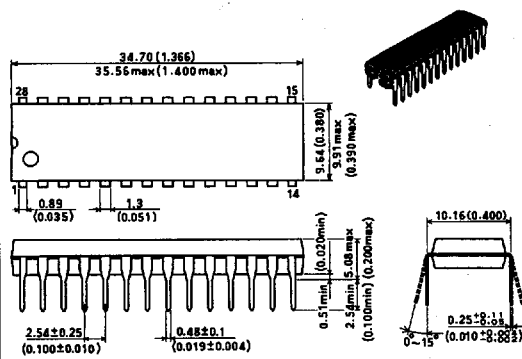
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

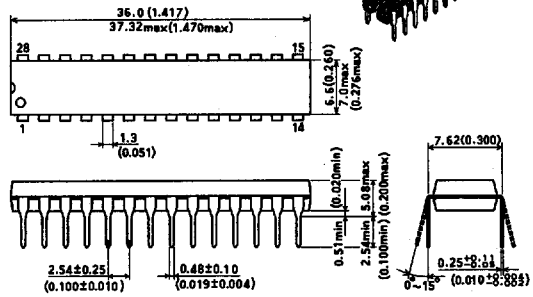
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

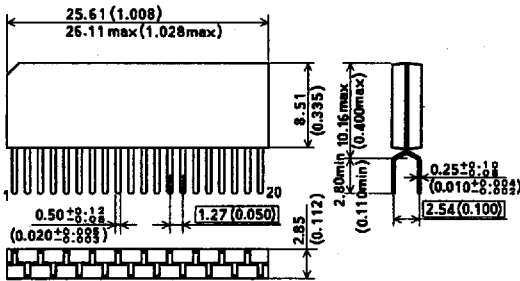
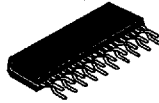


• Zigzag-in-line Plastic

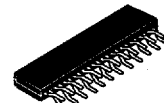
HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

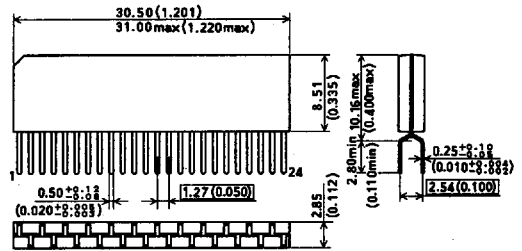
• ZP-20



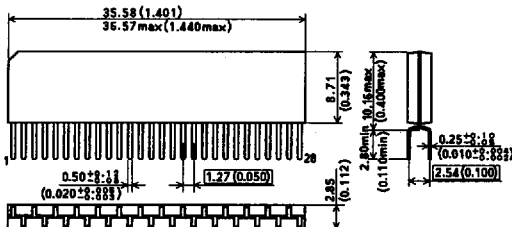
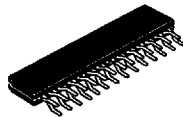
• ZP-24



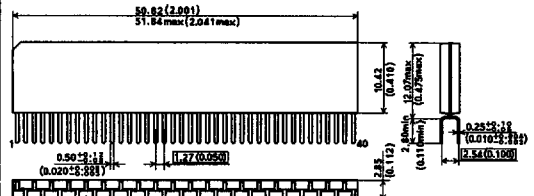
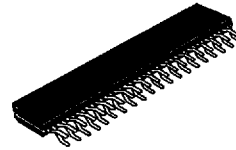
T-90-20



• ZP-28



• ZP-40



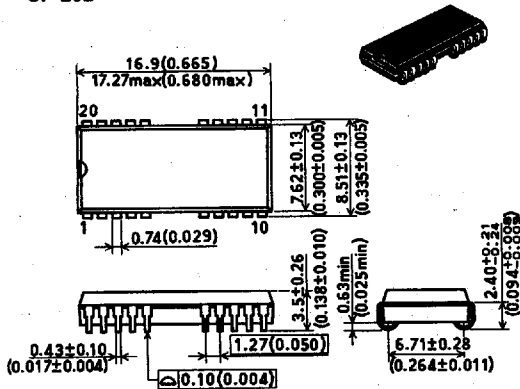
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

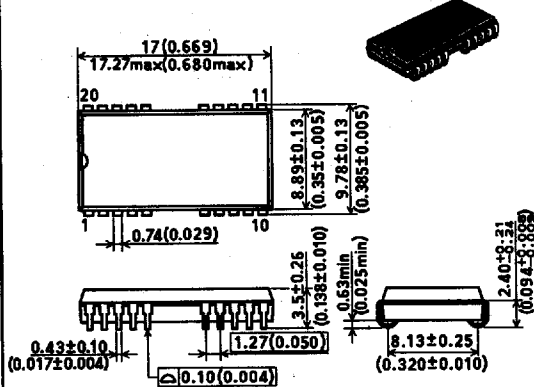
Unit: mm (inch) Scale 3/2

T-90-20

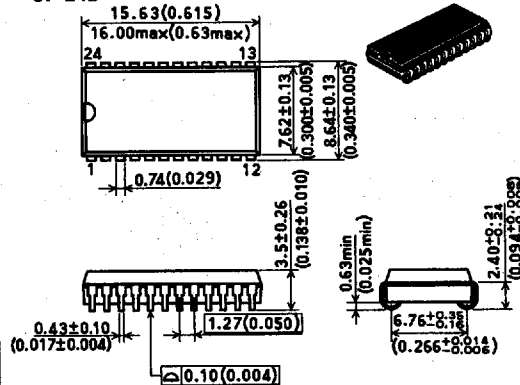
• CP-20D



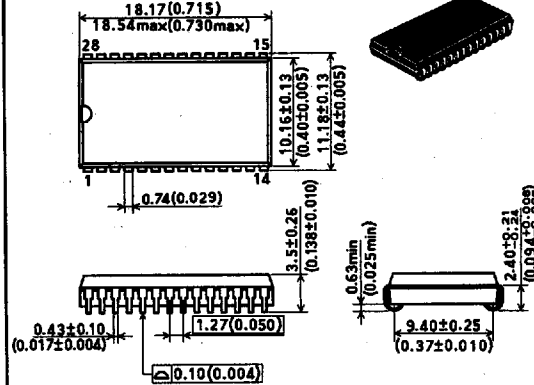
• CP-20DA



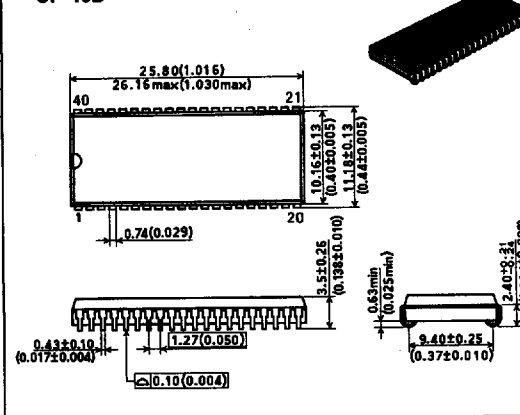
• CP-24D



• CP-28D



• CP-40D


HITACHI

• TSOP (Thin Small Outline Packag^e) HITACHI/ LOGIC/ARRAYS/MEM Unit: mm (inch) Scale 3/2

