
HB56G25632 Series

262,144-word $\times$ 32-bit High Density Dynamic RAM Module

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ADE-203-
Rev. 0.0
Dec. 1, 1995

Description

The HB56G25632B/SB is a 256 k $\times$ 32 dynamic RAM module, mounted 2 pieces of 4-Mbit DRAM (HM514260CJ/CLJ) sealed in SOJ package. An outline of the HB56G25632B/SB is 72-pin single in-line package. Therefore, the HB56G25632B/SB makes high density mounting possible without surface mount technology. The HB56G25632B/SB provides common data inputs and outputs. Decoupling capacitors are mounted beside each SOJ.

Features

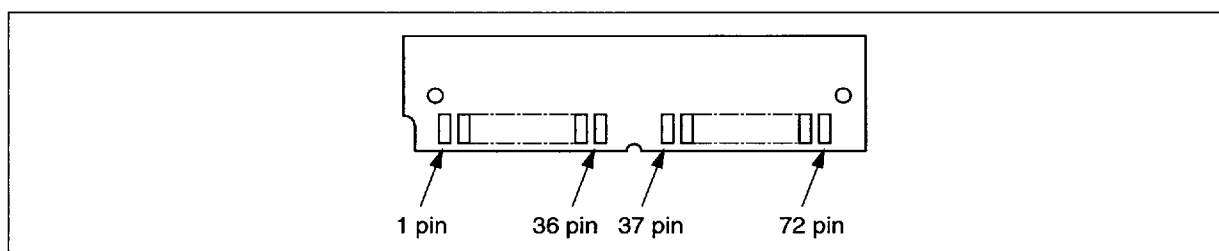
- 72-pin single in-line package
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm$ 5%) supply
- High speed
 - Access time: 70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 1.5 W/1.4 W (max)
 - Standby mode: 21 mW (max)
2.1 mW (max) (L-version)
- Fast page mode capability
- 512 refresh cycle: 8 ms
128 ms (L-version)
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

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Ordering Information

Type No.	Access time	Package	Contact pad
HB56G25632B-7C/7CL	70 ns	72-pin SIP socket type	gold
HB56G25632B-8C/8CL	80 ns		
HB56G25632SB-7C/7CL	70 ns	72-pin SIP socket type	solder
HB56G25632SB-8C/8CL	80 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	CAS0	58	DQ28
5	DQ17	23	DQ21	41	CAS2	59	V _{CC}
6	DQ2	24	DQ6	42	CAS3	60	DQ29
7	DQ18	25	DQ22	43	CAS1	61	DQ13
8	DQ3	26	DQ7	44	RAS0	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	WE	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	NC	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	RAS2	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

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Pin Description

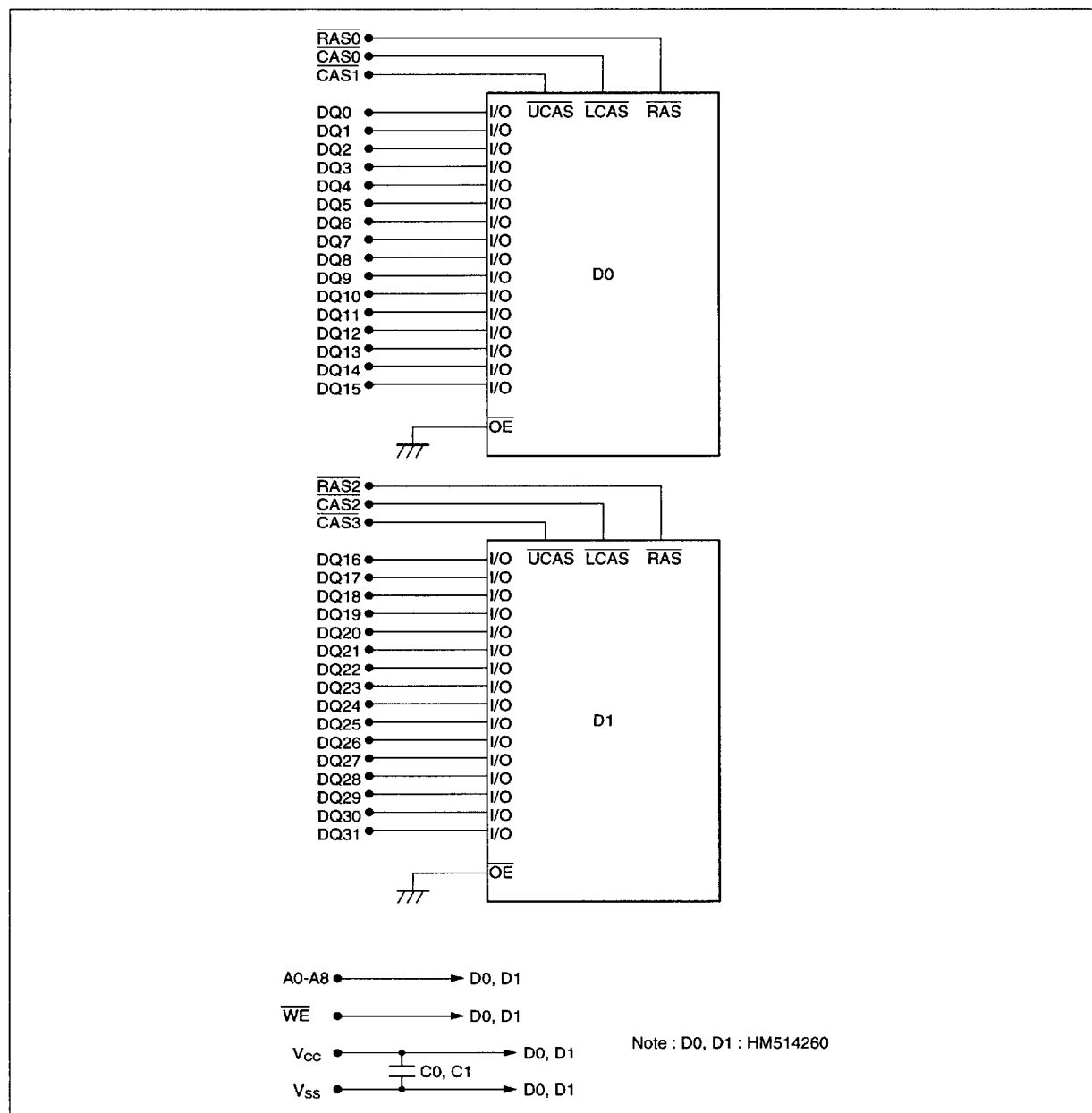
Pin name	Function
A0 – A8	Address input
A0 – A8	Refresh address input
DQ0 – DQ31	Data-in/data-out
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column address strobe
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row address strobe
$\overline{\text{WE}}$	Read/write enable
V_{cc}	Power supply (+5 V)
V_{ss}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56G25632B/SB	
Pin No.	Pin name	70 ns	80 ns
67	PD1	V_{ss}	V_{ss}
68	PD2	NC	NC
69	PD3	V_{ss}	NC
70	PD4	NC	V_{ss}

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Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	2	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	35	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	34	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	27	pF	1
I/O capacitance	C_{VO}	—	19	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable Dout.

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)

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Parameter	Symbol	70ns		80ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I _{CC1}	—	280	—	250	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	4	—	4	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	2	—	2	mA	CMOS interface RAS, CAS, WE ≥ V _{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I _{CC2}	—	0.4	—	0.4	mA	CMOS interface RAS, CAS, WE ≥ V _{CC} – 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	260	—	220	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	10	—	10	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	260	—	220	mA	t _{RC} = min	2
Page mode current	I _{CC7}	—	260	—	240	mA	t _{PC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I _{CC10}	—	0.6	—	0.6	mA	CMOS interface CBR refresh: t _{RC} = 250 μs t _{RAS} ≤ 1 μs, WE = V _{IH} CAS = V _{IL} , Dout = High-Z	4
Input leakage current	I _{LI}	–10	10	–10	10	mA	0 V ≤ Vin ≤ 6.5 V	
Output leakage current	I _{LO}	–10	10	–10	10	mA	0 V ≤ Vout ≤ 6.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = –5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.

3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

4. $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $0 \leq V_{IL} \leq 0.2\text{ V}$, Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.

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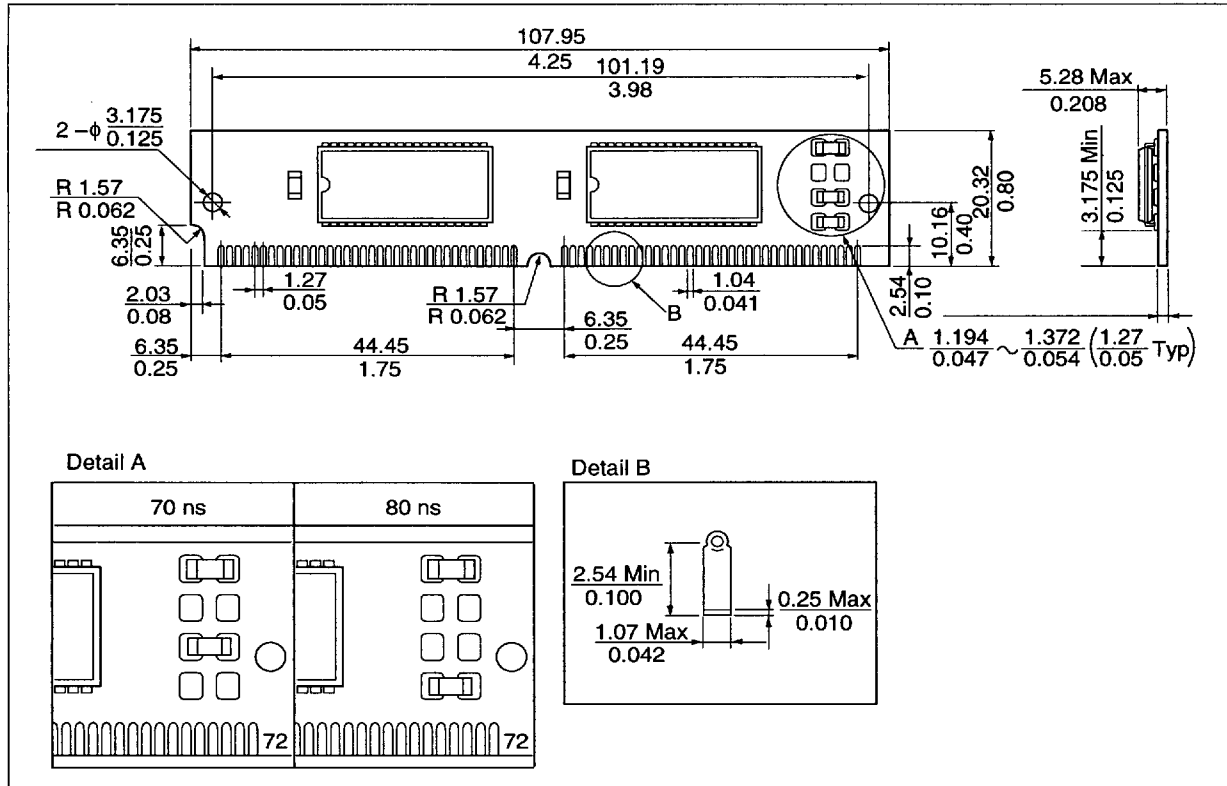
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AC Characteristics

- Refer to the HM514260C data sheet.
- The HB56G25632 writes data only in early write cycle ($t_{wcs} \geq t_{wcs}(\min)$).
Delayed write cycle is not available. ($\overline{OE}$ pin is fixed to V_{ss}).

Physical Outline

Unit: mm/inch



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