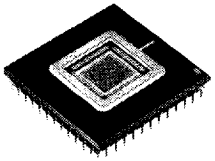
DDC
ILC DATA DEVICE CORPORATION®

BU-65612



MIL-STD-1553 BUS CONTROLLER REMOTE TERMINAL AND BUS MONITOR

Contact Factory For BUS-65612 (CMOS SOS Version)

DESCRIPTION

The BU-65612 is a 16 MHz single chip dual redundant MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT). Packaged in a Pin Grid Array (PGA), the BU-65612 performs all the functions required to interface a MIL-STD-1553 dual redundant serial data bus transceiver, such as DDC's BUS-63125, and a subsystem parallel three-state data bus.

Using a single DDC custom monolithic CMOS IC, the BU-65612 features pin-for-pin and functional BUS-65600 compatibility, user-initiated self-test, and low power consumption.

Compatible with most microprocessors, the BU-65612 provides a 16-bit three-state parallel data bus and uses direct memory access (DMA type) handshaking for subsystem transfers.

All message transfer timing, DMA, and control lines are provided internally, thereby reducing the subsystem overhead associated with message transfers.

The BU-65612 implements all dual redundant MIL-STD-1553 mode codes. In addition, any mode code may (optionally) be illegalized through the use of an external PROM. Complete error detection is provided by the BU-65612 for BC and RTU operation. Error detection includes: response time-out, inter-message gaps, sync, parity, Manchester, word count, and bit count. The BU-65612 is fully compliant with MIL-STD-1553 and operates over the full military temperature range of -55°C to +125°C — making it an excellent choice for MIL-STD-1553 applications.

FEATURES

- *COMPLETE BC, RTU, OR MT OPERATION*
- *16 MHz SINGLE CHIP BUS-65600 REPLACEMENT*
- *CMOS TECHNOLOGY*
- *PGA PACKAGES*
- *IMPLEMENTS ALL DUAL REDUNDANT MODE CODES*
- *SELECTIVE MODE CODE ILLEGALIZATION AVAILABLE*
- *BC CHECKS STATUS WORD FOR CORRECT ADDRESS AND SET FLAGS*
- *DMA HANDSHAKING FOR SUBSYSTEM MESSAGE TRANSFERS*
- *CONTINUOUS ON-LINE AND INITIATED BUILT-IN-TEST*

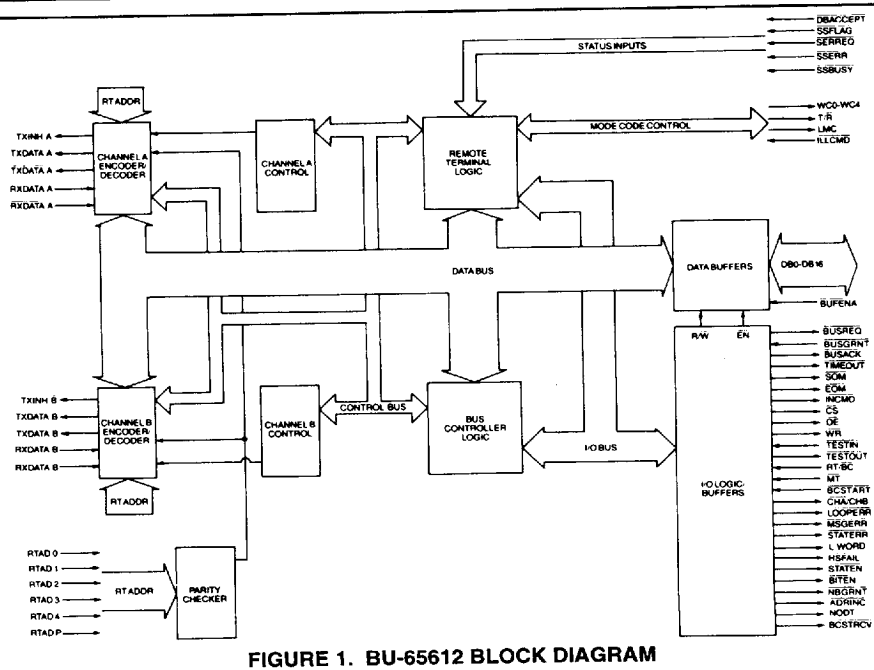


FIGURE 1. BU-65612 BLOCK DIAGRAM

TABLE 1. BU-65612 PIN FUNCTIONS (PGA)			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
A01	TIM2	C05	A RX
A02	A NBRQ	C06	TESTENA
A03	PCLK	C07	VSS
A04	A RX	C08	RTAD1
A05	B RX	C09	VDD
A06	PARENA	C10	BRO
A07	RTADPAR	C11	NW
A08	RTAD3	C12	LMC
A09	RTAD0	C13	SA3 MC3
A10	CLKRST	D01	DB10
A11	ND	D02	DB12
A12	VW	D03	DB15
A13	VA	D11	RTFAIL
B01	VDD	D12	SA2 MC2 B8
B02	LOOPERR	D13	SA0 MC0 B6
B03	RTPARERR	E01	DB08
B04	TEST1	E02	DB09
B05	B RX	E03	DB11
B06	BROENA	E11	SA1 MC1 B7
B07	RTAD4	E12	WC4 CWC4 B5
B08	RTAD2	E13	WC3 CWC3 B4
B09	CLK	F01	DB05
B10	TIM1	F02	DB06
B11	MC	F03	DB07
B12	CMD	F11	WC2 CWC1 B3
B13	SA4 MC4	F12	WC1 CWC1 B2
C01	DB13	F13	WC0 CWC0 B1
C02	DB14	G01	DB02
C03	TD	G02	DB04
C04	B NRBQ	G03	DB03

TABLE 1. BU-65612 PIN FUNCTIONS (PGA) (Continued)			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
K03	A TX	N01	VSS
K11	BUFENA2	N02	TS0
K12	BUSGRNT	N03	LWORD
K13	ILLCMD	N04	OE
L01	B TX	N05	CS
L02	CYCENA	N06	INCMD
L03	MT	N07	ERROR
L04	TEST2	N08	ADRINC
L05	R/W	N09	BUSACK
L06	SOM	N10	BUSREQ
L07	EOM	N11	T/R
L08	CMDTRF	N12	GBR
L09	BITEN	N13	VSS
L10	STATEN	G11	WCMUXENA
L11	CSTINH	G12	VDD
L12	WRMASK	G13	SAMUXENA
L13	RESET	H01	DB01
M01	A TX	H02	DB00
M02	TS1	H03	TIMEOUT
M03	HSFAIL	H11	SVCRQST
M04	STATSET	H12	SEL2
M05	WR	H13	SSFLAG
M06	INCMD	J01	TACT
M07	ME	J02	CH B/A
M08	DTSTR	J03	A TXINH
M09	TIMERR	J11	RTFLAG
M10	DBACC	J12	ADBC
M11	NBGRNT	J13	SSBUSY
M12	RT/BC	K01	B TXINH
M13	BUFENA1	K02	B TX

ORDERING INFORMATION

BU-65612- P 0 - 1 4 0

- **Test Criteria:**
  - 0 = None
- **Screening:**
  - 0 = Commercial Screening/No Burn-In
  - 1 = Fully compliant to MIL-STD-883
  - 2 = Screened to MIL-STD-883 but without QCI testing
  - 4 = 883B and Solder Dip
- **Temperature Range:**
  - 1 = -55 to +125°C
  - 3 = 0 to +70°C
- **Options:**
  - 0 = None
- **Packaging:**
  - P = PGA (Pin Grid Array)

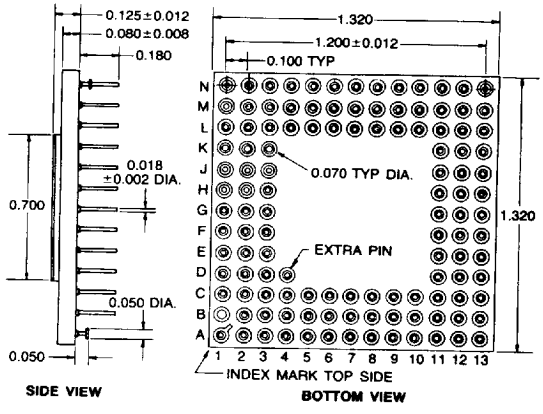


FIGURE 2. BU-65612P0 MECANICAL OUTLINE (PGA)

A